TRANSACTIONS ON ELECTRICAL AND ELECTRONIC MATERIALS
Vol. 12, No. 6, pp. 245-248, December 25, 2011

Regular Paper

pISSN: 1229-7607 eISSN: 2092-7592
DOI: http://dx.doi.org/10.4313/TEEM.2011.12.6.245

Modeling Electrical Characteristics for Multi-Finger MOSFETs Based on Drain Voltage Variation

Mingu Kang and Ilgu Yun†
Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Korea

Received August 22, 2011; Revised September 19, 2011; Accepted October 20, 2011

The scaling down of metal oxide semiconductor field-effect transistors (MOSFETs) for the last several years has contributed to the reduction of the scaling variables and device parameters as well as the operating voltage of the MOSFET. At the same time, the variation in the electrical characteristics of MOSFETs is one of the major issues that need to be solved. Especially because the issue with variation is magnified as the drive voltage is decreased. Therefore, this paper will focus on the variations between electrical characteristics and drain voltage. In order to do this, the test patterned multi-finger MOSFETs using 90-nm process is used to investigate the characteristic variations, such as the threshold voltage, DIBL, subthreshold swing, transconductance and mobility via parasitic resistance extraction method. These characteristics can be analyzed by varying the gate width and length, and the number of fingers. Through this modeling scheme, the characteristic variations of multi-finger MOSFETs can be analyzed.

Keywords: Multi-finger metal oxide semiconductor field-effect transistors, Modeling, Characteristic variation

1. INTRODUCTION

Downscaled metal oxide semiconductor field-effect transistors (MOSFETs) have been in progress for several years and were displayed in the 2009 International Technology Roadmap for Semiconductors (ITRS) [1]. The scaled down MOSFET has many advantages, such as integration of chip density, low voltage operation, driving current enhancement, and so on [2]. However, the variations in the electrical characteristics of MOSFET are an inevitable phenomenon and it must be overcome. This paper focuses on the modeling and analysis of the electrical characteristics of the multi-finger MOSFET according to the drain voltage variation.

When the multi-finger MOSFET is operated by changing drain voltage, the electrical characteristics are affected. Due to scaling down and the driving voltage variation, the scaling variables and device parameters also became smaller. Thus, electrical characteristic variations will be primarily focused on drain voltage variation. In addition, the electrical properties are also analyzed by varying the gate width and length and the number of fingers. By observing these variations, the behavior of downscaled multi-finger MOSFETs can be estimated via parameterization.

In this paper, the multi-finger MOSFETs are fabricated using a commercial 90 nm process to investigate the characteristic variations. To build the device model, a parasitic resistance extraction method is used. Here, the characteristic variations of threshold voltage (V_{th}), subthreshold swing (S_{sub}), drain induced barrier lowering (DIBL), transconductance (g_m), and mobility (μ_{FEmax}) are analyzed where the drain voltage and the gate structures are varying at the same time.

2. MODELING METHODOLOGY

The multi-finger MOSFETs can be used in various applications since they have a large value of g_m and it can control the current flow effectively. In addition, it can enhance the driving current because the multi-finger MOSFET has low gate resistance. Figure 1 is a basic schematic structure of a multi-finger MOSFET.

In Fig. 1, L_f is the length of gate, W_f is the width of gate, and N_f is the number of fingers. Thus, the total gate width of the tested

† Author to whom all correspondence should be addressed:
E-mail: iyun@yonsei.ac.kr

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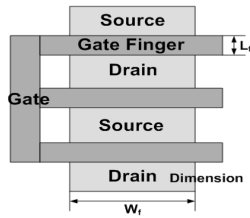

Fig. 1. Basic structure of multi-finger metal oxide semiconductor field-effect transistor.

Table 1. Summary of the test structure information for each group.

Group	Name	N_f	L_f (μm)	W_f (μm)	W_{total} (μm)	Active dimension (μm)^2
A	A1	4	0.09	2	8	2.72
	A2	(fixed)	(fixed)	4	16	5.44
	A3			6	24	8.16
B	B1	3	0.09	4	12	4.28
	B2	4	(fixed)	(fixed)	16	5.44
	B3	5			20	6.6
	B4	6			24	7.76
	B5	7			28	8.92
	B6	8			32	10.08
C	C1	4	0.07	6	24	7.68
	C2	(fixed)	0.09	(fixed)	(fixed)	8.16
	C3		0.11			8.64
	C4		0.13			9.12

MOSFET can be represented by the following equation:

$$W_{total} = W_f \times N_f \tag{1}$$

In this paper, the test patterned multi-finger MOSFETs that change the gate structure are used to build a model and analyze the characteristics. Varying the gate width and length and the number of fingers was used to measure and investigate for variations.

The three groups of test structures are fabricated and used for analysis in this work. Here, group A consists of the test structures varying with the gate width, and group B consists of the structures varying with the number of gate fingers. It is noted that the total gate width of groups A and B are changed using different geometric factors. Finally, group C consists of the structures varying with the gate length. The group information can be summarized in Table 1.

The multi-finger MOSFETs used in this paper were manufactured in a common-source configuration. These test MOSFETs have a ground-signal-ground pad pattern that is designed with a pitch of 75 μm.

In order to measure the current-voltage characteristics, an HP 4145B semiconductor parameter analyzer was used. The measured data is stored with the aid of software and equipment. For the output characteristics (I_D-V_{DS}), the drain voltage is measured from 0 V to 0.9 V while the gate voltage is increased from 0.3 V to 1.2 V with a step of 0.3 V. In addition, the transfer characteristic (I_D-V_G) is derived by sweeping the gate voltage from 0.0 V to 1.2 V while the drain voltage is increased from 0.1 V to 0.7 V with a step of 0.2 V.

To extract the electrical characteristics of multi-finger MOSFETs, the parasitic resistance model is used in this paper [3]. In order to build the device model, a Berkeley short-channel insulated gate field effect transistor model 4 is based on the core

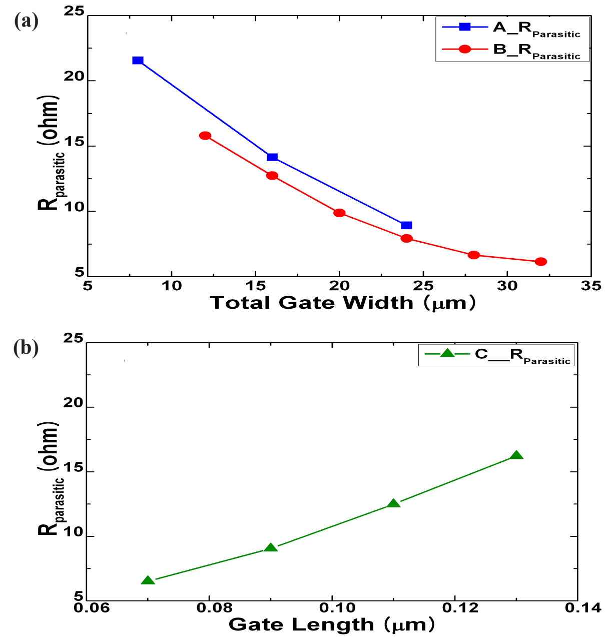

Fig. 2. Total parasitic resistance according to the gate geometric variations.

model. By connecting additional parasitic resistance for each terminal, it can complete the model. There are four different variables and they are optimized in the modeling process. The HSpice simulation program is used to extract the parasitic resistances via the I_D-V_{DS} output characteristic. The transfer characteristic is used to calculate V_{th}, DIBL, S_{sub}, g_m, and μ_{FEmax}.

3. RESULTS AND DISCUSSION

The sum of the optimized R_s and R_d is the total parasitic resistance that is calculated by using the extraction method. R_g is very small and it can be ignored because it is almost floating gate. Also, R_b can be ignored because the multi-finger MOSFET is fabricated in a common-source configuration.

In Fig. 2, as the total gate width is increased, the parasitic resistance is reduced as the parasitic resistance is related to the operating current of the MOSFET. Here, equation of the parasitic resistance can be extracted, so it will be described as:

$$R_{parasitic}\, \alpha\, \frac{L}{W}\frac{1}{\mu C_i (V_G - V_T)} \tag{2}$$

As a result of Eq. (2), the parasitic resistance is proportional to gate length, and is inversely proportional to gate width [4]. Both the gate width and the number of fingers change the total gate width, so it comes out with the same results.

Threshold voltage is one of the most important characteristics of the MOSFETs. This paper extracted V_{th} from the transfer characteristic curve. The results of the extracted V_{th} are shown in Fig. 3.

From the results, the size of the MOSFET is reduced and the V_{th} decreases. In Fig. 3(a), both the number of fingers and gate width are reduced and V_{th} decreased gradually. It indicates that the variations of the gate width and the number of fingers have the same effects on V_{th}.

However, the variations in drain voltage affect V_{th} along with the change of the gate length. In Fig. 3(b), this reduction of V_{th} with a scaled down length is defined as the V_{th} roll-off since the

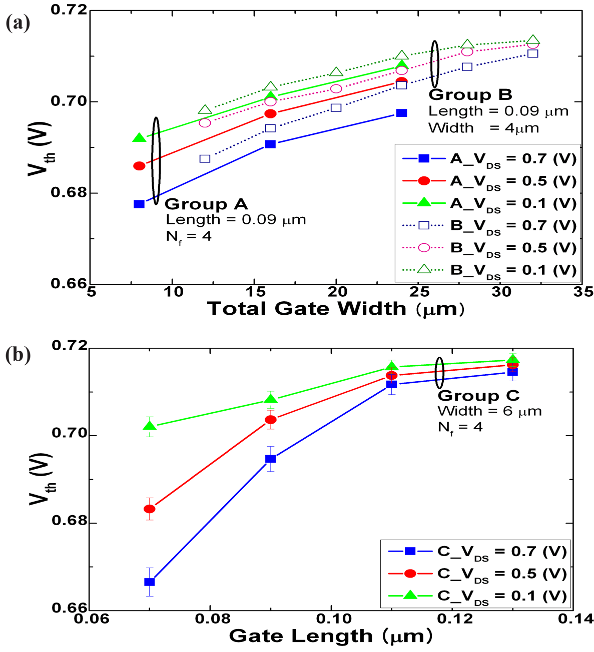

Fig. 3. V_{th} variations: (a) total gate width and (b) gate length variation.

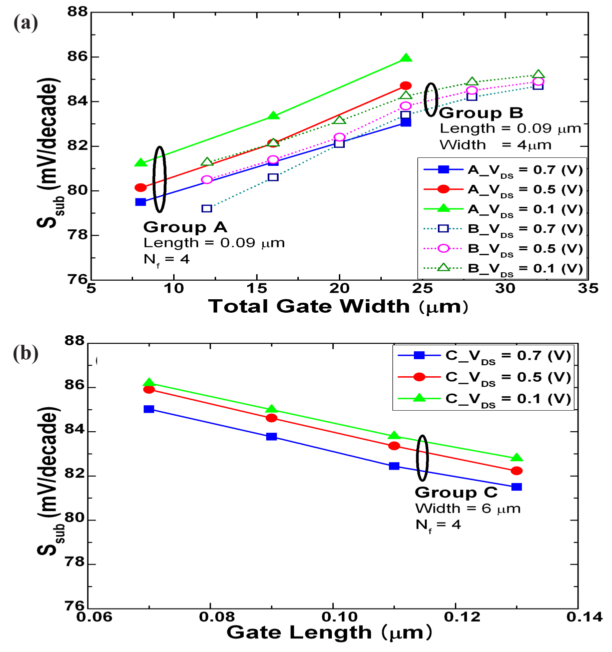

Fig. 5. S_{sub} variations: (a) total gate width and (b) gate length variation.

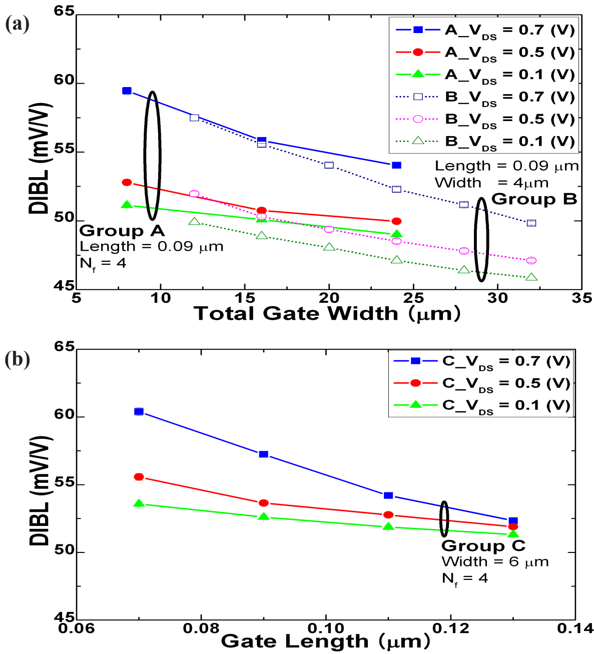

Fig. 4. DIBL variations: (a) total gate width and (b) gate length variation.

short channel effect occurs [5]. The fields of source and drain influence the channel, and as the dimension of the MOSFET decrease, the V_{th} roll-off phenomenon occurs on a large scale. Thus, it greatly affects the short channel on the potential profile [5]. In addition, the DIBL effect can also cause significant V_{th} roll-off.

The results of the calculated DIBL of the multi-finger MOSFETs are presented in Fig. 4. In this paper, DIBL is calculated as ΔV_G over ΔV_D, where $V_D = 1.2$ V and V_G is $I_D = 0.1$ μA/μm [6].

As mentioned, DIBL is one of the major reasons for V_{th} roll-off [5]. When a large drain voltage is applied, the DIBL is increased because the barrier is reduced between the drain and the source. DIBL can increase the drain current and it is proportional to the applied drain voltage, thus DIBL is sensitive to drive voltage. As the size of the total gate width is increased, the dimensions of MOSFETs are increased and the DIBL is decreased in all three groups. The gap between the source and the drain is also increased. Thus, a large dimension prevents the drain field from penetrating the channel. It also prevents the potential barrier lowering [7]. The reduction of the DIBL in group B is much larger than group A because the dimension increment of group B is larger than that of group A. So, group B is less affected by short channel effects. In Fig. 4(a), the DIBL of group B also rapidly decreased compared with group A. Figure 4(b) shows that the dimension variation due to the change in length affects the DIBL. As a result, it has a high immunity about DIBL effect to use many fingers as the group B.

S_{sub} variation results are shown in Fig. 5. In general, S_{sub} is proportional to the total gate width and is inversely proportional to gate length. The following Eq. (3) expresses the S_{sub}:

$$S_{sub} = \frac{dV_G}{d(\log_{10} I_D)} = In10\frac{kT}{q}(1+\frac{C_{dm}}{C_{ox}}) \approx 60(1+\frac{C_{dm}}{C_{ox}}) \quad (3)$$

In Fig. 5(a), the S_{sub} is gradually raised by increasing the total gate width. The depletion region and the value of the depletion capacitance (C_{dm}), which is a crucial factor for S_{sub}, are taken into account for analyzing the S_{sub}. From these results, if both the number of fingers and gate width are increased, the C_{dm} becomes large. As the depletion region is increased, the C_{dm} is also increased. However, S_{sub} of group B is larger than that of group A because the variation of C_{dm} through the change of the number of fingers is larger than that of change of the gate width.

In contrast, the S_{sub} decreases when increasing the gate length as shown in Fig. 5(b). Since the dimension of the MOSFET grows very large, the full depletion region is decreased, and the result is C_{dm} reduction [8].

The g_m is the ratio of the drain current changes to the gate voltage changes. In this paper, g_m is defined as the maximum value

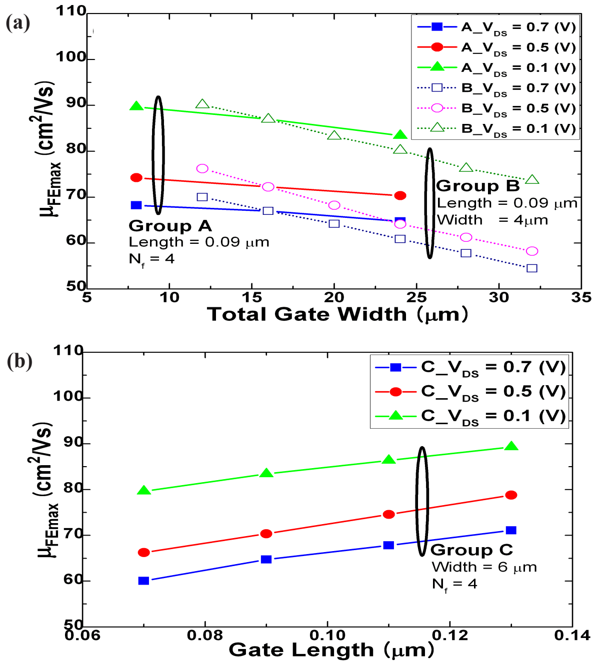

Fig. 6. μ_{FEmax} variations: (a) total gate width and (b) gate length variation.

of the differential transfer curve. The μ_{FEmax} is proportional to g_m, so μ_{FEmax} can be calculated from the following equation:

$$\mu_{FE\max} = g_m / (W / L) C_i V_{DS} \quad (4)$$

where C_i is gate capacitance per unit area. Figure 6 shows the calculated μ_{FEmax} of the multi-finger MOSFETs.

In general, if the total gate width is increased, the g_m is increased. The g_m is related to the flow drain current and the current is increased when the gate width is increased, which makes g_m large.

However, in Fig. 6(a), the μ_{FEmax} is slightly decreased as the total gate width is decreased. The reason for this is that the size of the multi-finger MOSFETs has larger effects on the mobility than the transconductance. Also, the slopes of μ_{FEmax} of group B are larger than those of group A because the dimension variation of group B becomes larger than that of group A.

Conversely, for group C in Fig. 6(b), the three slopes of μ_{FEmax} are almost the same, which is a different trend than group A and B because the gate length variation of group C comes to change on a large scale, so it has dominant effects on the μ_{FEmax}.

4. CONCLUSIONS

The geometric variation effects depending on the drain voltage of the multi-finger MOSFETs were investigated in this paper. The electrical characteristics of multi-finger MOSFETs were extracted from the proposed model and used for variation analysis. The electrical properties, such as V_{th}, DIBL, S_{sub}, g_m, and μ_{FEmax}, were analyzed depending on the drain voltage and gate structure variation. Thus, this modeling methodology allows us to provide the design guidelines for the gate geometric structure of the multi-finger MOSFET depending on the driving voltage for memory applications.

ACKNOWLEDGMENTS

This research was supported by the HYNIX Semiconductor Inc. and TCAD tool was supported under the IC Design Education Center.

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