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GHz EMI Characteristics of 3D Stacked Chip PDN with Through Silicon Via (TSV) Connections

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Abstract

GHz electromagnetic interference (EMI) characteristics are analyzed for a 3dimensional (3D) stacked chip power distribution network (PDN) with through silicon via (TSV) connections. The EMI problem is mostly raised by P/G (power/ground) noise due to high switching current magnitudes and high PDN impedances. The 3D stacked chip PDN is decomposed into P/G TSVs and vertically stacked capacitive chip PDNs. The TSV inductances combine with the chip PDN capacitances produce resonances and increase the PDN impedance level in the GHz frequency range. These effects depend on stacking configurations and P/G TSV designs and are analyzed using the P/G TSV model and chip PDN model. When a small size chip PDN and a large size chip PDN are stacked, the small one's impedance is more seriously affected by TSV effects and shows higher levels. As a P/G TSV location is moved to a corner of the chip PDNs, larger PDN impedances appear. When P/G TSV numbers are enlarged, the TSV effects push the resonances to a higher frequency range. As a small size chip PDN is located closer to the center of a large size chip PDN, the TSV effects are enhanced.

Key words: GHz EMI, 3D, Chip-PDN, 3D IC, TSV, Stacking Configuration.

Ⅰ. Introduction

Currently developed systems are demanding chip packages with higher performance and integration. Therefore, 3D (3-Dimensional) stacked chip structure is becoming an essential technology for many chip, package, and system companies. The 3D stacked chip technologies such as bond wire, flip chip, and through silicon via (TSV) provide various flexible functional combinations to a single chip package allowing short electrical delay paths between chips and small package sizes [1]~[4]. Among the 3D stacked chip technologies, TSV is the most interesting technology because it can provide very large numbers of inter-chip interconnections, very small parasitic inductance, and short electrical delays between chips, as well enabling relatively high chip density design. However, the increased power consumption per unit area must be considered in a 3D stacked on-chip PDN because total power consumption is proportional to increased current magnitudes through TSVs and EMI (electromagnetic interference) is increased by high current switching and high PDN impedances. Of course, TSV shows very small inductance, which is very helpful to 3D IC by giving lower PDN impedance [5]. However, when it combined with the large capacitance of a chip-PDN, it can induce high PDN impedances, which are called as TSV effects or TSV inductance effects and can be an EMI source in the GHz range as shown in [6]. In addition, since 3D IC is being developed for combining various functional chips and various size chips, TSV ef-

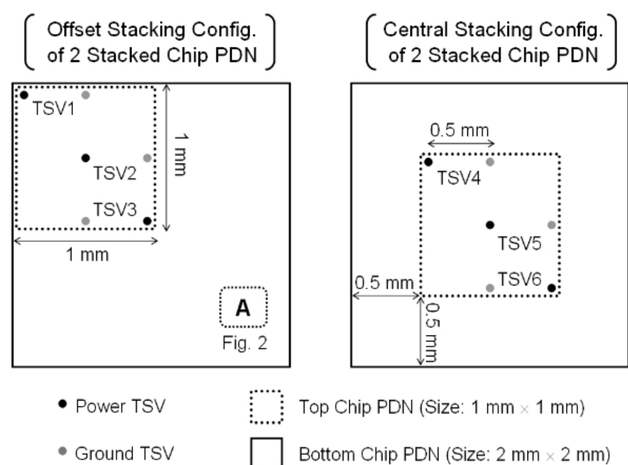

Fig. 1. Stacking configurations and P/G TSV design of 3D stacked chip PDN with two different size chip PDNs.

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fects that depend on stacking configurations and the P/G TSV designs of 3D stacked chip PDN should be considered and analyzed. In this paper, those are analyzed using the P/G TSV model and the multi-TSV model proposed in [7], [8].

Ⅱ. Stacking Configurations & P/G TSV Designs

As shown in Fig. 1, two stacking configurations are considered. One is an 'Offset Stacking Configuration'; i.e., 'Offset Config.', and the other is a 'Central Stacking Configuration'; i.e., 'Central Config.' Each configuration has two different-sized chip PDNs. A small size chip PDN (the dotted line rectangle; i.e., 'Top Chip PDN') is stacked onto the large size chip PDN (the solid line rectangle; i.e., 'Bottom Chip PDN'). The sizes of the small and large chip PDNs are 1 mm by 1 mm and 2 mm by 2 mm, respectively. In the Offset Config., the Top Chip PDN is stacked onto the Bottom Chip PDN with corner-to-corner alignment, while the Central Config. is aligned with center-to-center alignment. All four chip PDNs are designed as meshed type chip PDNs on 2 metal layers, as shown in Fig. 2, which is a zoomed-in figure of 'A', the dotted line area in Fig. 1.

As shown in Fig. 2, the metal lines with 10 μm line width are assumed in the analyses to be repeated vertically on metal layer 1 and horizontally on metal layer 2 with 100 μm line pitch. Power and ground electrical properties are assigned one by one in vertical and horizontal directions as shown in conventional chip PDN designs. No resistance is also assumed at cross points of two vertical and horizontal lines if the two lines have the same electrical property (power or ground); where many micro-vias connect two different metal layers and very small resistance appears.

Each configuration has three P/G TSV pairs, designed TSV1, TSV2, and TSV3 for Offset Config. and TSV4, TSV5, and TSV6 for Central Config. Each P/G TSV pair has 0.5 mm pitch and consequently a reasonable assumption is that the the mutual effect between them is negligible [8].

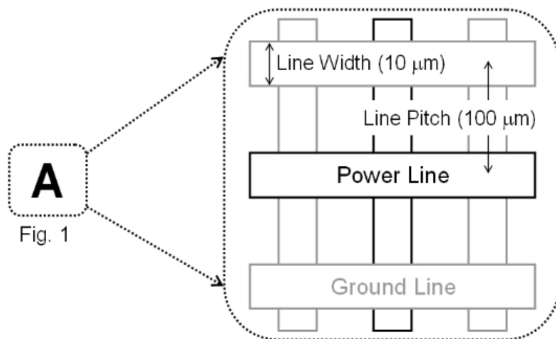

Fig. 2. Chip PDN design of four chip PDNs of Fig. 1.

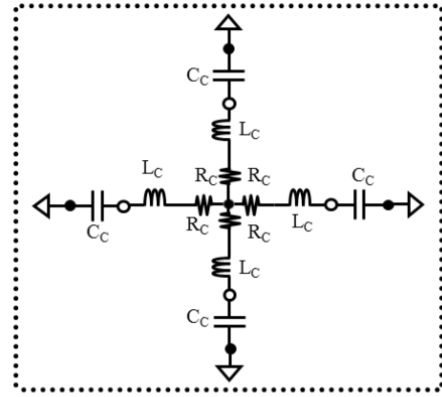

Fig. 3. Spice model of Fig. 2 for chip PDN simulations.

Two stacking configurations are simulated with the proposed chip PDN models, which are composed of multi-connecting unit chip PDN models of Fig. 3. Since all chip PDNs are assumed to have meshed type, they can be modeled by vertically and horizontally repetitions and connections of unit chip PDNs (small circles of four legs are connection nodes).

The unit chip PDN model has a spice type and its lumped elements are defined by the following equations, based on chip PDN dimensions.

$$R_c = \frac{LP}{2 \cdot \sigma_{AI} \cdot T \cdot LW}$$

$$L_c = \frac{\mu_0 \cdot LP}{2 \cdot 2\pi} \cdot \left[(\text{In}\left(\frac{(\text{LP}-\text{LW}/4)^2}{2 \cdot \text{LP} \cdot (\text{T}+\text{LW})} \right) + 1 \right]$$

$$C_c = C_{OV} + 2 \cdot C_{TT}$$

$$C_{OV} = \frac{\epsilon_{r_{INS}} \cdot \epsilon_0 \cdot LW \cdot T}{INS}$$

$$C_{TT} = \frac{3 \cdot \epsilon_{r_{INS}} \cdot \epsilon_0 \cdot LW}{INS} + T$$

where σ_{Al} is the conductivity of aluminum (3.8×10^8 S/m), LW and LP are Line Width and Line Pitch of Fig. 2, T is the thickness of metal layer (T=0.5 μm), ε_{rINS} and INS are the relative dielectric constant and the thickness of the insulator between two metal layers, C_{OV} is the overlap capacitance between two lines of metal 2 and 1, and C_{TT} is the fringe top-to-top capacitance from metal 2 to metal 1 lines. μ_0 and ε_0 are permeability and permittivity of free-space, each value being $4\pi \times 10^{-7}$ H/m and 8.854×10^{-12} F/m, respectively.

In Fig. 4, the proposed chip PDN model gives a good estimate of the measured chip PDN impedances, which come from 1 mm×1 mm size chip PDN made by Hynix Semiconductor Inc.'s memory technology. Since the chip

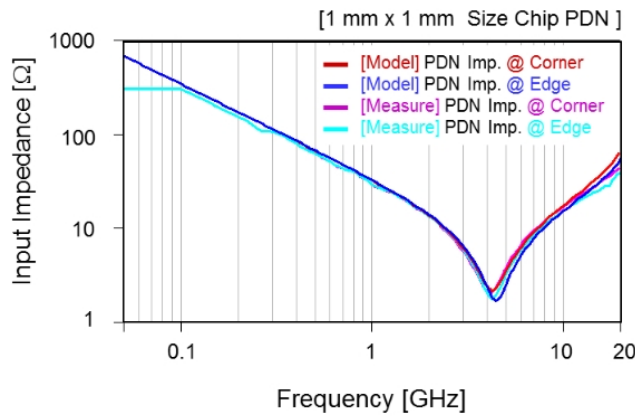

Fig. 4. Comparison of chip PDN impedances between the proposed model and measurement results.

PDN is small, its low frequency response shows capacitive impedance, whereas inductive impedance appears in the high frequency range over 4 GHz. If the chip PDN size increases, its capacitance also increases and capacitive impedance level decreases, whereas its inductance decreases due to its longer line length, decreasing the inductive impedance level. Consequently, its series resonance frequency, which appears as an under peak around 4.5 GHz in Fig. 4, moves to a lower frequency range.

A vertical cross sectional view of two stacking configurations including TSV is shown in Fig. 5. The Top Chip is stacked on the Bottom Chip, and the two chip PDNs have two metal layers and are connected by TSVs. It is considered that a TSV has 30 μm diameter, 100 μm length, and a 0.5 μm SiO_2 (grey colored area) TSV insulator thickness is present between TSV and Si (silicon) substrate during the analyses.

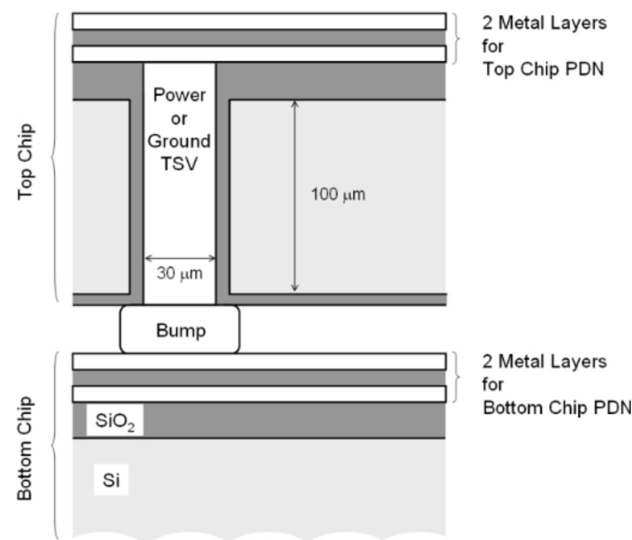

Fig. 5. Vertical cross sectional view of two stacking configurations and TSV.

Ⅲ. GHZ EMI Characteristics of 3D Stacked Chip PDN; TSV Effect on 3D Stacked Chip PDN

As mentioned in this chapter title and [8], the GHz EMI characteristics of a 3D stacked chip PDN are high PDN impedances caused by TSV interconnections between high capacitive chip PDNs. Therefore, 3D stacked chip PDN impedances should be analyzed whenever stacking configurations and TSV designs are changed. (Fig. 1) Since these two configurations have two stacked chip PDNs, the PDN impedances show a single high peaks over GHz frequency range as mentioned in [8]. All PDN impedances of chip PDN and 3D stacked chip PDN with TSV connections have been obtained by using the P/G TSV model and the P/G multi-TSV model proposed by the authors in [7], [8], applied to the typical dimensions of DRAM memory and TSV technologies.

3-1 Chip PDN Impedances of Non-Stacked Condition

First of all, chip PDN impedances of non-stacked condition are analyzed, as shown in Fig. 6. This analysis must be performed accurately because the 3D stacked chip PDN is a combination of non-stacked chip PDNs. The PDN impedances are calculated at four locations, as follows: Z_{T_Corner}; left-bottom corner of Top Chip PDN, Z_{T_Center}; center of Top Chip PDN, Z_{B_Corner}; left-bottom corner of Bottom Chip PDN, and Z_{B_Center}; and left-bottom corner of Bottom Chip PDN, as depicted in Fig. 6.

As the chip PDN size is increased, its capacitance and inductance increase because the overall overlap area between power and ground metals, as well as the line lengths, is increased. As the PDN calculation location gets closer to the center, inductance decreases because current flow paths are wider around the center than at the corners-and wider current paths exhibit lower inductance. These tendencies are very similar to those of PDNs of PCB and packages. These current path effects can be adopted in analyzing chip PDN resistance, which controls the PDN impedance level or Q-factor at resonance

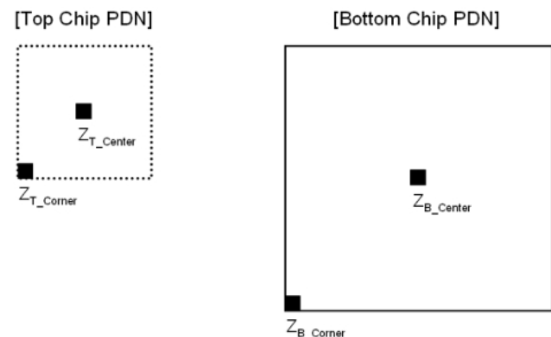

Fig. 6. Four PDN impedance calculation locations.

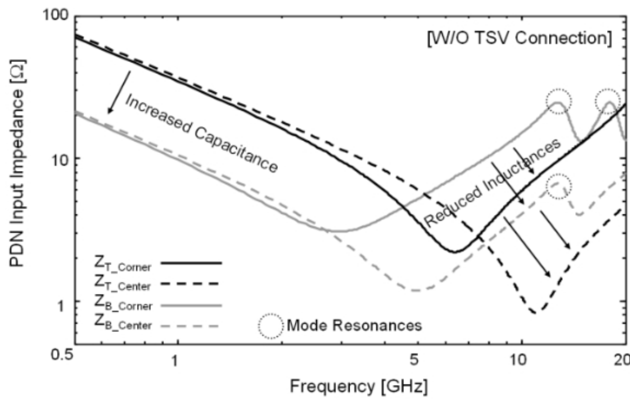

Fig. 7. Non-stacking chip PDN impedance variation depending on chip PDN sizes (Fig. 1) and impedance calculation locations (Fig. 6).

frequency. A smaller chip PDN shows larger Q-factor, which can be verified with sharper resonance peaks in Fig. 7.

The dotted line circles indicates mode resonances such as (1, 0) / (0, 1) and (1, 1) modes caused by 2 mm chip PDN length as shown in cavity resonances of PCB and package PDNs. The Top Chip PDN has no mode resonance due to the shorter length of 1 mm and the limited plot range of frequency scale (up to 20 GHz) in Fig. 7. However, because of the meshed type chip PDN with different line widths and pitches, and consequently different phase velocities in vertical and horizontal directions, even the same size chip PDN as those shown in Figs. 1 and 6 do not always guarantee the same resonance phenomena, as shown in Fig. 7.

For example, when line width becomes narrower, the overlapping area between two lines on two metal layers decreases, resulting in smaller capacitance (C_C) and increased inductance of line (L_C) based on equations and the narrow current path. However, since C_C is directly proportional to the line width, whereas L_C only has a logarithmic relationship to the line width, C_C more strongly affects the phase velocity on the chip PDN, increasing the delay, and consequently moving the mode resonance frequencies to lower frequency range. Therefore, same size chip PDN with different line designs results in different chip PDN impedance, as mentioned before.

3-2 Offset Stacking Configuration

Fig. 8 shows four PDN impedances of Offset Config., measured at the four impedance calculation locations (Fig. 6), when only TSV1 is used for vertical connection. The higher PDN impedances appear at the Top Chip PDN (Smaller chip PDN) compared to the Bottom Chip

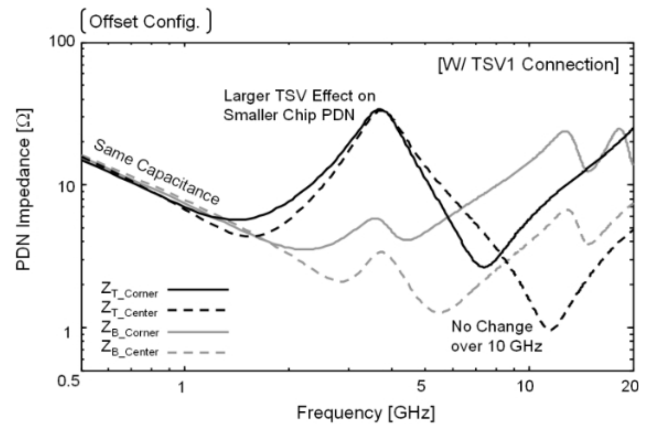

Fig. 8. Chip PDN impedance variation of Offset Stacking Configuration depending on impedance measurement locations (Fig. 7) when only TSV1 connects two chip PDNs.

PDN because smaller chip PDN shows smaller resistance and has larger Q-factor and consequent higher PDN impedance level at 4 GHz resonance. The PDN impedances over 6 GHz still remain the same, as shown in Fig. 7, because TSVs cannot give electrical paths between two stacked chip PDNs due to the high impedance of TSV inductance in the high frequency range.

Consequently, a larger TSV effect is induced on smaller chip PDN when two different-sized chip PDNs are stacked with a TSV. Therefore, we should pay more attention to smaller size chip PDN designs when selecting TSV numbers and stacking locations, so that they are closer to larger decoupling capacitors on packages and PCBs.

Fig. 9 shows how PDN impedances variation depending on P/G TSV locations, such as from corner to center. As the TSVs move closer to the center, the chip PDN in-

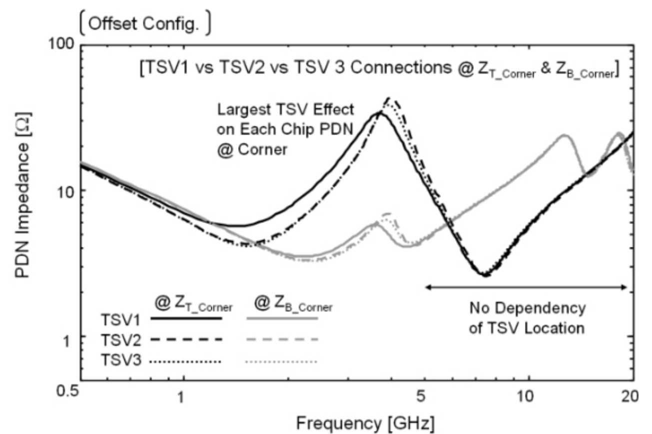

Fig. 9. Comparison of chip PDN impedances of Offset Stacking Configuration depending on TSV locations (Fig. 1) and impedance calculation locations (Fig. 6).

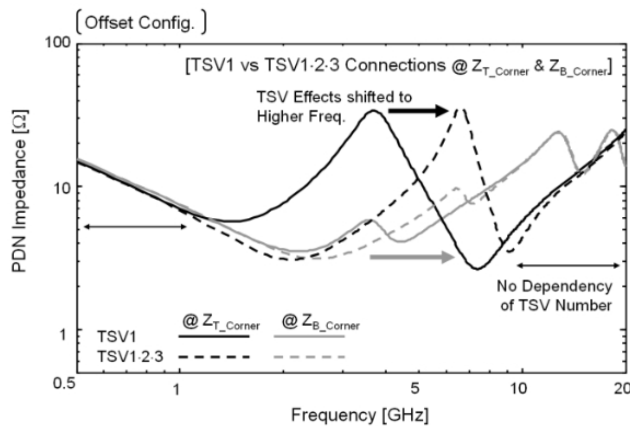

Fig. 10. PDN impedance variations of Offset Config. depending on numbers of P/G TSV pairs.

ductance and resistance at each location are reduced and consequently the resonance frequencies move to higher frequency also PDN impedance peak values go up. Therefore, higher frequency application of TSVs, the location at which the TSVs are connected should be carefully considered. Usually, critical harmonic frequencies of simultaneous switching noise (SSN), which is a critical design issue in PDN design, appear at PDN impedance peak frequencies, coinciding with the resonance frequencies of the PDN.

The resonances due to TSV effect can arise from the combination of serially connected TSVs and chip PDN inductances and chip PDN capacitance. If on-chip decoupling capacitors are added to a chip PDN, the resonances move down to lower frequency ranges where EMI problems should be more carefully treated due to larger level spectrum density.

When the number of P/G TSV pairs increases from TSV1 to TSV1, TSV2, and TSV3 (= TSV1 · 2 · 3) or from one pair P/G TSV connection to three pairs, the resonance frequencies move to a higher frequency because TSV effective inductance decreases due to parallelism, as shown in Fig. 10.

3-3 Central Stacking Configuration

In this section, Central Config. is considered. As shown in Fig. 11, PDN impedances are different from those in Figs. 9 and 10 because the Top Chip PDN is stacked on the low impedance area of the Bottom Chip PDN: the center location as explained in section III-1. On the top PDN, TSV4 and TSV5 are located at exactly the same points as TSV1 and TSV2, respectively. Nevertheless, since TSVs are located at different points on the Bottom Chip PDN, different values of chip PDN inductance are obtained due to TSV effect and the PDN impedances show the discrepancies.

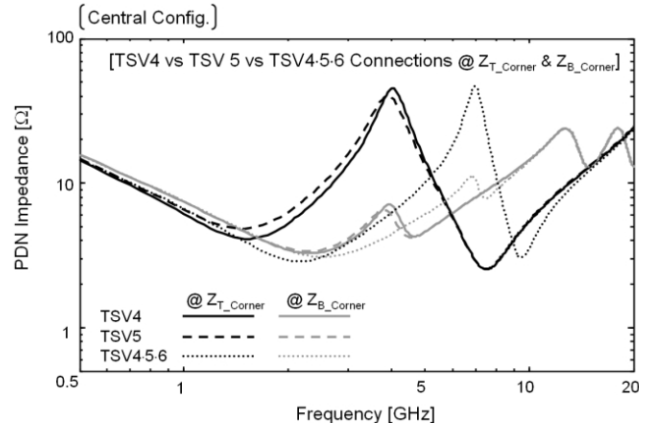

Fig. 11. PDN impedance variations of Central Config. depending on TSV locations and numbers of P/G TSV pairs.

The PDN impedance variation of Central Config. is almost same as that of Offset Config. including TSV location and number effect on high PDN impedance level due to resonances.

To know the discrepancy between the PDN impedances of Offset and Central Configs. in detail, Fig. 12 compares four cases; TSV1, TSV4, TSV1 · 2 · 3, and TSV 4 · 5 · 6. Offset Config. shows the larger TSV effects (thick solid arrows) than does Central Config. by showing the larger chip PDN impedance levels because of the lower PDN impedance of Bottom Chip PDN. On the other hand, in the frequency range without resonances, Offset Config. shows higher levels since chip PDN impedance is dominant in this range. Nevertheless, since the EMI problem due to power switching noise occurs when signal and clock harmonic frequencies coincide with resonance frequencies, lower PDN impedance levels at resonance frequencies are more important when designing a chip PDN and even a 3D stacked chip PDN.

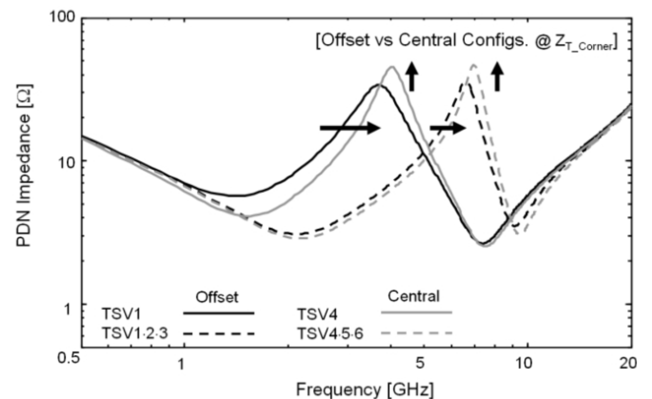

Fig. 12. Comparison of Offset and Central Configs. in a view point of PDN impedances at the corner location of Top Chip PDN.

Ⅵ. Conclusion

GHz EMI generator or high PDN impedances in GHz frequency range or TSV effect in 3D stacked chip PDN with TSV connections have been analyzed by considering the two different size chip PDNs, two different stacking configurations, seven different TSV designs. The variations of 3D stacked chip PDN impedance come from TSV inductance, and chip PDN inductance and resistance depending on 3D stacked chip PDN designs. The 3D stacked chip PDNs are analyzed using the P/G TSV model and the P/G multi-TSV model in [7], [8]. When small size chip PDNs and large size chip PDNs are vertically stacked with P/G TSV pair connections, the small one is more severely affected by P/G TSV pairs and shows a larger PDN impedance in the GHz frequency range than does the larger one. When a stacking configuration is fixed and TSV location is moved to a corner on the chip PDNs, larger PDN impedance appears. When P/G TSV numbers are enlarged, the TSV effects move to the higher frequency range. As a small size chip PDN is closer to the center of a large size chip PDN, TSV effects are enlarged.

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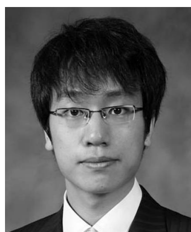

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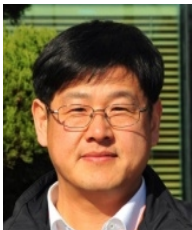

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