http://dx.doi.org/10.6109/ijice.2011.9.6.738

Analysis on DIBL of DGMOSFET for Device Parameters

Hak-Kee Jung, *Member, KIICE*

***Abstract*— This paper has studied drain induced barrier lowering(DIBL) for Double Gate MOSFET(DGMOSFET) using analytical potential model. Two dimensional analytical potential model has been presented for symmetrical DGMOSFETs with process parameters. DIBL is very important short channel effects(SCEs) for nano structures since drain voltage has influenced on source potential distribution due to reduction of channel length. DIBL has to be small with decrease of channel length, but it increases with decrease of channel length due to SCEs. This potential model is used to obtain the change of DIBL for DGMOSFET correlated to channel doping profiles. Also device parameters including channel length, channel thickness, gate oxide thickness and doping intensity have been used to analyze DIBL.**

***Index Terms*— DGMOSFETs, DIBL, digital devices, transport model, device parameter**

I. INTRODUCTION

THE downscaling to the sub-10nm range can be implemented in the structure of the double gate(DG) MOSFETs. In the International Technology Roadmap for Semiconductors 2007(ITRS) for the DGMOSFET, the physical channel length is 4.5nm for the year 2022[1]. With DGMOSFET short channel effects(SCEs) lessened dramatically and current controllability of gate electrodes becomes nearly twice. The SCEs have been occurred with scaled down transistor, and the kinds of SCEs are threshold voltage roll-off, subthreshold swing degradation, and drain induced barrier lowering(DIBL) and the like[2]. The single gate conventional CMOS in planar technology is yet dominant in the semiconductor market and industry. However, with scaling down device dimension, short channel effects(SCEs) considerably increase in the conventional MOSFET, at last we could not use planar conventional CMOS any more in the sub-10nm region. Many research has been done to solve these problems, and DGMOSFETs, FinFET and surrounding gate MOSFET have been studied as candidate and investigated to improve gate controllability and to reduce SCEs[3]. The DGMOSFET could overcome SCEs and control effectively currents.

The DIBL in SCEs is that drain biased voltage influences on barrier height of source with shrink of channel length. The channel charge and current are partially controlled by drain biased voltage rather than gate voltage due to the DIBL effect. In order to solve this problem, various researches have been done such as doping profile control, gate workfunction engineering, and multiple gate device[4]. A fully analytical model for potential distribution of DGMOSFET is derived in details from Poisson's equation to investigate SCEs with various structure and process parameters[5][6]. But they don't investigate DIBL in details even though their potential model is validated with results of 2D simulation. So to study DIBL in DGMOSFET, this study uses nonuniform channel doping profile with Gaussian distribution to solve Poisson's equation. Since scaled down may lead to such obstacles as nonuniform carrier distribution and serious theoretical modeling, subthreshold characteristics have to be analyzed in the condition of nonuniform channel doping profile. This study has investigated the DIBL when channel doping profile is Gaussian distribution. Since the Gaussian distribution is general doping profile, this study uses this distribution to solve Poisson's equation, and explains Tiwari's potential model[6]. Using this model, we obtain the DIBL and explain the dependence of DIBL according to the channel thickness, gate oxide thickness and channel length for various channel doping profiles.

This paper is organized in four major sections. A 2D analytical potential and DIBL models with Poisson's equation are explained in Sec. II. In Sec. III, this study discusses potential distributions and DIBL to be derived from this model and validates with results of 2D simulator. The conclusion has been drawn in Sec. IV.

II. POTENTIAL AND DIBL MODEL

Figure 1 is the schematic diagram of a symmetric DGMOSFET, where L_g, t_{si}, t_{ox} are channel length, channel thickness and gate oxide thickness, respectively. As shown in Fig. 1, $x-$ and $y-$ directions are considered to be along channel thickness and channel length. The 2D Poisson's equation to solve potential

Manuscript received September 15, 2011; revised October 24, 2011; accepted November 1, 2011.

Hak-Kee Jung is with the Department of Electronic Engineering, Kunsan National University, Kunsan, 573-701, Korea (Email: hkjung@kunsan.ac.kr)

$\varphi(x,y)$ is

$$\frac{\partial^2\varphi(x,y)}{\partial x^2}+\frac{\partial^2\varphi(x,y)}{\partial y^2}=\frac{qn(x)}{\varepsilon_{si}} \tag{1}$$

where ε_{si} is permittivity of silicon.

Ion implantation has been generally used for impurity doping in semiconductor, and total distance that an ion travel to rest is called its range R .The projection of this distance along the axis of incidence is called the projected range R_p . The statistical fluctuations in the projected range are called the standard projected deviation σ_p . Along the axis of incidence implanted impurity profile can be approximated by Gaussian distribution function:

$$n(x)=\frac{S}{\sqrt{2}\pi\sigma_p}\exp\left[-\frac{(x-R_p)^2}{2\sigma_p{}^2}\right] \tag{2}$$

where S is the ion dose per unit area and $s/\sqrt{2}\pi\sigma_p$ is constant N_p .

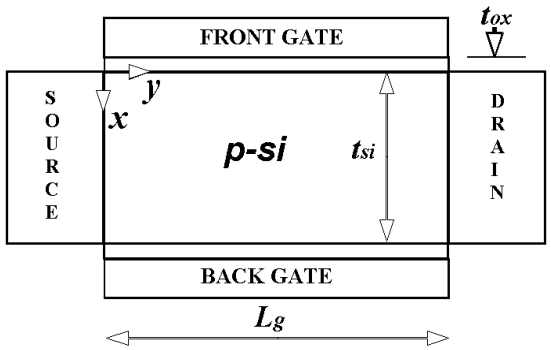


Fig. 1. The schematic diagram of a symmetric DGMOSFET

Using the methods proposed by Zhang et al[4] and Tiwari et al[5], Eq. (1) can be modified as

$$\frac{\partial^2\varphi_s}{\partial y^2}+\frac{V_G-V_{fb}-\varphi_s}{\lambda^2}=\frac{qN_p}{\varepsilon_{si}}\exp\left(-B^2\right) \tag{3}$$

where φ_s is surface potential, ε_{Si} is the permittivity of silicon, V_{fb} is flat-band voltage, V_G is biased voltage, and λ is the following as the characteristic length related with surface potential

$$\lambda^2=\sqrt{\pi}\sigma_p{}^2\left\{\frac{DB-E-Berf(B)-\exp(-B^2)/\sqrt{\pi}}{\exp(-B^2)}\right\} \tag{4}$$

The erf is error-function, and refer the previous paper[7] for B,D,E . Eq. (3) is solved to obtain surface potential φ_s . The surface potential is

$$\varphi_s=F\exp(y/\lambda)+G\exp(-y/\lambda)+V_G-V_{fb}-\lambda^2qN_p\exp(-B^2)/\varepsilon_{si} \tag{5}$$

Refer the previous paper[7] for F,G . Note that $\varphi_s=\varphi_s(y_{\min})$ represents the minimum of $\varphi_s(y)$. The $y_{\min}$ can be derived from $d\phi_s(y)/dy\big|_{y=y_{\min}}=0$ as the followings.

$$y_{\min}=\frac{\lambda}{2}\ln(G/F) \tag{6}$$

Using Eqs. (5) and (6), minimum surface potential can be derived as

$$\varphi_{s\min}=2\sqrt{FG}+V_G-V_{fb}-\lambda^2qN_p\exp(-B^2)/\varepsilon_{si} \tag{7}$$

The threshold voltage V_{th} is derived from definition such that surface potential is twice of Fermi potential φ_f when gate voltage is threshold voltage. By definition, since surface potential is $2\varphi_f$ at $V_G=V_{th}$, the V_{th} can be obtained using quadratic formula as following [5];

$$V_{th}=\frac{R-\left\{R^2-4(4HK-1)\times(4NP-S^2)\right\}^{1/2}}{8HK-2} \tag{8}$$

$$S=V_{fb}+2\phi_f+\lambda^2qN_p\exp(-B^2)/\varepsilon_{si}$$

$$R=2S-4(HP+KN)$$

Refer the previous paper[7] for H,K,N,P,S .

The DIBL represents threshold voltage dependence on drain voltage, and causes the threshold voltage to be a function of operating voltage. Using Eq. (8), we obtained DIBL according to structure and process parameters as the followings ;

$$DIBL=V_{th}(0)-V_{th}(1) \tag{9}$$

where $V_{th}(1)$ is the threshold voltage at $V_D=1V$, and $V_{th}(0)$ is the threshold voltage at $V_D=0V$.

III. RESULTS OF POTENTIAL DISTRIBUTION AND DIBL

Figure 2 shows the variation of the surface potential φ_s along the channel length with $L_g=65nm$, $t_{si}=20nm$, $t_{ox}=1.5nm$, $V_{bi}=0.868V$, $V_{fb}=-0.26V$. The parameters of the Gaussian function are $R_p=10nm$,

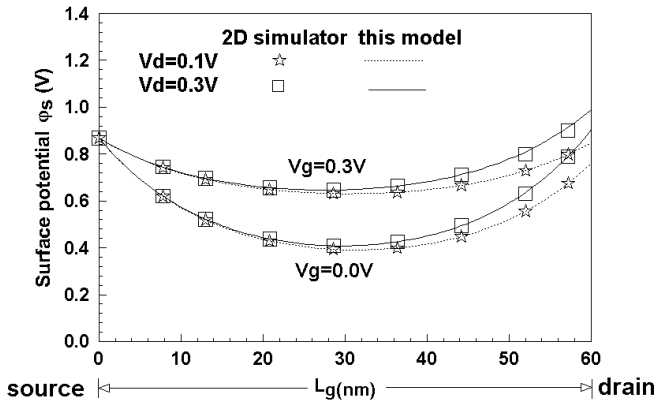


Fig. 2. Surface potential from source to drain with Gaussian doping profile having $R_p = 10nm$, $\sigma_p = 5nm$, and $N_p = 10^{15}/cm^3$.

$\sigma_p = 5nm$, and $N_p = 10^{15}/cm^3$. Using various gate voltages and drain voltages, these results have been compared with those of 2D simulator indicated with stars and squares. Note these results are good agreements with those of 2D simulator[6]. Minimun potential value has directed to source with the increase of gate voltage, and surface potential is increasing with the increase of drain voltage. The variation of minimum surface potential with drain voltage causes the change of threshold voltage, eventually DIBL. We have used, therefore, this potential model to calculate DIBL for various doping profile and structure parameters. Note as V_D and V_G increases the minimum of surface potential is increasing, causing the significant reduction of channel barrier height.

Figure 3 shows DIBL derived from Equation (9) according to gate length with the parameter of channel thickness. The projected range is 10nm and standard deviation is 5nm. The doping parameter N_p is $10^{16}/cm^3$. With the increase of channel length DIBL is decreasing. Usually the DIBL is proportional to the channel thickness , and is inversely proportional to the gate length. As shown in Fig. 3, the DIBL is increasing with the increase of channel thickness even though proportion is not linear. The influence of channel thickness on DIBL is increasing with the increase of channel length.

Due to influence of drain voltage on threshold voltage, even a smaller gate voltage is able to cause a strong inversion, resulting in a leakage and even a punch-through in some cases. Gate oxide thickness is very important factor to leakage current. Therefore, to explain the influence of gate oxide thickness on DIBL in details, the DIBL is calculated and plotted as a function of the channel length with the parameter of gate oxide thickness in Fig. 4. As shown in Fig. 4, the DIBL is increasing with the increase of gate oxide thickness even though proportion is not linear.

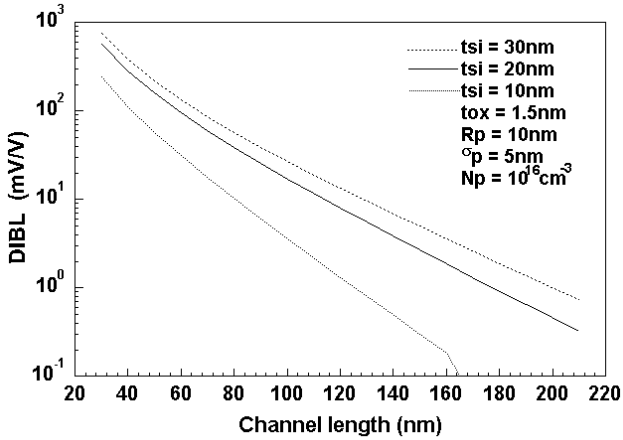


Fig. 3. DIBL according to gate length with the parameter of channel thickness. The projected range is 10nm and standard deviation is 5nm.

Note the influence of gate oxide thickness on DIBL is increasing with the increase of channel length.

To consider influence of channel doping concentration on DIBL, the DIBL is calculated and plotted as a function of the channel length with the parameter of channel doping concentration and channel thickness in Fig. 5. As shown in Fig. 5, the DIBL is decreasing with the increase of channel doping concentration. Even though channel thickness is smaller, the decreasing rate with the increase of doping concentration is nearly constant. The increase of doping concentration in channel causes the decrease of DIBL and subthreshold swing[8], but results in increase of impurity scattering and degradation of carrier transport. Therefore SCEs such as DIBL, subthreshold swing and threshold voltage are relation of trade-off for channel doping concentration.

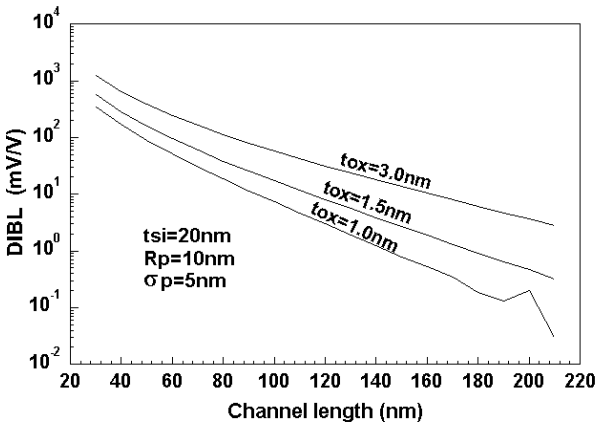


Fig. 4. DIBL according to gate length with the parameter of gate oxide thickness. The projected range is 10nm and standard deviation is 5nm.

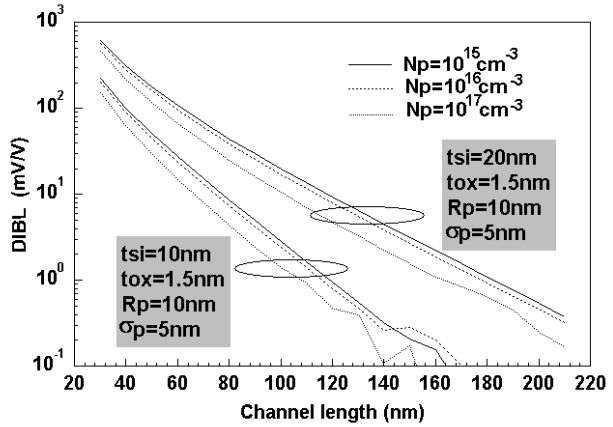


Fig. 5. DIBL as a function of gate length with the parameter of channel thickness and doping concentration. The projected range is 10nm and standard deviation is 5nm.

Figure 6 shows the SCEs such as DIBL, SS and threshold voltage roll-off have interrelations. DIBL and SS increase with increase of doping intensity, but threshold voltage decreases with increase of doping intensity. Since carriers transport ballistically through fully depleted channel of DGMOSFET, doping intensity must be low or channel intrinsic to lessen impurity scattering. If channel doping is low, SCEs such as DIBL and SS are too large, even though threshold voltage is low.

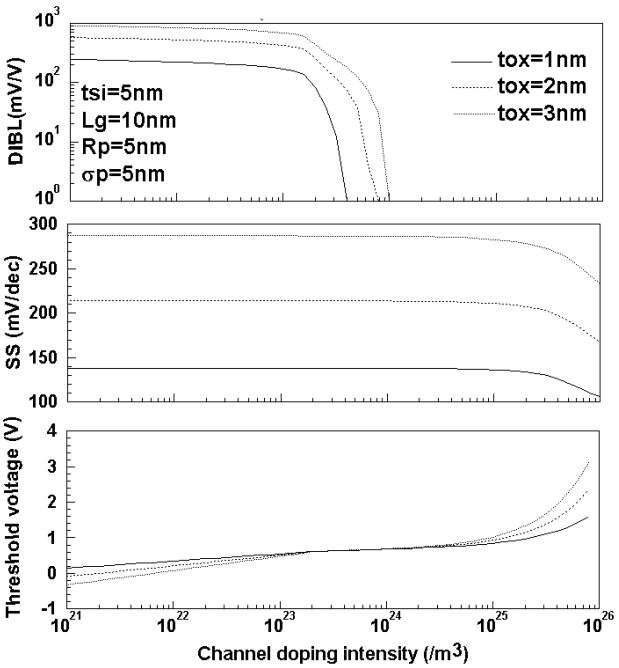


Fig. 6. DIBL, SS and threshold voltage as a function of doping intensity with the parameter of gate oxide thickness. The projected range is 5nm and standard deviation is 5nm.

If channel doping is high, device donot operate properly since threshold voltage is too large. Therefore precise control of doping intensity is needed to control SCEs.

IV. CONCLUSIONS

This study has presented DIBL for DGMOSFET using analytical potential model. Two dimensional analytical potential model has been presented for symmetrical DGMOSFETs with device parameters. DIBL is very important SCEs for nano structures since drain voltage has influenced on source potential distribution due to reduction of channel length. DIBL has to be small with decrease of channel length, but it increases with decrease of channel length due to SCEs. This study has obtained DIBLs as a function of channel length with a parameter of channel thickness, gate oxide thickness and doping concentration. Note DIBL is proportional to the channel thickness and gate oxide thickness, and is inversely proportional to the gate length. Also DIBL is decreasing with the increase of channel doping concentration. Since SCEs such as DIBL, SS and threshold voltage have trade-off relation for doping intensity, note controllability of doping intensity is very important for digital devices. These results should be used to design DGMOSFET for ideal subthreshold operation.

REFERENCES

[1] Technology Roadmap on Semiconductors, 2007 edition, Semiconductor Industry Association. URL: http://public.itrs.net.

[2] A.Kranti, T.M.Chung, D.Flandre and J.P.Raskin, “Analysis of quasi double gate method for performance prediction of deep submicron double gate SOI MOSFETs,” Semicond. Sci. Technol., vol.20, pp.423-429, 2005.

[3] F.Djeffal, M.A.Abdi, Z.Dibi, M.Chahdi and A.Benhaya, “A neutral approach to study the scaling capability of the undoped Double-Gate and cylindrical Gate All Arround MOSFETs,” Materials Sci. and Eng:B, vol.147, pp.239-244, 2008.

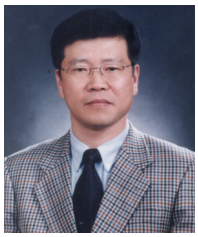
[4] A.Anwar and I.Hossain,”A Comparative Numerical Simulation of a Nanoscaled Body on Insulator FinFET,” Proc. 27th International Conference on Microelectronics(MIEL2010), pp.413-416, 2010.

[5] G.Zhang, Z.Shao and K.Zhou,”Threshold voltage model for short channel FD-SOI MOSFETs with vertical Gaussian profile,” IEEE Trans. Electron Devices, vol.55, pp.803-809, 2008.

[6] P.K.Tiwari,S.Kumar, S.Mittal, V.Srivastava, U.PandeyK and S.Jit,”A 2D Analytical Model of the Channel Potential and Threshold Voltage of Double-Gate(DG) MOSFETs With Vertical Gaussian Doping Profile,” IMPACT-2009,pp.52-55,2009.

[7] H.K.Jung, J.H.Han, J.I.Lee and S.Dimitrijev,”Analysis of DIBL for DGMOSFET Using Structure and Process Parameters,” Proc. of ICKIMICS2011, vol.4, no.1, pp.289-292,2011.

[8] Q.Chen, B.Agrawal and J.D.Meindl,”A Comprehensive Analytical Subthreshold Swing(S) Model for Double-Gate MOSFETs,” IEEE Trans. Electron Devices, vol.49, pp.1086-1090, 2002.



Hakkee Jung Received the B.S. degree from Ajou University in 1983, the M.S. and Ph.D degrees from Yonsei University in 1985 and 1990, respectively, all in electronic engineering. In 1990, he joined Kunsan National University, Chonbuk, Korea, where he is current a Professor in the School of Electronic and Information Engineering. From 1994 to 1995, he held a research position with the Electronic Engineering Department, Osaka University, Osaka, Japan. From 2004 to 2005, he was with the School of Microelectronic Engineering, Griffith University, Nathan, QLD, Australia. His research interests include semiconductor device physics and device modeling with a strong emphasis on quantum transport and Monte Carlo simulation.