A Study on Self Repairing for Fast Fault Recovery in Digital System by Mimicking Cell

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Abstract— **Living cells generate the cell cycle or apoptosis, depending on the course will be repeated. If an error occurs during this period of life in order to maintain the cells in the peripheral cells find the error portion. These cellular functions were applied to the system to simulate the circuit. Circuit implementation of the present study was constructed the redundant structure in order to found the error quickly.**

Self-repairing of digital systems as an advanced form of fault-tolerance has been increasingly receiving attention according as digital systems have been more and more complex and speed-up especially for urgent systems or those working on extreme environments such as deep sea and outer space. Simulating the process of cell differentiation algorithm was confirmed by the FPGA on the counter circuit. If an error occurs on the circuit where the error was quickly locate and repair.

In this paper, we propose a novel self-repair architecture for fast and robust fault-recovery that can easily apply to real, complex digital systems. These Self-Repairing Algorithms make it possible for the application digital systems to be alive even though in very noisy and extreme environments.

Index Terms— **Self-Repair, FPGA, DMR(Double Modular Redundancy), Gene, Bio-Inspired Engineering.**

I. INTRODUCTION

21ST Century Information, Age to the increase in transfer rate for sending a large quantity of data rapidly and has been a lot of effort[1]. For this phenomenon, It is finding convergence study a solution in the physical structure of living cells and the unique characteristics of the system applied to Digital System[2][3].

In order to achieve systems dependability, several fault-tolerant and self-repair systems have been developed. It is one part refers to Bio-inspired engineering. Each cell has its own unique information and specific function. It was called a Stem Cell. These cells are different functions depending on the position[3][4]. Inspired from molecular biology, self-repair systems first appeared in the 1990s. In contrast to fault-tolerant systems, fault-detection modules are necessarily required in self-repairing systems [5]. Moreover, in self-repairing systems, all standby spare cells with no specified functions are initially implemented as logic blocks or routing resources in a fine-grained scale, and are to be programmed to replace the faulty cells upon the failures.

For the fault recovery method, there are two requirements: time after its detection. For some applications there could be logical correctness and temporal correctness [6]. In terms of fault recovery, logical correctness means that a circuit restores its own functionality, and temporal correctness means that a fault should be detected within a definite period of time after its occurrence, and such fault should be restored within a definite period of a problem if the repair time exceeds the fault recovery time limit. For example, if any electronic circuit cannot survive with a fault up to ten minutes, then the self-repair system must restore the fault within the first ten minutes.

In spite of this fact, until now most researchers have only focused on the logical correctness and neglect the temporal correctness for fault recovery of self-repair systems. From this standpoint, in order to meet the challenge of various applications, a new technique which guarantees a fast fault recovery is highly required.

In this paper, We propose the unique characteristics of mimicking cells and the confirm digital circuit. This model has been applied to the example of the one timer. The stem cells are differently differentiation according to the given location. But In this paper, because the increased complexity of the structure pre-differentiated cells to assume, If an error occurs in any particular area, It designed differentiation structure to two daughter cells[1].

To simplify such self-repairing architecture, partial reconfiguration of a stem cell with a built-in microprocessor can be studied in the future work. The RISA architecture can be helpful for developing such an implementation [7].

In Part II, describes main part of the overall Self Repair algorithm and the structure of the system on the block structure. In Part III, explain implemented the board's hardware specifications and the experimental results. The conclusion is Part IV.

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II. SELF-REPAIR ALGORITHMS

In this paper, We has mimicking of a cell and designed the timer circuit subdivided into specific the circuit. Conventional self-repair hardware with the differentiation process in stem cells needs the delay for cellular differentiation. However, our proposed the hardware does not need this delay because of the pre-generated redundancy.

In order to confirm the value of the output of the data in operation state, We built the DMR(Double Modular Redundancy) and TMR(Triple Modular Redundancy) structure on our algorithm. The figure below shows Flow chart of this paper

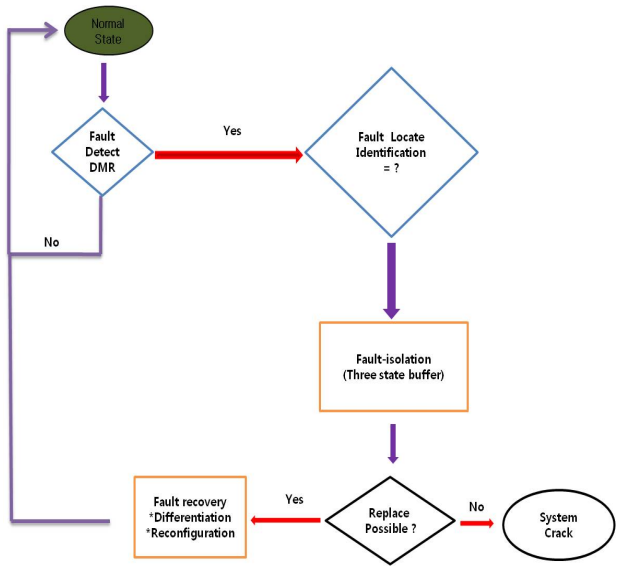

Fig. 1. Self-Repair Algorithm Flow-chart

Figure1. shows one of the flow chart at four blocks. The rest of three blocks show same flow. Each output is compared output bit. If output bit value is equal '0 ', It was normal state but If output bit is equal '1 ' then It will considered as an error state.

When Output state value is '1 ', it means occurred error at this circuit. So we must to blocking output port of the original circuit. Error modules are differentiated into the two daughter cells, It will return to normal status.

Because differentiated circuit into two daughter cells, the final output will change the TMR structure and Majority Select method. However, if daughter cell detected the error, there is no area for replacement of the hardware state. So digital system will be occurs crack. It has fast recovery and but it don't has the repair region. So in the current study was one of the disadvantages.

Since the differentiation of stem cells into redundant cells is not related to normal operation, there is no need to stop its normal operation in order to differentiate a stem cell into a redundant cell. Through pre-generated redundant cells and partial reconfiguration of stem cells, fast fault recovery can be achieved clearly.

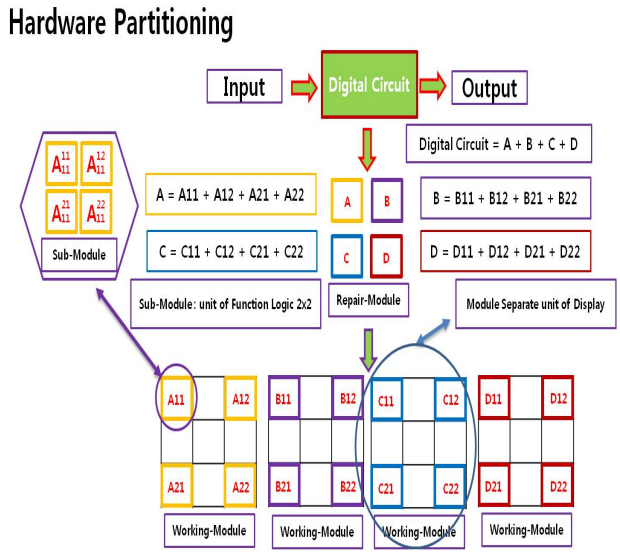

Fig. 2. Hardware Partitioning of Digital system

Figure 2 is showed the Hardware partitioning about Self-Repair algorithm in this paper. As shown this figure, Total application hardware structure was separate unit of Module. First, Current each module is separate unit of counter block, and then each sub-module is separate unit of function logic. So, our proposed algorithm was fast recovery architecture

As shown in Figure 3, Timer circuit is divided into blocks. Each output is compared output bit. If output bit value is equal '0 ', It was normal state but If output bit is equal '1 ' then It will considered as an error state.

When Output state value is '1 ', it means occurred error at this circuit. So we must to blocking output port of the original circuit. The digital circuit was divided by four blocks, and divided by other same-circuit design in center region. So error detection method is DMR structure.

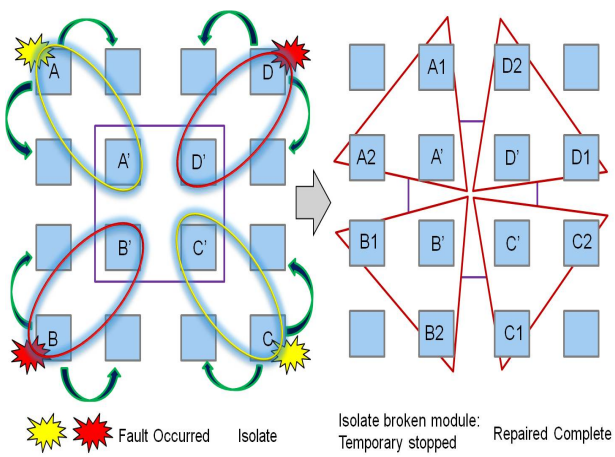

Fig. 3. Error Detect and Repair Mechanism

This circuit is one of the mother cell. Current error detection method is DMR structure. If Mother cell was detect the error, It was differentiated two daughter Cell. It will change the error detection method with TMR. Therefore, the error detection method was determined the Majority Select ways.

III. EXPERIMENTAL RESULT

In this paper, in order to confirm the self-healing algorithm, We was used the Hanback Electronics HBE-Combo III FPGA model. The FND was used to display the output of the Mother Cell. Push button was used to state of the fault.

To apply the algorithm, It was used for digital circuits. input clock of timer was divided 1 / 100 second, 1/10 seconds, one second, one minute. The figure.2 is a block diagram on FPGA designed in this paper. Digital circuit blocks of four divided by the Mother Cell. Each mother Cell is 1 / 100 second, 1/10 second, one second, one minute module block.

Digital circuit divides four blocks. The four blocks in the same four dogs was comparing the output of module. When push the button, an error detect in one block. Error module was differentiated to the two daughter cells. It will operate normally again. In this paper, we wanted a form of differentiation rather than the structures already implemented. but algorithm was designed as a pre-routing structure. Based on the results of this study, the Hardware will be change the structure. The two daughter cell into one mother cell was differentiation with the real-time using the pre-compile method.

The following figure 4 in this paper, conducted by the digital system is the timing for implementation details shows an example of one of the four blocks. Main Clock is 10MHz, and It show normally the data structure. When the value of the switch changed '0' to '1', The value of two mother cell was different. Error module output will be blocking. When input and output of the module become enable, two daughter cell was active state. Where The final output, the output of the three modules will be selected only as a result of the Majority select.

If no working cell is operable, a working cell and its corresponding redundant cell both have faults at the same time, or a working cell which originally was a redundant cell has a fault during the self-test for a faulty cell - then inevitable time delay is required for a stem cell to be reconfigured into the corresponding working cell. In this experiment, however, such situations have not been considered because they seldom happen. In future paper, The hardware will be designed to change the structure. The type of error is related to the S/W on a Embedded Processor and FPGA-based TFT LCD window between the bonding structure is designed set up.

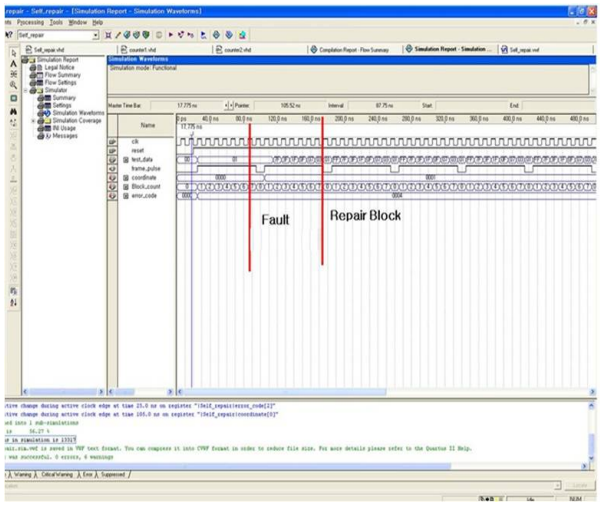

Fig. 4. Simulation Result

IV. CONCLUSIONS

In this paper, a digital circuit for fault recovery for the cells carrying the concept was applied to simulation of the properties. We seen as one of the cell with equal part at four digital circuit. More details can be further divided into four blocks of the present paper, the timer is divided by the number of building blocks. So other system can be increase count of module. In this paper, the digital circuit was mimicking of cell functions through cell division. So we must continuously control the part of error at digital circuit.

The first four module have DMR structure and error detection was found by comparing the output data. but when failed circuit was differentiated into the two daughter cells, error detection method was changed TMR structures of Majority Select structure. Through this paper, the recovery for errors real time differentiation of the structure and function features simulated cell structure was designed.

By push button in the event of failure data to identify the exact location of the error. Error module was repaired quickly with the normal state model of output. Enabled daughter cell is to quickly show that normal operation can be. Delay, however, have shown that the degree of a few clock. However, It has delay degree of one clock. in the direction of this paper is How to turn over the original value to be realized.

But It is required of the next Self-test method for fault-circuit the additional requirements of the circuit is. Daughter cell are enabled by pre-implementation Mux structure according to the function. The differentiation of cells was suitable on the daughter cell that is a bit of a file stored in the memory circuit. So It was downloaded to the FPGA bit stream. In the next study, It will be implement using the embedded system and wireless communication module. .

By utilizing partial reconfiguration techniques, when a fault occurs, our architecture does not suffer from the time-delay for downloading a stem cell. However, our implementation has a limitation in that an external PC is required for the partial reconfiguration of a stem cell.

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