Chip Impedance Evaluation Method for UHF RFID Transponder ICs over Absorbed Input Power

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Based on a de-embedding technique, a new method is proposed which is capable of evaluating chip impedance behavior over absorbed power in flip-chip bonded UHF radio frequency identification transponder ICs. For the de-embedding, four compact co-planar test fixtures, an equivalent circuit for the fixtures, and a parameter extraction procedure for the circuit are developed. The fixtures are designed such that the chip can absorb as much power as possible from a power source without radiating appreciable power. Experimental results show that the proposed modeling method is accurate and produces reliable chip impedance values related with absorbed power.

Keywords: RFID tag chip impedance, chip impedance modeling, de-embedding technique.

I. Introduction

A passive radio frequency identification (RFID) transponder is composed of a transponder chip and an antenna in a compact package. The antenna captures electromagnetic waves from an RFID reader and feeds the power to the transponder chip. In order to transfer maximum power to the chip, impedance matching between the antenna and the chip should be achieved. Antenna designers usually get the chip impedance value from chip manufacturer's data sheet, which specifies the impedance only at a limited power level and frequency. One way to evaluate the chip impedance is using the source-pull method [1], which is used for characterization of nonlinear RF devices. This method, however, requires a tuner system and specialists who can handle a complex setup and measurement. Knowledge of more complete chip impedance behavior as a function of power is becoming a crucial factor for successful tag design [2]. However, the impedance measurement issues of UHF RFID chips in thin-shrink small outline package are only addressed in [2]. Since flip-chip packaging is widely used in commercial tag manufacturing and the impedance measurement technique used in [2] is not directly applicable to this package type, we need to develop a chip impedance evaluation method suitable for flip-chip packaged IC.

As it is impractical to measure the chip impedance directly at the bonded device terminals, some form of test fixture is employed, and the effect of the fixture is de-embedded [3] later to determine the true chip impedance and the absorbed power of the chip. To evaluate the chip impedance and absorbed power of the chip simultaneously, we should know the equivalent circuit and model parameters of the fixture. For this purpose, four co-planar structured test fixtures, an equivalent circuit for the fixtures, and a set of equations used to determine the values of model parameters in the circuit are developed.

II. De-embedding and Evaluation Method

For our study, three dummy fixtures and one chip fixture are designed by using a co-planar structure. The dummy fixtures, shown in Figs. 1(a) to 1(c), are used to completely characterize (de-embed) parasitics around the mounted chip of Fig. 1(d). The chip fixture shown in Fig. 1(d) and Fig. 2 has a mounted chip and is used to test the chip. As shown in Fig. 2, a semi-rigid coaxial cable is used to provide signal power to the transponder chip from a vector network analyzer (VNA), and its effect on evaluation is removed during a calibration process of the VNA. The two strip lines that connect the coaxial cable to the chip form a kind of transmission line. The transmission line is not a parallel one but forms a loop which produces an

Manuscript received June 14, 2010; accepted July 22, 2010.

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doi:10.4218/etrij.10.0210.0208

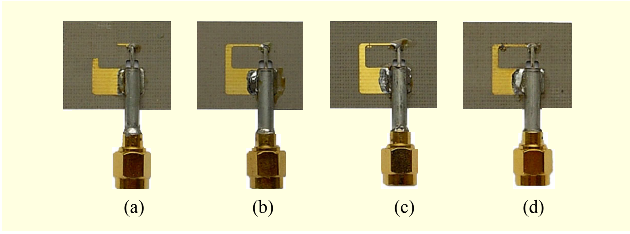

Fig. 1. Four types of fixtures: (a) fully open, (b) short, (c) open, and (d) chip fixtures.

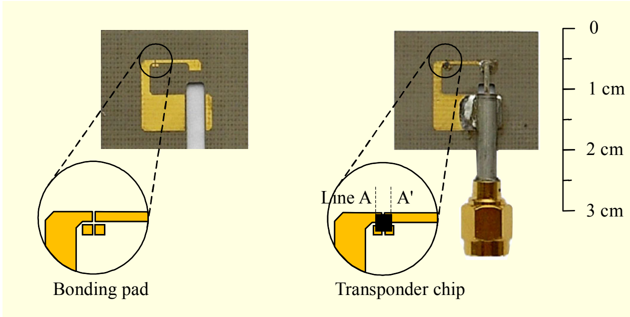

Fig. 2. Bare PCB and fully assembled chip fixture.

inductive component. This loop is used for matching the capacitive component inside the chip to allow as much power absorption as possible in the chip. To make the electromagnetic radiation from the loop negligible for modeling accuracy, the electrical length of the transmission line is kept to less than 10% of the wavelength at operating frequency, and the semi-rigid coaxial cable is used for directly connecting the VNA to the loop of the fixture.

Figure 3 shows an equivalent circuit using lumped elements when a VNA is connected to the SMA connector of the fixture in Fig. 2. The VNA is simply modeled using the signal source V_{NA} (Fig. 3) and an internal resistance R_{NA} (Fig. 3), which is 50 Ω. The model of the semi-rigid coaxial cable is not included in the equivalent circuit because the effect of the cable is removed by applying a port-extension method [4] while calibrating the VNA. The loop-shaped transmission line in Fig. 2, from the end of the coaxial cable to the line *A*-*A*', is modeled with the transmission line model composed of R_p-C_p, R_s-L_s, and R_{pc}-C_{pc} in Fig. 3.

Chip impedance, seen from line *A*-*A*' to the chip inside, is modeled with a simple parallel circuit of R_c-C_c. The chip impedance includes parasitic effects generated on the bonding pad after chip mounting and the impedance inside the chip. The four types of fixtures in Fig. 1 are designed to determine the value of each element in Fig. 3 except VNA model parameters (V_{NA}-R_{NA}).

The strip-line pattern in Fig. 1(a) is obtained when the chip and its periphery are removed from the line pattern of Fig. 1(d)

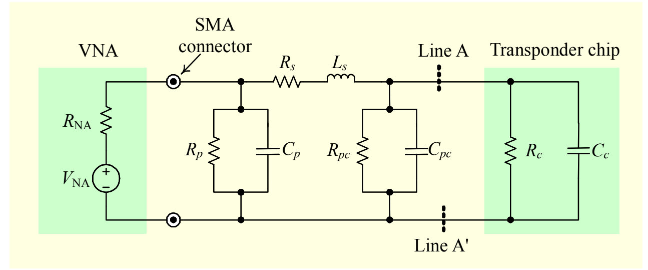

Fig. 3. Equivalent circuit of chip fixture.

(fully open). Therefore, the resulting equivalent circuit for Fig. 1(a) has only R_p-C_p, and the rest of elements are omitted because of the removal of the chip and its periphery. If we call Y_i, where *i* is *a*, *b*, *c*, or *d*, the admittance parameter converted from *S*-parameter measured at the SMA connector, the value of R_p-C_p is extracted by

$$R_p = 1/real(Y_a),\ C_p = imag(Y_a)/\omega. \tag{1}$$

The line pattern in Fig. 1(b) is a shorted one, where the bonding pad in Fig. 2 is replaced by a short strip line. If the equivalent circuit for Fig. 1(b) has R_p-C_p and R_s-L_s blocks with line A-A′ shorted, the model block R_{pc}-C_{pc} becomes inactive. Using Y_a and Y_b, the value of R_s-L_s is calculated with

$$L_s = imag\left(1/(Y_b - Y_a)\right)/\omega,\ R_s = real\left(1/(Y_b - Y_a)\right). \tag{2}$$

Figure 1(c) shows the strip-line pattern without chip mounting (open). Therefore, the equivalent circuit for Fig. 1(c) has every element in Fig. 3 except R_c-C_c and VNA block. In order to determine the value of R_{pc}-C_{pc}, admittance parameter Y_a, Y_b, and Y_c are used as

$$\begin{aligned} R_{pc} &= 1/real\left[1/\left(1/(Y_c - Y_a) - 1/(Y_b - Y_a)\right)\right], \\ C_{pc} &= imag\left[1/\left(1/(Y_c - Y_a) - 1/(Y_b - Y_a)\right)\right]/\omega. \end{aligned} \tag{3}$$

Using Y_a through Y_d, the transponder chip impedance R_c-C_c is determined by

$$\begin{aligned} R_c &= 1\Bigg/ real\begin{bmatrix} 1/\left(1/(Y_d - Y_a) - 1/(Y_b - Y_a)\right) \\ -1/\left(1/(Y_c - Y_a) - 1/(Y_b - Y_a)\right) \end{bmatrix}, \\ C_c &= imag\begin{bmatrix} 1/\left(1/(Y_d - Y_a) - 1/(Y_b - Y_a)\right) \\ -1/\left(1/(Y_c - Y_a) - 1/(Y_b - Y_a)\right) \end{bmatrix}\Bigg/\omega. \end{aligned} \tag{4}$$

Once the supply power of the VNA connected at the SMA connector of the chip fixture is set, the actual power, P_{NA}, supplied by the VNA, is measured using a power meter. The value of V_{NA} in Fig. 3 is, then, computed by $V_{\mathrm{NA}} = 2\times\sqrt{50\times P_{\mathrm{NA}}}$ in root mean square value. This V_{NA} value is needed to supply P_{NA} power to the output port when the output terminal of the VNA is terminated with 50 Ω impedance. The amount of power absorbed in the chip is the same as that of power

dissipated at R_c, which can be calculated from a circuit analysis in Fig. 3. When a desired power absorption level in the chip is given, the supplying power, P_{NA}, of the VNA varies until the desired power is dissipated at R_c.

III. Experimental Results and Discussion

In order to check the validity of the proposed evaluation method, input impedance of a mounted UHF RFID chip when the absorbed power level is –13 dBm, –9 dBm, and –6 dBm was evaluated as a function of frequency. For the experiment, three sets of fixtures in Fig. 1 were fabricated and tested one by one. Single layered PCB of ORCER RF35 (ε_r=3.50 and tan δ=0.0018) was used for the fixtures. The shape and size of the bonding pad shown in Fig. 2 were designed following the design guidelines of the mounted chip. The semi-rigid coaxial cables in the fixtures are the RG-402SR type, and the length is 25 mm. We used the EPCglobal Gen-2 certified transponder chip from Texas Instrument Inc., which is flip-chip bonded on the chip fixture. For each type of the fixture in Fig. 1, the *S*-parameter was measured with the Agilent N5230A network analyzer in the frequency range of 0.7 GHz to 1.1GHz at various power levels. The results were converted to admittance parameters, and they were used for determining the value of each element in Fig. 3 using (1) through (4) in section II. An equivalent circuit (see Fig. 3) was constructed using the values we determined at a specific frequency and power level of the VNA. By using a circuit analysis, the power dissipated at the chip R_c is calculated, and the signal power level of the VNA varies until the dissipated power reaches –6 dBm, –9 dBm, and –13 dBm.

Table 1 shows chip impedance values Z_s in ohm at three different operating frequencies (866 MHz, 915 MHz, and 956 MHz) when the chip absorbs power of –13 dBm, –9 dBm, and –6 dBm. Also, in Table 1, the values obtained from the experiment (exp) and the chip manufacturer's data sheet (mfr) are compared. The experimental values are the average results obtained from three sets of fixtures. The values from the data sheet are those measured on a bare die, according to the sheet. When we compare the impedances from the experiment and the manufacturer under the same condition, the real part of them are in close agreement, but the imaginary part shows some deviation in magnitude. In order to find out the cause of the difference, the series represented by Z_s was converted to parallel impedance. C_c columns in the table, corresponding to C_c in Fig. 3, show the value of parallel capacitance (in pico-farad) of the converted impedance. It is reasonable that the differences in C_c between the exp and mfr are mainly caused from the fact that the experimental values do include parasitic capacitance generated by chip mounting on the fixture, whereas the data from manufacturer do not. The value of C_c from the experiment at a specific frequency increases as the amount of power the chip absorbs increases. In [2], we can see a similar increase in the capacitive component of measured-transponder chip impedance as the absorbed power increases. The value of C_c from the experiment is almost constant regardless of the operating frequencies when the chip absorbs the same power. This suggests that the proposed evaluation process can produce reliable results.

Table 1. Chip impedances from exp and mfr under different frequency and power absorbing levels.

		866.5 MHz		915 MHz		953 MHz	
		Z_s	C_c	Z_s	C_c	Z_s	C_c
–13 dBm	exp	10.2-j60. 8	2.9	9.3-j57.4	3.0	9.0-j54.7	3.0
	mfr	9.4-j64.2	2.8	9.9-j60.4	2.8	9.5-j55.7	2.9
–9 dBm	exp	14.6-j56.1	3.1	12.8-j53.9	3.1	11.9-j50.8	3.1
	mfr	12.4-j65.9	2.7	11.3- j59.8	2.8	10.7- j55.7	2.9
–6 dBm	exp	18.8-j47.9	3.3	16.9-j46.7	3.3	15.3-j46.2	3.3
	mfr	17.2-j63.2	2.7	18.1- j60.4	2.7	14.5- j55.7	2.8

IV. Conclusion

This letter proposed an evaluation method which is capable of estimating complete chip impedance behavior as a function of absorbed power in flip-chip bonded UHF RFID ICs. For the evaluation, a de-embedding technique using a VNA and four simple structured coplanar fixtures has been developed. The fixtures are designed to minimize electromagnetic radiation to enhance the accuracy of evaluation results. From the experiment, the proposed evaluation method was shown to be accurate and capable of producing reliable chip impedance value as a function of absorbed power level. Though not shown here, the proposed method can be applied to other commercial flip-chip bonded RFID ICs with different chip impedance.

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