A 50-mA 1-nF Low-Voltage Low-Dropout Voltage Regulator for SoC Applications

Gianluca Giustolisi, Gaetano Palumbo, and Ester Spitale

In this paper, we present a low-voltage low-dropout voltage regulator (LDO) for a system-on-chip (SoC) application which, exploiting the multiplication of the Miller effect through the use of a current amplifier, is frequency compensated up to 1-nF capacitive load. The topology and the strategy adopted to design the LDO and the related compensation frequency network are described in detail. The LDO works with a supply voltage as low as 1.2 V and provides a maximum load current of 50 mA with a drop-out voltage of 200 mV: the total integrated compensation capacitance is about 40 pF. Measurement results as well as comparison with other SoC LDOs demonstrate the advantage of the proposed topology.

Keywords: CMOS integrated circuits, voltage regulator, low-dropout, low-voltage, system-on-chip, frequency response.

I. Introduction

Over the last decade, power management in integrated circuits (ICs) has been gaining more and more attention because it allows for drastic reduction in the consumption of battery-powered portable equipment, such as cellular phones, pagers, camera recorders, laptops, and PDAs [1]-[4]. Ordinary on-chip power management architecture consists of a single power supply (for example, an external battery) and one or more local voltage regulators (VR) to power up different sub-blocks [5]. As an example, a typical mixed-signal context may be composed of high voltage blocks (that is, I/O buffers powered at 1.8 V for compatibility reason), of medium voltage blocks (that is, analog circuits such as PLLs or operational amplifiers powered at 1.2 V to 1.4 V), and of low voltage blocks (that is, the logic circuit working at 0.6 V to 1 V) [6].

In this scenario, low-dropout voltage regulators (LDOs) have been widely used in those applications where high-performance power supply circuits are required. In fact, they can provide regulated and accurate supply voltages for noise sensitive analog blocks and, they are often arranged in series to switching regulators to remove the inherent noise produced by the switching activity [1], [2], [7].

LDOs are based on a non-inverting feedback topology made up of a voltage reference, an error amplifier (EA), and a power device. Although conceptually similar to two-stage or multi-stage amplifiers, it is harder to compensate for them because of the wider range of both the output current and load capacitance, which cause the poles to vary over many decades. As a matter of fact, load currents may range from few micro-ampere to hundreds of milli-ampere, and load capacitances may span from few tens of picofarad in SoC applications, to tens of microfarad, in external load regulation. Moreover, the

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use of a PMOS power device makes compensation even more critical as the output pole plays a significant role in the compensation.

LDOs designed for external load regulation are generally compensated for by means of a microfarad range external capacitor which also helps in attenuating the output voltage overshoots. Many designs exploit the zero given by the equivalent series resistance (ESR) of the output capacitor [1], [2], [8] while few of them use different techniques for obtaining an internal and more stable zero as the ESR changes both with temperature and frequency [9]-[12].

Recently, capacitor-free LDOs that do not require external compensation and are suitable for system-on-chip (SoC) implementation have been proposed [13]-[18]. In these cases, the capacitive load is given by the interconnection lines and, for complex and large circuits, it may grow to several hundred picofarads. However, due to the absence of an external microfarad range capacitor, it is difficult to suppress the output voltage overshoots, and only few of them are able to maintain such variations below 100 mV [16]-[18]. Moreover, when working in SoC environments, their capacitive load capability is limited to no more than 100 pF.

In this paper, we introduce a low-voltage LDO topology suitable for SoC application. The proposed LDO can be powered with a minimum supply voltage of 1.2 V and is stable for a capacitive load up to 1 nF. It is also capable of delivering 50 mA load current with a drop-out of 200 mV.

The circuit compensation does not rely on any external capacitor and exploits the multiplication of the Miller effect through current amplification [19]. This approach is well known in the design of operational transconductance amplifiers (OTA) and requires particular care during the design of the compensation network since it may give rise to complex-conjugate poles which may cause instability [20]-[22]. Moreover, in a regulator, this issue becomes pricklier since the current of the output stage (and the associated pole) may extend over several decades, which makes the compensation even more critical.

This paper is organized as follows. Section II defines the proposed LDO topology on the basis of some design considerations. Section III discusses the design of the compensation network posing the analytical conditions for obtaining stability over the whole range of load currents and capacitive loads. Section IV treats the transistor-level topology of the LDO. Section V deals with the integrated circuit implementation as well as the simulation and measurement results. Finally, we conclude in section VI.

II. LDO Design Considerations

The basic schematic of a generic LDO based on a PMOS pass-transistor is shown in Fig. 1(a). A part of the output voltage is fed back through R_1 and R_2 to the input of the EA and is compared to the voltage reference V_{REF}. Capacitor C_L stands for the capacitive load which is offered by the interconnection lines in SoC designs. The current generator, I_L, represents the load whose current is supplied by the power transistor, M_P. Quite often a voltage buffer (VB) is inserted before the power transistor to decouple the high capacitive load seen at the gate of M_P [1], [2], [23], [24]. The VB allows one to relax the EA specifications and facilitates the compensation. The compensation network, represented as a dashed box, is based on the Miller effect and is placed between the EA output and the LDO output (Fig. 1(b)).

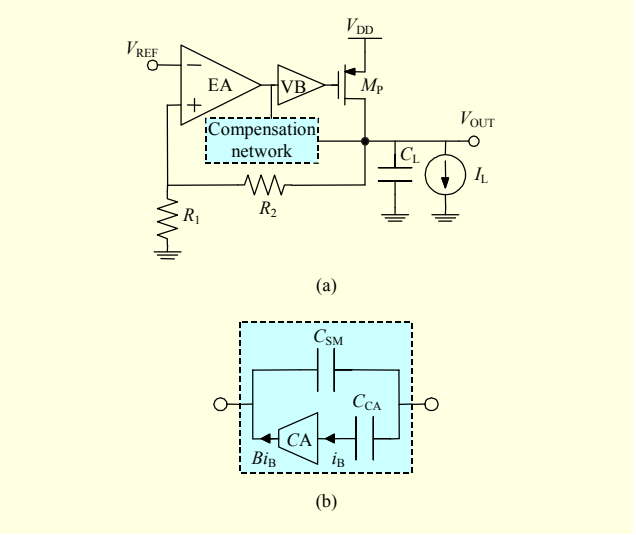


Fig. 1. (a) LDO basic structure and (b) compensation network (compensation is achieved by amplifying C_{CA} with current amplifier (CA) in conjunction to standard Miller capacitor, C_{SM}).

1. Voltage Buffer

In order to maximize the load current while saving area consumption, transistor M_P must be capable of experiencing the maximum possible overdrive, that is $V_{GSP}^{max} \approx V_{DD}$. It is worth noting that this constraint is particularly critical in low-voltage environments where the supply voltage is around 1 V to 1.5 V.

For example, consider a PMOS with 600 mV of threshold voltage, sized to deliver the current I_L^{max} when biased with $V_{SG} = 1.2$ V. The same PMOS, biased with $V_{SG} = 1.1$ V (that is, 100 mV less), requires a 25% increase in area occupation to provide the same current. The area occupation even grows to 250% if V_{SG} drops down to 0.9 V.

Referring to Fig. 1(a), under the above consideration, not only does the EA require a rail-to-rail output stage, but the use

of a decoupling VB, as in [1], [2], [23], and [24], becomes unreasonable since it reduces the power MOS overdrive. On the basis of this consideration, our LDO shall not include the decoupling VB.

2. Error Amplifier

When the EA is directly connected to the power transistor, it must be designed to rapidly charge (or discharge) the capacitive contribution seen at the gate of M_P that, quite often, may be as large as 50 pF to 100 pF [17]. On the contrary, the EA itself should provide very low power dissipation (especially in stand-by mode), and its bias currents must be kept as low as possible. It is apparent that a speed/dissipation trade-off arises, and the main limitation is manifested in terms of slew-rate (SR) of the error amplifier.

As an example, if the EA can deliver to a 50-pF power-MOS gate no more than 5 μA of current, producing a 500-mV step will take 5 μs of slewing interval. Considering that during this time the control loop of the LDO is interrupted and that the output voltage is out of control, it is apparent that such a long slewing period may negatively impact on the LDO performance, especially in terms of output voltage overshoots which may become unacceptable for many applications.

In order to completely avoid SR limitations, we used a class-AB topology for the EA. This allows improvement to the transient response without increasing the DC consumption.

3. Compensation Network

In SoC applications, the load capacitor is determined by interconnection lines and typically spans from 0.1 to 1 nF [16]-[18]. This capacitive value is too small to set a dominant pole at the output node, and the compensation must be achieved through the Miller effect. Treating the LDO in Fig. 1(a) as a common two-stage amplifier (although very similar), would lead to a compensation capacitor of a few hundred picofarads which may cause serious problems to the integration.

Such a huge compensation capacitor can be reduced, multiplying its effect through the use of current amplifiers (CAs), as addressed in [22]. The idea is not new and was already used in LDO compensation in [23]-[27], where, however, external capacitors were necessary. Indeed, in [23], the compensation requires an external compensation capacitor of at least 1.5 nF. In [25] and [26], the external compensation capacitor grows to 50 nF. In [24] and [27], an external microfarad range capacitor is necessary.

The compensation network that we adopted is shown in Fig. 1(b), and is made up of a compensation capacitor, called C_{CA}, because it is amplified by B through a CA. Moreover, the compensation network also includes a standard Miller capacitor, C_{SM}, that will be proven to be necessary. However, thanks to the amplification experienced by C_{CA}, the value of C_{SM} is not so high to have an impact on its integration.

III. Design of the Compensation Network

1. Analysis of the Stability

The regulator of Fig. 1 has two loops: an *external loop*, due to the feedback of the output voltage through R_1 and R_2, and an *internal loop*, due to the compensation network.

The worst-case for stability is when the regulator is used in unity-gain configuration, that is with $R_1 = \infty$ and $R_2 = 0$. The open-loop small-signal circuit for evaluating the loop-gain is shown in Fig. 2. Elements C_{in}, G_{m1}, R_{o1}, and C_{o1} model the error amplifier and its equivalent output load. Elements G_{m2}, R_{o2}, and C_L model the power stage and the overall output load. Observe that G_{m2} and R_{o2} depend on the load current I_L and that, specifically, G_{m2} changes within several orders of magnitude. The current amplifier is represented by its input resistance, R_{CA}, and the current-controlled current source, Bi_b. Since C_{in} is usually very small (it is the input capacitance of a differential pair), it will be neglected in our analysis. C_{o1} is mainly due to the gate-source and gate-bulk capacitances of the power MOS while $C_{FB} = C_{SM} + C_{gd}$, where C_{gd} is the power MOS gate-drain capacitance.

The complete open-loop transfer function of the regulator modeled in Fig. 2 is

$$T(s) = -\frac{v_{out}}{v_{in}} = T(0)\frac{\left(1-\frac{s}{z_{LHP}}\right)\left(1-\frac{s}{z_{RHP}}\right)}{1+a_1 s+a_2 s^2+a_3 s^3}, \quad (1)$$

where

$$\begin{aligned} T(0) &= G_{m1}R_{o1}G_{m2}R_{o2}, \\ z_{LHP} &= -\frac{1}{R_{CA}C_{CA}}, \\ z_{RHP} &= \frac{G_{m2}}{C_{FB}}, \\ a_1 &\approx \left[G_{m2}R_{o1}\left(BC_{CA}+C_{FB}\right)+C_L\right]R_{o2}, \\ a_2 &\approx C_L\left(C_{FB}+C_{o1}\right)R_{o1}R_{o2} \\ &\quad + C_{CA}\left(C_{FB}G_{m2}R_{o1}+C_L\right)R_{o2}R_{CA}, \\ a_3 &\approx C_L C_{CA}\left(C_{FB}+C_{o1}\right)R_{o1}R_{o2}R_{CA}. \end{aligned} \quad (2)$$

Stability is guaranteed when both the external and the internal loops are properly compensated. In particular, the internal loop may be responsible for two complex-conjugate poles [21], [22]. Assuming $T(s)$ has a dominant pole, we

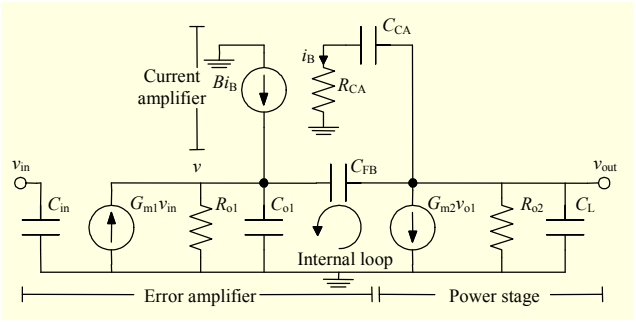


Fig. 2. LDO with CAM and SM compensation: small-signal schematic.

can represent (1) as

$$T(s) \approx T(0)\frac{\left(1-\frac{s}{z_{LHP}}\right)\left(1-\frac{s}{z_{RHP}}\right)}{\left(1-\frac{s}{p_D}\right)\left(1+\frac{s}{GBW_I}+\frac{s^2}{GBW_I^2 K_I}\right)}, \quad (3)$$

where

$$p_D \approx -\frac{1}{a_1},$$
$$GBW_I \approx \frac{a_1}{a_2}, \quad (4)$$
$$K_I \approx \frac{a_2^2}{a_1 a_3}.$$

Neglecting the zeroes, the term $1+s/GBW_I+s^2/GBW_I^2K_I$ in the denominator of (3) represents the closed-loop transfer function of the internal loop whose open-loop transfer function takes the form

$$T_I(s) = \frac{T_I(0)}{\left(1-\frac{s}{p_{DI}}\right)\left(1-\frac{s}{p_{2I}}\right)}, \quad (5)$$

where $T_I(0)$ is the DC gain, p_{DI} is the dominant pole of the internal loop, and p_{2I} is the second pole of the internal loop. These latter quantities are related to GBW_I and K_I through

$$GBW_I = T_I(0)\cdot|p_{DI}|,$$
$$K_I = \frac{|p_{2I}|}{GBW_I}. \quad (6)$$

It is apparent that GBW_I is the gain-bandwidth product of the internal loop, and that K_I, defined as the ratio between the second pole and the gain-bandwidth product, is related to the stability of the internal loop [21], [22]. Specifically, under the assumption that the internal loop is stable, the gain-bandwidth product, GBW_I, approximates the transition frequency of the internal loop and therefore

$$\tan(\phi_{mI}) \approx K_I, \quad (7)$$

ϕ_{mI} being the phase margin of the internal loop.[1)]

If $K_I \approx 1$, the internal loop is stable with a phase margin $\phi_{mI} \approx 52°$, and a small peak is present in the frequency domain. If $K_I \approx 2$, the phase margin is $\phi_{mI} \approx 65°$, and the frequency response is maximally flat. Finally, for $K_I > 4$, the poles of the closed-loop transfer function related to the internal loop are real [21].

Once the internal loop stability is guaranteed, the overall stability depends on the external loop and, specifically, on the ratio between the equivalent second pole of the external loop, p_2, and the overall gain-bandwidth product, $GBW = T(0)\,|p_D|$. The equivalent second pole depends on the closed loop transfer function of the internal loop and is approximately equal to GBW_I. Consequently,

$$K_E = \frac{|p_2|}{GBW} \approx \frac{GBW_I}{GBW} = \frac{a_1^2}{a_2 T(0)}, \quad (8)$$

which has a similar meaning to K_I but refers to the external (or overall) loop. In particular, as in (7), the overall phase margin, ϕ_m, is approximately given by

$$\tan(\phi_m) \approx K_E. \quad (9)$$

The stability of the overall amplifier is certainly guaranteed if $K_I \geq 1$ and $K_E \geq 1$. In general, a convenient choice is setting $K_I = K_E = 2$ which guarantee a maximally flat response in the closed-loop gain of the internal loop and an overall phase margin of about 65° [21], [22].

The LDO compensation must account for the fact that the large-signal current of the second stage (and hence G_{m2}) varies within several orders of magnitude (that is, from I_L^{min} to I_L^{max}). Therefore also K_E and K_I fluctuate with the load current, thus making the compensation problematic. However, by keeping both K_E and K_I higher than minimum targets, K_{ET} and K_{IT}, we ensure the stability in the whole output current range. Therefore, the behavior of both K_E and K_I with G_{m2} has to be analyzed.

2. Stability of the Internal Loop

Under the assumption that $R_{CA}C_{CA} << R_{o1}(C_{FB}+C_{o1})$, substituting (2) into (4), and equating $\partial K_I/\partial G_{m2} = 0$, we find the minimum of K_I by

$$K_I^{min} \approx \frac{4C_{FB}}{BC_{CA}+C_{FB}}, \quad (10)$$

and the corresponding value of G_{m2} by

1) An accurate expression that bounds K_I and ϕ_{mI} together may be found in [28] where, for a pure two-pole system, we have $\tan^2(\phi_{mI}) = \frac{2K_I}{\sqrt{K_I^2+4}-K_I}$.

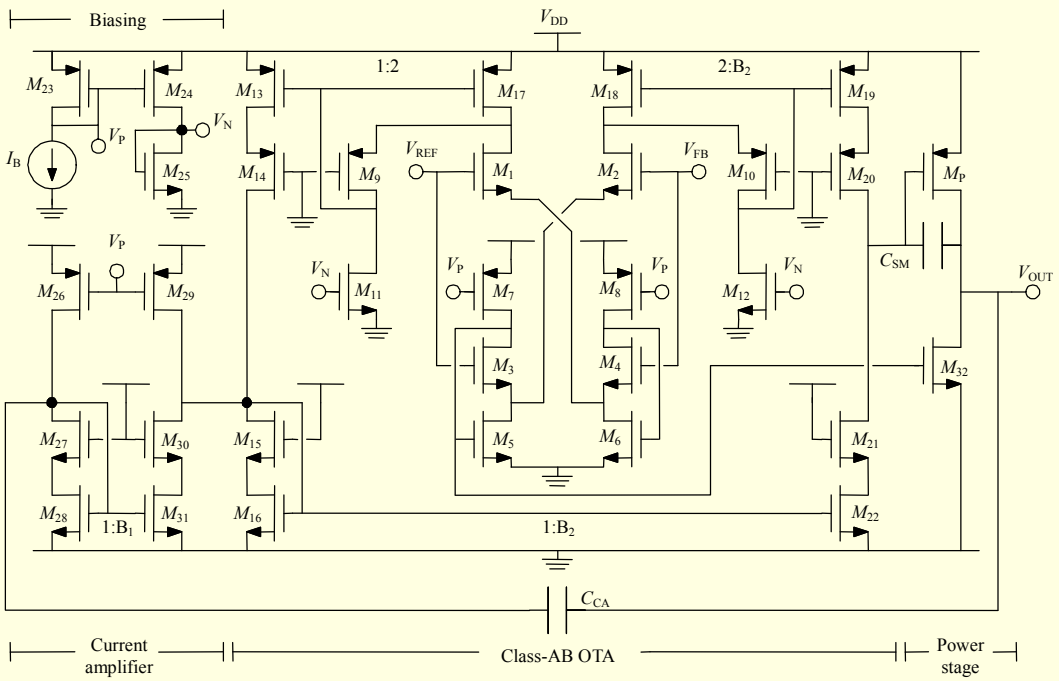


Fig. 3. Circuit implementation of proposed LDO.

$$G_{m2}^{(K_I)} \approx \frac{C_L\left(C_{o1}+C_{FB}\right)}{R_{CA}C_{CA}C_{FB}}. \tag{11}$$

Imposing K_I^{min} equal to a target value K_{IT}, we stabilize the internal loop of our LDO for any value of G_{m2} (hence for any load current value). This constraint leads to a precise relationship between C_{FB} and the equivalent compensation capacitance BC_{CA}, that is

$$C_{FB} = \frac{K_{IT}}{4-K_{IT}} BC_{CA}. \tag{12}$$

Relationship (12) reveals that a standard Miller capacitor ($C_{SM} = C_{FB} - C_{gd}$) is often mandatory to stabilize the internal loop.

3. Stability of the External Loop

Substituting (2) into (8) and equating $\partial K_E / \partial G_{m2} = 0$, we find that K_E presents a minimum for

$$G_{m2}^{(K_E)} \approx \frac{C_L}{\left(BC_{CA}+C_{FB}\right)R_{o1}}. \tag{13}$$

However, for typical on-chip loads ($C_L \le 1$ nF), this value is smaller than any reasonable value of G_{m2}^{min}, so we may state that

$$\frac{\partial K_E}{\partial G_{m2}} > 0, \qquad \forall G_{m2} > G_{m2}^{min}. \tag{14}$$

This means that the minimum value of K_E is obtained for the minimum transconductance, G_{m2}^{min}, that is

$$K_E^{min} = K_E\big|_{G_{m2}^{min}}. \tag{15}$$

If we impose K_E^{min} equal to a target value K_{ET}, considering (12), we obtain

$$C_{CA} = \frac{\left(4-K_{IT}\right)K_{IT}K_{ET}}{32B}\frac{G_{m1}}{G_{m2}^{min}}C_L \times\left(1+\sqrt{1+\frac{64}{K_{IT}^2K_{ET}}\frac{G_{m2}^{min}}{G_{m1}}\frac{C_{o1}}{C_L}}\right). \tag{16}$$

It is apparent that C_{CA} is proportional to C_L and that a high current gain B helps in reducing the area occupation.

In addition, it is worth to noting that, from (12) and (16), the total compensation capacitance, $C_{CA}+C_{SM}$, depends on the ratio G_{m1}/G_{m2}^{min}. However, reducing the area occupation (that is, $C_{CA}+C_{SM}$) through G_{m1} means slowing down the LDO speed response. On the contrary, decreasing the area occupation through G_{m2}^{min} increases the DC stand-by current, I_L^{min}. Therefore, a trade-off between area ($C_{CA}+C_{SM}$), speed (G_{m1}), and dissipation (I_L^{min}) exists.

IV. LDO Topology

The complete schematic of the proposed LDO is shown in Fig. 3. It is made up of a class-AB OTA, current amplifier,

biasing stage, and power stage.

1. Error Amplifier

As mentioned in II.2, to improve the transient response without increasing the DC consumption, the error amplifier is based on a class-AB topology and is made up of transistors M_1 to M_{22}.

The input stage structure is a revised version of the class-AB stage reported in [29]. Assuming $(W/L)_{1,2} = (W/L)_{3,4}$, when $V_{FB} = V_{REF}$, the differential pair current is forced to be equal to the bias current set by the current sources M_7 and M_8, that is, $I_{D1,2} = I_{D7,8}$. More in general, assuming a first-order model for MOS transistor, when $V_{FB} \neq V_{REF}$, we get

$$\begin{aligned} I_{D1} &= I_{D7,8} - 2\sqrt{\beta_{1,2} I_{D7,8}}\, V_D + \beta_{1,2} V_D^2, \\ I_{D2} &= I_{D7,8} + 2\sqrt{\beta_{1,2} I_{D7,8}}\, V_D + \beta_{1,2} V_D^2, \end{aligned} \tag{17}$$

being $\beta_{1,2} = (1/2)\mu_n C_{ox} (W/L)_{1,2}$ and $V_D = V_{FB} - V_{REF}$.

The input stage is then placed into a low-voltage stacked mirror structure. Specifically, current I_{D1} is carried to the EA output and amplified by $B_2/2$ through the low-voltage cascode current mirrors M_{17} to M_{13} and M_{16} to M_{22}. Meanwhile, current I_{D2} is carried to the EA output and amplified by $B_2/2$ through the current mirror M_{18} and M_{19}. Hence, the voltage produced at the EA output node is

$$V_{outEA} = \frac{B_2}{2}\left(I_{D2} - I_{D1}\right) R_{o1} = G_{m1} R_{o1} V_D, \tag{18}$$

where $G_{m1} = B_2\sqrt{\beta_{1,2} I_{D7,8}}$ the EA transconductance and $R_{o1} = (g_{m21} g_{m22} r_{d22} \,\|\, g_{m20} g_{m19} r_{d19})$ the output resistance.

In the EA, we used cascode mirrors to obtain a higher DC gain by increasing R_{o1}. This seems to reduce the swing of M_P to $V_{SGP}^{max} = V_{DD} - 2V_{DS}^{sat}$. However, if V_{SGP} approaches $V_{DD} - 2V_{DS}^{sat}$, what really happens is the drop of the DC gain, due to the reduction of the EA output resistance, which becomes $R_{o1} \approx r_{d22}$. Nevertheless, the gain still remains high (~ 30 to 40 dB) to guarantee the proper voltage regulation.

2. Current amplifier

To save area consumption, the compensation must exploit the multiplicative effect provided by the CA and, as a consequence, the amplification factor B must be as high as possible.

In the proposed LDO, we split the CA into two smaller current amplifiers based on low-voltage cascode current mirrors whose gains are B_1 and B_2, respectively. The splitting allows one to obtain the signal inversion, easily. Moreover, this helps in saving the stand-by power consumption since CAs amplify DC components, too.[2)]

In Fig. 3, the first CA is made up of transistors M_{26} to M_{31} and has a gain of B_1. The second CA, with a gain of B_2, is shared with the error amplifier and is made up of M_{15} and M_{16}.

3. Biasing and Power Stage

The biasing section is made up of transistors M_{23} to M_{25} and provides the bias voltages for the n-based and p-based biasing current mirrors.

The power stage is composed of the power MOS, M_P, and its biasing transistor, M_{32}. The latter imposes a minimum current (I_L^{min}) through M_P, which guarantees regulation even without any (external) load. In order to obtain fast responses during negative load transients (that is, for I_L abruptly decreasing), transistor M_{32} is connected to the gate of M_5 thus exploiting the class-AB operation of the OTA. This avoids the typical transient behavior where the settling response is typically longer after a negative load transient than after a positive one due to the intrinsic asymmetric structure of the linear regulator.

In the proposed LDO, when I_L suddenly falls off, V_{OUT} and V_{FB} tend to go high. The increment of V_{FB} not only does adapt the drain current of M_P to I_L (as in traditional LDOs) but also increases the current on both M_5 and M_{32} which rapidly discharge the load capacitor C_L and improve the time response.

V. LDO Design and Characterization

The regulator has been integrated in standard 0.35-μm CMOS technology ($V_{Tn} \approx 0.55$ V, $V_{Tp} \approx 0.65$ V, $\mu_n C_{ox} \approx 0.175$ μA/V^2, $\mu_p C_{ox} \approx 0.60$ μA/V^2). The IC has been designed to work with an external voltage reference $V_{REF} = 1$ V and has

Table 1. Transistor aspect ratios of proposed LDO.

Transistors	Aspect ratios
$M_1 - M_4$	9.6/0.6
M_5, M_6	4.8/0.6
$M_7 - M_{16}$	12/1
M_{17}, M_{18}	24/1
$M_{19} - M_{22}$	48/1
$M_{23} - M_{28}$	12/1
$M_{29} - M_{31}$	60/1
M_{32}	24/0.6
M_P	50000/0.6

2) If I_{CA} is the bias current in the input branch of a CA, using a single amplifier of gain B_1B_2 dissipates $(1 + B_1B_2)I_{CA}$, while splitting the gain into two CAs dissipates $(2 + B_1 + B_2)I_{CA}$.

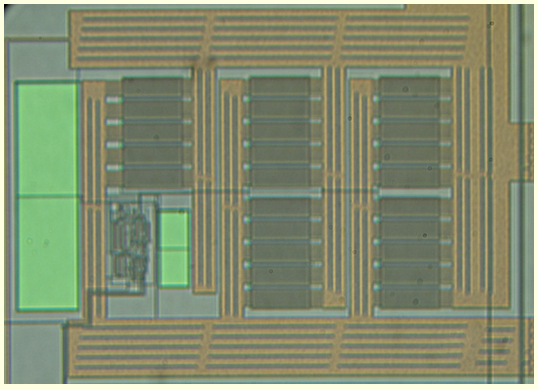


Fig. 4. Chip photo of proposed LDO voltage regulator.

been optimized for a supply voltage ranging from 1.2 to 1.5 V, although it can work at 3.3 V, also. Two IC pins were dedicated to V_{FB} and V_{OUT} so to allow the use of different feedback factors by means of off-chip resistive partitions (in the case of unity-gain configuration, V_{FB} was obviously short circuited to V_{OUT}). The external bias current, I_B, flowing through transistor M_{23}, has been set to 1.5 μA .

Transistor aspect ratios are reported in Table 1. The circuit is able to provide a load current of 50 mA with a drop-out voltage of 200 mV.

The DC current flowing through the differential pair transistors is about 1.5 μA and the minimum (internal) load current is $I_L^{min} \approx 15$ μA. It follows that $G_{m1} \approx 140$ μA/V and $G_{m2}^{min} \approx 500$ μA/V. The power MOS parasitic capacitances are $C_{o1} = C_{gs} + C_{gb} \approx 40$ pF and $C_{gd} \approx 5$ pF.

The compensation network has been sized in order to maintain stability for load capacitors up to 1 nF. The stability has been imposed setting $K_{IT} = 1$ and $K_{ET} = 1.2$, that is, a phase margin of about 52° for the internal loop and about 55° for the external loop. The overall current gain has been set to $B = 20$, and the two gains of the current amplifiers are $B_1 = 5$ and $B_2 = 4$. From (12) and (16), we have set $C_{CA} = 6$ pF and $C_{SM} = 35$ pF. It is worth noting that a pure standard Miller compensation (that is, with no current amplifier) would have required a theoretical compensation capacitor of about 250 pF for compensating the LDO with the same capacitive load and the same phase margin of 55°.

The chip photo of the proposed LDO is shown in Fig. 4. As expected, the main contribution to area occupation is due to the power MOS and the two compensation capacitors.

1. Simulation and Experimental Results

The simulated[3] Bode plots of the LDO loop-gain in the case of unity-gain feedback factor (the worst-case for stability) is shown in Fig. 5, with different values of load current. More specifically, Fig. 5(a) depicts the Bode plots when the circuit is powered by a 1.2 V supply voltage and the load current ranges from the no-load condition to 50 mA. In this case, as expected from theory, the minimum phase margin occurs at no load and is about 57°. Observe that, as discussed in IV.1, when the load current approaches 50 mA, the DC loop-gain drops to its minimum value because $V_{SGP} \approx V_{DD} - V_{DS}^{sat}$ and M_{21} enters the triode region. Figure 5(b) depicts the Bode plots when the circuit is powered by a 1.5 V supply voltage. The Bode plots are similar to the case of $V_{DD} = 1.2$ V except for the DC gain which is less sensitive to the load current.

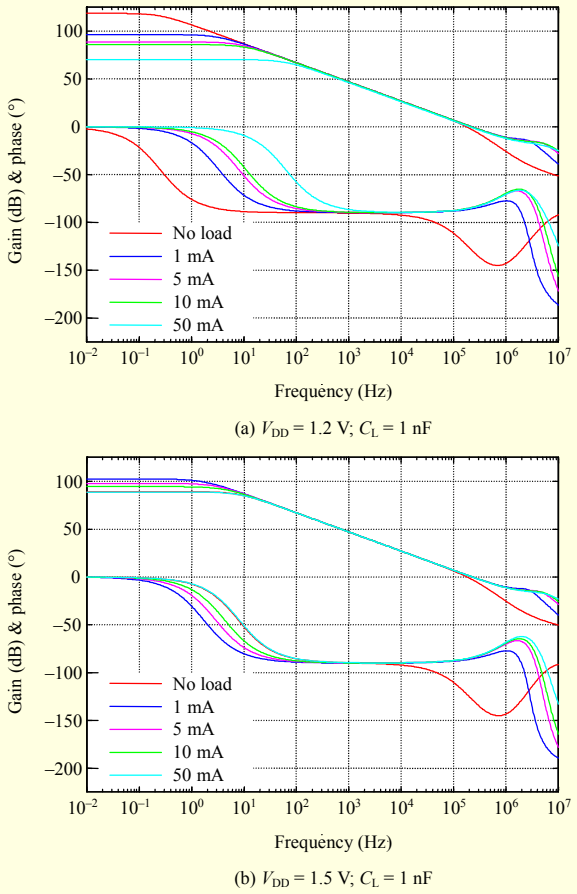


Fig. 5. Simulation of open-loop gain and phase of proposed LDO in buffer configuration ($V_{OUT} = V_{REF} = 1$ V) for different values of I_L.

Figure 6 shows the measured load regulation of the proposed LDO at $V_{OUT} = V_{REF} = 1$ V for three different values of power supply. Measurements have been taken for load currents up to 70 mA. It is apparent that, at $V_{DD} = 1.2$ V, the circuit exhibits a drop-out of 200 mV at 50 mA of load current.

3) Simulations have been performed in Cadence environment using the Spectre simulator.

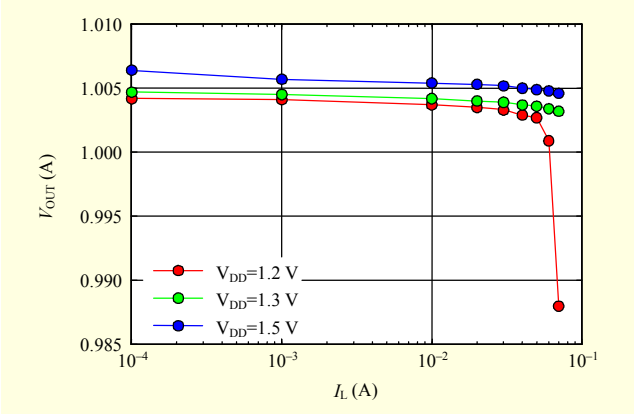
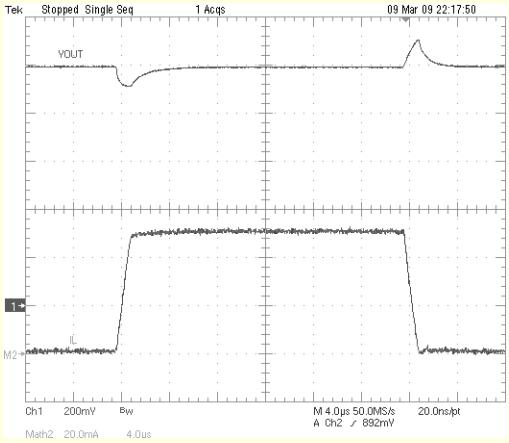
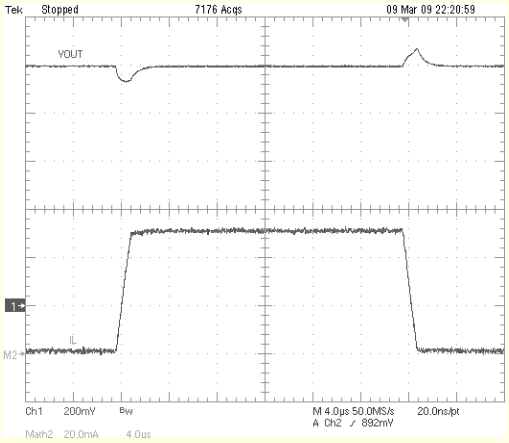


Fig. 6. Load regulation of proposed LDO at different supply voltages.



(a) V_{DD} = 1.2 V; C_L = 1 nF



(b) V_{DD} = 1.5 V; C_L = 1 nF

Fig. 7. Measurement results of V_{OUT} for I_L going from 1 mA to 50 mA and back to 1 mA.

Figure 7 displays the measured transient response of the output voltage for load current steps in the worst-case of output capacitor (that is, C_L = 1 nF). Specifically, Fig. 7(a) refers to the circuit powered by a 1.2-V supply voltage while Fig. 7(b) refers to the LDO powered at 1.5 V. In both measurements, the load current I_L goes from 1 mA to 50 mA and back again to 1 mA with a rise/fall-time of about 1 µs. Positive and negative overshoots stay below 70 mV while the response time, T_R, takes about 4 µs.

Table 2. Performance comparison between recent works on SoC LDOs.

	[14]	[15]	[16]	This work
Year	2003	2007	2007	2009
Process	0.6 µm	0.35 µm	0.35 µm	0.35 µm
V_{IN}	1.5 V	3 V	1.2 – 3.3 V	1.2 – 1.5 V
V_{OUT}	1.3 V	2.8 V	1 V	1 V
Drop-out	200 mV	200 mV	200 mV	200 mV
C_C^{total}	12 pF	7 pF	6 pF	41 pF
C_L^*	~ 0 pF	0 – 100 pF	100 pF	0 – 1 nF
I_L^{max}	100 mA	50 mA	100 mA	50 mA
I_Q	38 µA	65 µA	100 µA	45 µA
ΔV_{OUT}	100 mV	< 90 mV	50 mV	70 mV
Settling	~ 2 µs	~ 15 µs	~ 10 µs	~ 24 µs
FOM_1	0.76 ns	19.5 ns	10 ns	3.6 ns
FOM_2	0.92 ** ns	1.36 ns	0.60 ns	0.15 ns

* Internal capacitive load (SoC)
** Estimated load capacitor ~10 pF

2. Performance Comparison

Table 2 provides comparison between the performance of the proposed LDO regulator and other published designs that are targeted for SoC power management. The figure of merit (FOM)

$$\text{FOM}_1 = T_R \times \frac{I_Q}{I_L^{max}}, \quad (19)$$

previously used in [6] and [15], is adopted here to evaluate the effect of the load transient response time (T_R) in different designs. A lower FOM implies a better slewing performance. On the basis of FOM_1, our LDO has a good time-response performance. The figure of merit FOM_1 does not take into account the different maximum SoC capacitive load, C_L^{max}, that each LDO may experience and invariably affects the time response. Moreover, it does not give any information on the area occupied by the overall compensation capacitor C_C^{tot}. To consider both the effects, we also compared the LDOs through another FOM, defined as

$$\mathrm{FOM}_2 = \mathrm{FOM}_1 \times \frac{C_{\mathrm{C}}^{\mathrm{tot}}}{C_{\mathrm{L}}^{\mathrm{max}}}, \quad (20)$$

which is an upgrade of FOM_1. Once again, a lower FOM implies a better performance.

From Table 2, it is apparent that the proposed LDO has the best FOM_2 which is from 4 to 9 times lower than that of other designs.

VI. Conclusion

In this paper, a low-voltage LDO regulator for SoC power management has been presented. The proposed LDO is capable of providing 50 mA with a drop-out voltage of 200 mV when powered at 1.2 V. The circuit exploits a class-AB OTA and double-loop compensation based on the amplification of the Miller effect through the current amplifier.

The design procedure for obtaining the proper stability for wide output current and load capacitor ranges has been illustrated and discussed in detail.

The LDO was integrated and the experimental results have proven the high performance of the proposed topology.

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