Low-Cost High-Performance TDD Synchronizer for WiBro RF Repeater

Young-Ho Seo and Dong-Wook Kim

WiBro radio frequency (RF) repeater is used for solving the problem of partial shadow areas in the wireless communication field that uses time-division duplexing (TDD) mode. In this paper, a method to efficiently generate TDD signals for WiBro RF repeater is proposed and its digital circuit is implemented. A TDD signal is detected from RF signals transmitted/received to/from RF repeater and then inputted again into the RF repeater, so that it can operate normally. First, the envelope of downlink signals is detected and then clamped to extract the basic form of a TDD signal using an operational amplifier circuit. Next, the TDD signal is generated by restoring and filtering the shape which has been distorted by the wireless channel. The algorithm and system to acquire TDD signal are developed with a goal to have simple but powerful functions with as little cost as possible. The proposed method is implemented as an RF-digital integrated system and verified through the experiments under the same condition as actual WiBro service environment.

Keywords: TDD signal, synchronization, WiBro, design, FPGA, RF repeater.

I. Introduction

As the high-speed internet service market has reached its maturity, the user, whether stationary or mobile, has increasingly desired high-speed internet services. To satisfy such desire, WiBro has been developed in which wireless and cable communication networks are integrated to enable easy access to the Internet. WiBro, developed and introduced to meet the demand for multimedia services, can provide still or travelling subscribers with high-speed wireless Internet services at the rate of about 3 Mbps. The services provided by WiBro include streaming services (for example, VoD), video call services (for example, VoIP), FTP, E-mail, SMS, background services such as multicast/broadcast services, and interactive services like web-browsing. WiBro guarantees the mobility of about 60 km/h, a property which is between wireless LAN and a mobile communication system. It supports the data rate of about 3 Mbps which is between mobile communication system and a high-speed cable network. For this reason, it is recognized as a run-up for the 4th generation mobile communication [1]-[3].

An RF repeater in the wireless communication field that uses time division duplexing (TDD) should be accurately synchronized with its high-order system (base station) to control uplink (UL), downlink (DL), and idle regions (TTG and RTG). Since it does not have separate media for transmitting uplink synchronization signals, RF repeater should generate its own synchronization signals that have the same period and phase as those of a high-order system, by processing the signals transmitted from the high-order system [4], [5].

In the conventional system, a radio frequency (RF) repeater generally acquires the synchronization signal by demodulating

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and analyzing the signals from its high-order system. There is another relatively simple method to acquire the synchronization signal, and that is to correlate the preamble signal of the demodulation signal and then find the start point of the downlink signal. Both of these methods are available at low input-signal strength and fully satisfy the performance requirement of an RF repeater. However, the fact that it uses an expensive modern chip has been an obstacle in developing a moderately-priced TDD-based RF repeater [6]-[8].

This paper aims at developing a technology to acquire and generate the synchronization signal for an RF repeater that uses TDD mode as WiBro does [9], [10]. For this, the RF repeater synchronizes uplink, downlink, and idle regions with its high-order system when the base station sends a DL signal to the terminal and the terminal sends UL signal to the base station through temporal crossing. If the synchronization signal can be extracted (by detecting the downlink signal envelope, amplifying it, and restoring the distorted signals by the wireless channel environment) as the downlink signal envelope is detected and amplified, and the signals distorted in the wireless channel environment is restored, it would be possible to implement the technology with relatively inexpensive parts. Accordingly, it becomes possible to reduce the cost of a TDD-based home RF repeater to the level of the conventional repeater that uses frequency division duplexing (FDD) mode. It will contribute to the increase of the popularity of TDD-based home RF repeater that has not been widely commercialized because of its high manufacturing cost caused by using expensive modem chips. Generally the typical technique generates a TDD synchronizing signal by analyzing and demodulating the received signal from the upper communication system. Another previous technique correlates the preamble signals of the demodulated signal, detects the start points of the WiBro frames, and then produces TDD signal on the basis of those points. This method can operate at the low input level and satisfy the required specification for the WiBro RF repeater. However, both of them require the high-cost modem chipset. Since it increases the system complexity of the digital part in the repeater, the previous methods have been a major obstacle to develop a low-cost commercial RF repeater based on TDD synchronization. The proposed low-cost system will contribute to economically clearing partial shadow areas in TDD-based wireless communication like WiBro.

This paper is organized as follows. The WiBro RF repeater and the concept of TDD are introduced in section II. The proposed algorithm and techniques for TDD synchronization are described in section III. The proposed hardware architectures are shown in section IV. The experiment result is explained in section V. Finally, this paper is concluded in section VI.

II. WiBro RF Repeater and TDD

WiBro uses TDD mode, not FDD mode. It does not need a guard band and is capable of adjusting time slices depending on the traffic conditions of the UL and DL. Because of the reversible characteristics of UL and DL channels, it is possible to effectively introduce the concepts of multiple-in multiple-out (MIMO) and smart antenna and to increase the efficiency of frequency usage. Also, as it adopts orthogonal frequency division multiple access (OFMDA), granularity is guaranteed and frequency resources can be efficiently used. OFDMA works well in the multipath delay spread wireless environment, does not have inter-channel interference in the cell, and facilitates resource allocation [11]. It groups several subcarriers into one subchannel, and allocates traffic resources to each subchannel, according to full usage of the subchannels (FUSC), partial usage of the subchannels (PUSC), or tile usage of subchannels (TUSC) mode. The physical layer of WiBro symbol is exemplified by the 5 ms frame shown in Fig. 1 [11], [12].

Because WiBro RF repeater adopts TDD mode for hardware characteristics, it complies with 2.3 GHz band wireless Internet standard [1]. Depending on TDD characteristics, it carries out the function to prevent over-input to a UL part when DL signals are transmitted. In the DL region, the DL part is on and the UL part is off. On the contrary, in the UL region, the DL part is off and the UL part is on. In other words, DL and UL parts perform a switching action. Switching occurs in RTG and TTG regions, as shown in Fig. 1. The initial action is set to the DL region. Before TDD switching operates normally, the power amplifier (PA) in DL should not operate. When the symbol rate is changed, the TDD signal should also be changed automatically. In this paper, the system block that generates TDD signals is called a TDD synchronizer. The TDD synchronizer should detect the rates of DL and UL, and when the rate is changed, it should be able to automatically detect the changed rate. The DL:UL symbol rate serviced by SK Telecom, Korea, is one of three rates (30:12, 27:15, 24:18). Each symbol rate is defined as a mode. The TDD signal generated by the TDD synchronizer is inputted to the RF circuit, to activate the repeater.

Figure 1 shows the structure of WiBro frame. WiBro uses 1024 FFT-based OFDMA in the 5 ms frame. While the conventional CDMA identifies users using codes, WiBro allocates resources to users by identifying them using the location of OFDMA part carrier. A 5 ms symbol consists 42 OFDMA symbols, and each OFDMA symbol has 1,024 tones. The 42 OFDMA symbols are divided into 27 DL signals and 15 UL TDD signals. Of the 27 DL signals, one is used for preamble, 8 for MAP, and 18 for user data transmission. Of the

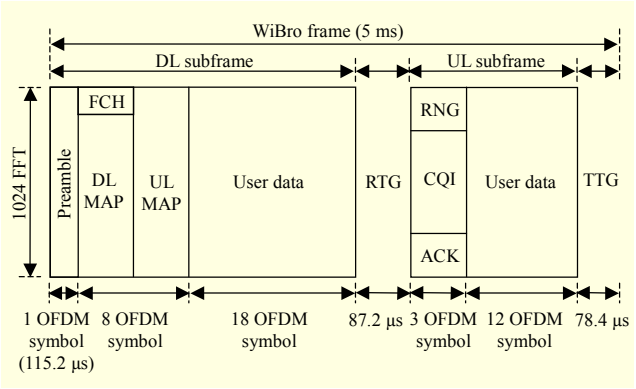


Fig. 1. OFDM-based WiBro symbol.

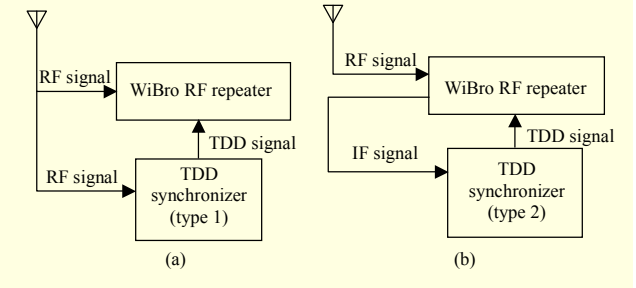


Fig. 2. WiBro RF repeater and TDD signal generation.

Table 1. Frequency band used.

Item	Specification
Duplexing	TDD
Frequency	2,300 – 2,327 MHz

Table 2. RF output power (max. output).

Classification	Specification	
Forward	2 dBm/FA, 7 dBm/Total	3FA
Reverse	13 dBm/Total	3FA

15 UL signals, 3 are used for UL control and 12 for user data transmission.

As shown in Fig. 2, TDD synchronizer extracts synchronization signal from WiBro RAS DL signals and reliably outputs the switching control signal that is appropriate for DL and UL periods defined by WiBro system. TDD signals detected by TDD synchronizer should be output reliably despite distortion, duplication, attenuation, and/or delay of signals such as multipath fading. Tables 1 and 2 summarize the frequency band used by WiBro RF repeater and its output power [12].

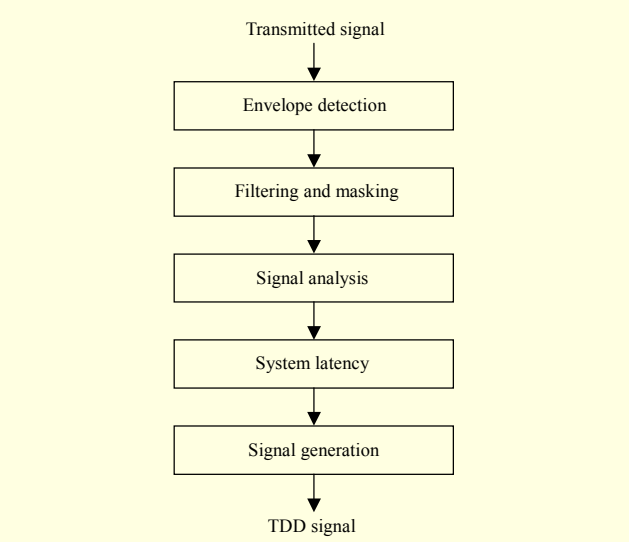


Fig. 3. Proposed procedure for TDD signal generation.

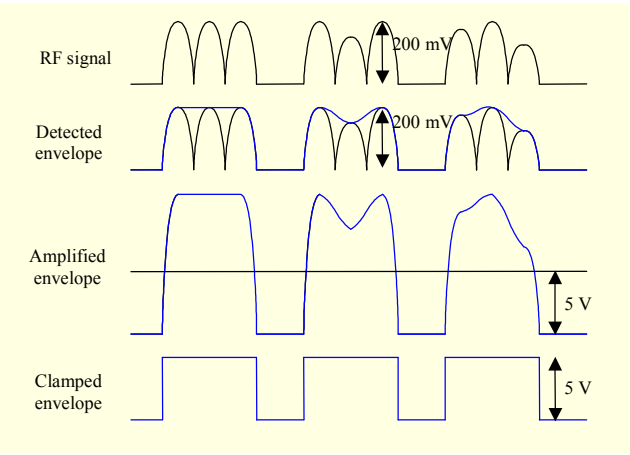


Fig. 4. Principle of envelope detection using clamping.

III. Proposed Synchronizing Method

In this section, an algorithm to detect a TDD signal from an RF or IF signals is proposed. The entire procedure consists of envelope detection, filtering and masking, signal analysis, system latency, and signal generation, as illustrated in Fig. 3.

1. Envelope Detection

When an RF signal is received, TDD synchronizer detects an envelope with a relatively simple detection circuit and amplifies it with an operational amplifier. This procedure is illustrated in Fig. 4. If there is no fading, it is possible to detect stable synchronization signal even though noises are added to an RF signal by removing it during the amplification process. However, if RF signal is distorted too much by multipath fading, noise elements of the signal are also amplified. As the

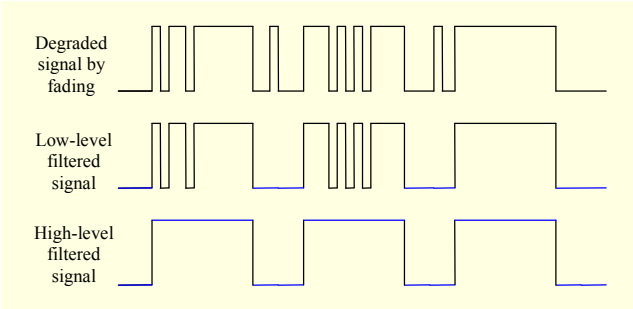


Fig. 5. Refinement of distorted signal using digital filtering.

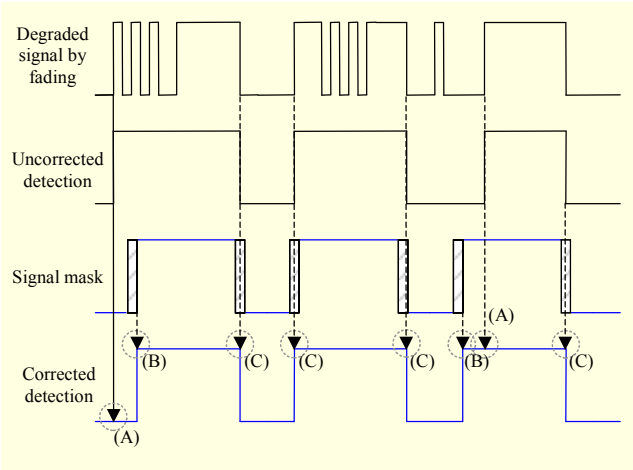


Fig. 6. Refinement of period and duration of TDD signal using mask.

result, the detected TDD signal becomes distorted. In this case, the original form of the distorted TDD signal should be restored by using a digital filter to obtain the reliable TDD signal.

2. Signal Shaping and Filtering

As described above, reliable TDD signals can be easily generated with an RF signal without fading by a detecting envelope using the clamping circuit configured with operational amplifier(s). However, with various fading conditions given, the signal is distorted, and it becomes impossible to generate reliable TDD signal with only a simple clamping circuit. Thus, this paper proposes and implements a digital processing method appropriate for such environment.

As shown in the first part of Fig. 5, when the signal is distorted by fading, a reliable UL region should be first estimated first through low-level filtering. For this, a 64-tap filter is used. Then, a reliable DL region should be estimated through high-level filtering. The combination of these filters is acquired experimentally. If the signal is distorted too much, as shown in the first figure in Fig. 5, however, it might be difficult

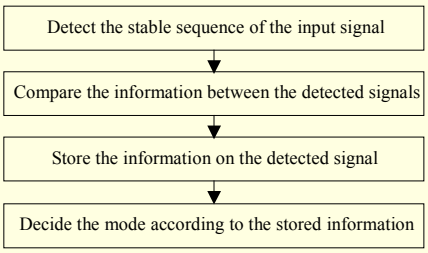


Fig. 7. Signal analysis algorithm.

to locate the start point of the TDD period or the position of the start point might not be constant. In other words, the generated TDD signal would look like as shown in the second figure in Fig. 6. For a solution to solve these problems, a region where signal change is allowed is established only where the change of TDD signal is allowed (as shown in the third part of figure in Fig. 6), only where the change of the TDD signal is allowed. In (A), the TDD signal is not changed. In (C) where the signal is changed in the allowable region, the signal is output. If the signal has not changed in the change-allowed region, the signal is changed by force at the same time when the change-allowable region ends as shown in (B). Through this procedure, a reliable period of TDD signal is estimated. The change-allowable region is set to 4 μs, so that the period change could be within 5 μs. This satisfies general WiBro service conditions.

3. Signal Analysis

The previous procedure is to detect the TDD signal. Then, it should be determined whether the detected TDD signal is valid information and, if it is valid, which mode it is. First, the TDD signal, which has been refined through filtering, masking and shaping, is checked for reliability. A check is also made to discover if there is a WiBro signal that can be reliably serviced. Second, a check is made as to whether or not there is any difference between the currently verified information and the one previously verified. If there is no difference, it means that the service environment is the same but if there is any difference, it means that there is a possibility of OFDM symbol rate change. Third, the information concerning the difference is stored. Finally, there is a check to see whether or not the stored information is actually a valid mode. If it is a valid mode, the corresponding mode information is transferred to the TDD signal generation process. In an area where multiple RASs are overlapped, and when the strength of WiBro RF signals are large enough and these signals are also overlapped, a constant symbol rate may occur even though it may not be a valid mode. Such an abnormal symbol rate should be prevented from occurring. The algorithmic flow of the signal analysis is shown in Fig. 7.

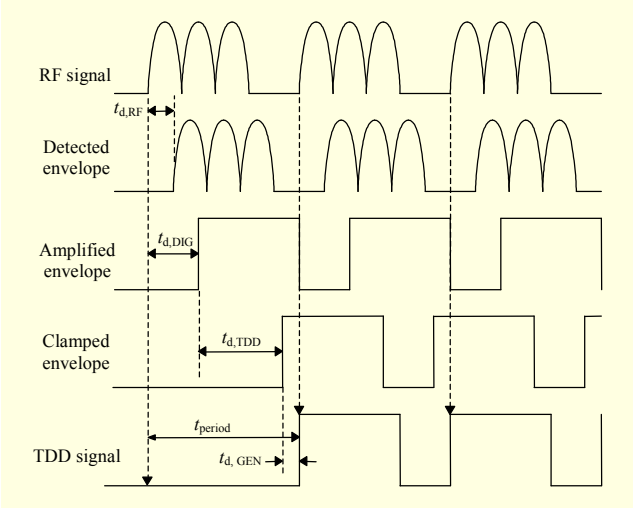


Fig. 8. System latency time.

4. System Latency

Because the RF circuit and TDD synchronizer have different latency times of their own, the generated TDD signal cannot be directly inputted to the RF circuit. In consideration of the latency times of these two systems, the TDD signal should be delayed for a certain time before being inputted to RF circuit. The delay time to be applied to the TDD signal is defined in (1) and illustrated in Fig. 8.

$$t_{d,TDD} = t_{period} - (t_{d,DIG} - t_{d,RF}) - t_{d,GEN}\ , \qquad (1)$$

where $t_{d,TDD}$ is the delay time for TDD signal, t_{period} is the period of TDD signal which is 5 ms, $t_{d,DIG}$ and $t_{d,RF}$ are time delays by the digital circuit and RF circuit, respectively. The former is caused by envelope detection, filtering, masking, and signal analysis, which is relatively longer than $t_{d,RF}$. $t_{d,GEN}$ is the delay time to be made at the time of signal generation, which is considered in $t_{d,TDD}$ in advance.

5. Signal Generation

The start point of the TDD signal, obtained in III.2, is delayed as much as the system latency described in III.4. Then, TDD signal is generated according to the mode information obtained in III.3. Even though another time delay is made in the process of TDD signal generation, it is considered beforehand in the system latency process. The waveform of the generated TDD signal is shown in Fig. 9.

Even though it is possible to generate a TDD signal for an input signal, it should not be generated if the level is lower than the one defined by the WiBro service specification. Because an RF system cannot perform a normal operation at an input level lower than the specification, the input of such a TDD signal will result in servicing the distorted signals.

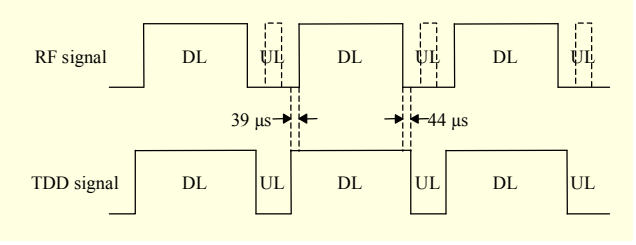


Fig. 9. Final TDD synchronization signal.

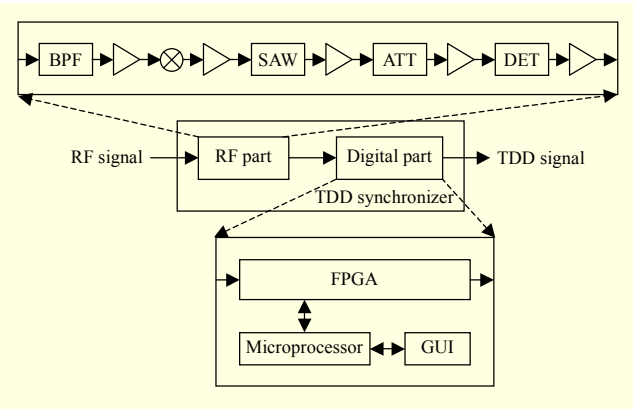


Fig. 10. Architecture of the proposed system.

IV. Proposed Hardware Architecture

This section describes the hardware architecture proposed in this paper.

1. Architecture of TDD Synchronizer

As shown in Fig. 10, a TDD synchronizer can be largely divided into an RF part and digital part. The RF part corresponds to the generally used RF block. It has a simple architecture that consists of a band-pass filter (BPF), a surface acoustic wave filter (SAW), a attenuator (ATT), a detector (DET), a mixer, and various amplifiers. The band-passed RF signal is amplified and is inputted to a mixer with the signal from a local oscillator. So the RF signal is converted to an IF signal. The attenuated IF signal is amplified in an amplifier, and the superfluous frequencies of the IF signal are restricted in the SAW. After the amplitude of the filtered IF signal is controlled by the ATT for the linear operation of the DET, the DC amplitude of the signal is generated in the DET. The DC value is transferred to the digital part through a envelope detector and an operational amplifier. Field-programmable gate array (FPGA) in the digital part is the main focus of this paper. In order to control the operation of the RF part and to interact with some of FPGA operations, microprocessor is used. However, as it hardly affects the hardware and algorithm proposed in this paper, it is not described here, but only the hardware

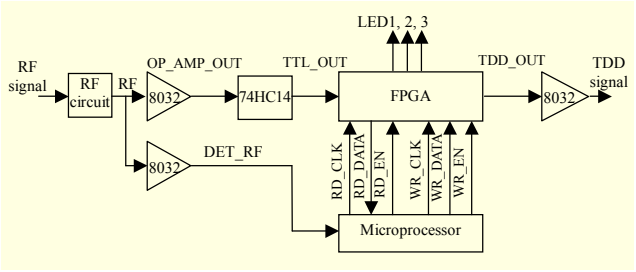


Fig. 11. Circuit placement of the proposed system.

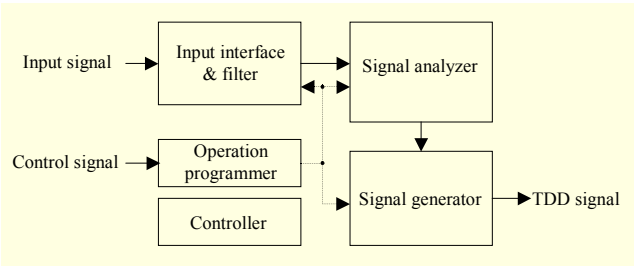


Fig. 12. Hardware architecture of digital part.

architecture designed by using FPGA is described.

Figure 11 shows how the proposed system architecture shown in Fig. 10 is implemented with actual circuit placement.

2. Hardware Architecture in FPGA

FPGA in the digital part is configured with 5 blocks as shown in Fig. 12: input interface and filter block that takes charge of input/output interface and digital filtering; signal analyzer that analyzes signals and detects their periods; signal generator that has system latency function and also generates TDD signals; operation programmer to program operating conditions; and controller to control all these blocks.

The digital part shown in Fig. 12 is illustrated in detail in Fig. 13. The input interface block is the module to receive the envelope signal that has been converted into a TTL signal. High-level and low-level filters filter logic-1 of the received signal that has been distorted to logic-0 back to logic-1, or refine logic-1 that has been distorted to logic-1 back to logic-0. The duration calculator calculates the period of logic-1 or logic-0 of the received signal that has been refined through the filtering process, and the level comparator compares the previously received signal information and the one currently received to identify whether the signals have the same period. After this comparison is made, the mode selector checks whether another regular mode is detected during a certain period of time, which is different from the previously detected mode. Next, the sync generator detects a synchronization signal for the current input signal by analyzing the input signal. If it fails to detect a synchronization signal or has detected a

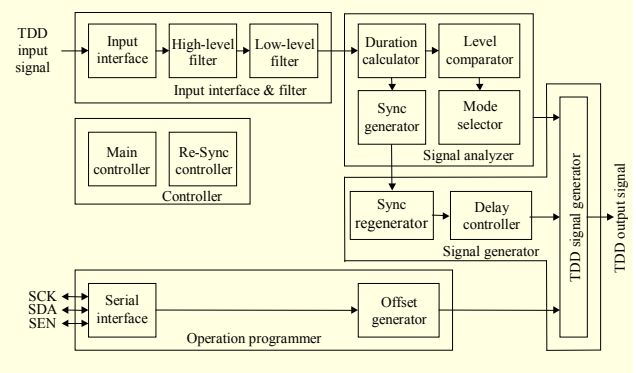


Fig. 13. Detail architecture of digital part.

wrong synchronization signal or detects a new synchronization signal. The delay controller delays the currently detected synchronization signal by generating as much delay time as defined. In addition, serial interface sends/receives various information through serial communication with the external processors, and offset generator generates signals to offset the errors caused by various environments inside/outside the circuit, by the external processor. Lastly, TDD signal generator generates TDD output signals based on the information and data obtained by several modules.

V. Implementation and Experimental result

1. Experimental Conditions

An experiment of the TDD signal generator proposed in this paper was conducted under the conditions given in Tables 3 and 4. Table 3 lists general WiBro communication conditions, while Table 4 summarizes the conditions of WiBro symbol and the actual period.

The environmental conditions of multipath fading are described in Table 5. Tables 3, 4, and 5 are based on the WiBro environment currently in service in Korea.

Table 3. Communication condition.

Item	Specification
Frequency range (MHz)	2,300 to 2,327
RF input range (dBm)	–80 to –50
Characteristic impedance	50 Ω
Switching accuracy (μs)	± 1
Switching time	TTG, RTG region
Switching stability with multipath fading (μs)	± 5
Output signal	TTL

Table 4. WiBro OFDM symbol and time (μs).

Symbols	1 Symbol	DL duration	TTG/2	RTG/2	Total
30	115.2	3,456	44	39	3,539
27	115.2	3,110			3,193
24	115.2	2,765			2,848

Table 5. Multipath fading condition.

ITU Pedestrian A speed 3km/h (PA3)		ITU Pedestrian B speed 3km/h (PB3)		ITU vehicular A speed 3km/h (VA30)		ITU vehicular A speed 3km/h (VA120)	
Speed for band I, II, III, IV, IX, X 3 km/h		Speed for band I, II, III, IV, IX, X 3 km/h		Speed for band I, II, III, IV, IX, X 30 km/h		Speed for band I, II, III, IV, IX, X 120 km/h	
Speed for band V, VI, VIII 7 km/h		Speed for band V, VI, VIII 7 km/h		Speed for band V, VI, VIII 71 km/h		Speed for band V, VI, VIII 282 km/h	
Speed for band VII 2.3 km/h		Speed for band VII 2.3 km/h		Speed for band VII 23 km/h		Speed for band VII 92 km/h	
Speed for band XI 4.1 km/h		Speed for band XI 4.1 km/h		Speed for band XI 41 km/h		Speed for band XI 166 km/h	
RD	RMP	RD	RMP	RD	RMP	RD	RMP
0	0	0	0	0	0	0	0
110	–9.7	200	–0.9	310	–1.0	310	–1.0
190	–19.2	800	–4.9	710	–9.0	710	–9.0
410	–22.8	1,200	–8.0	1,090	–10.0	1,090	–10.0
-	-	2,300	–7.8	1,730	–15.0	1,730	–15.0
-	-	3,700	–23.9	2,510	–20.0	2,510	–20.0

* RD: relative delay (ns), RMP: relative mean power (dB).

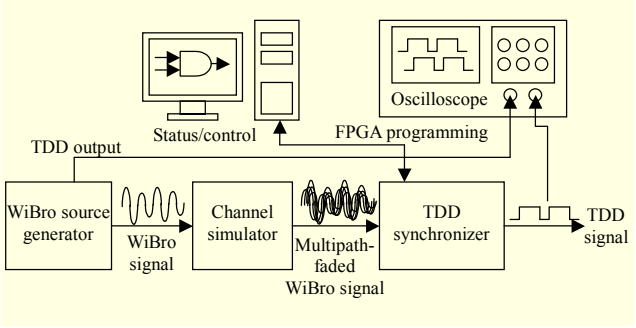


Fig. 14. Experimental environment.

Figure 14 illustrated the experimental environment to verify the system implemented in this paper. For a WiBro signal generator, Agilent's E4438C (WiBro) is used. As for the channel simulator to apply multipath fading conditions, Sprint's TAS4500 FLEX is used. TDD synchronization generator in Fig. 14 corresponds to the system implemented in this paper. The final TDD output signal is compared with the TDD reference signal (TDD output) from the signal generator.

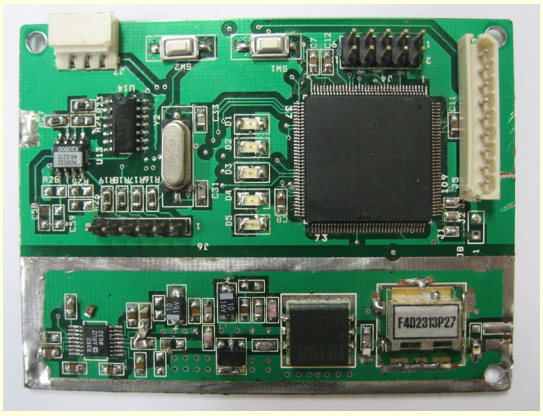
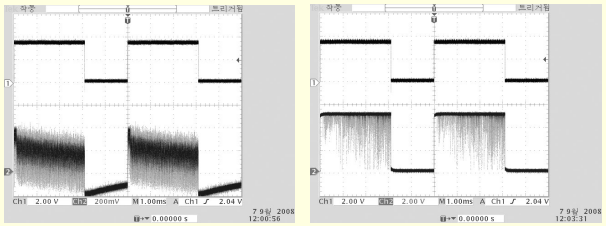


Fig. 15. Implemented integrated-system using PCB.



(a) (b)

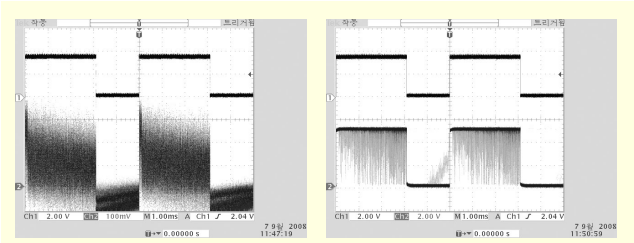
Fig. 16. Communication condition without multipath fading: (a) detected original envelope signal and (b) signal after amplification and clamping.

2. Implementation

For FPGA implementation, Altera's Cyclone EP1C3T144C6 device was used, and the hardware utilization rate was 2,641/2,910 (91%). The minimum clock cycle is 10.948 ns, and the maximum clock frequency is 91.34 MHz. Figure 15 shows PCB boards of the digital part and RF part implemented. The implemented board has the digital part and the RF system part on a single PCB, of which the bottom part corresponding to the RF part is wrapped with a metal cap for shielding.

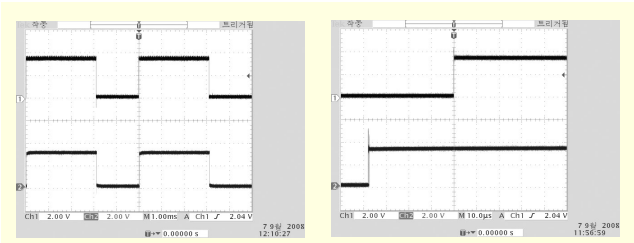
3. Experimental Result and Analysis

Figures 16 through 18 show the results obtained using the oscilloscope for operation of the implemented system. In all figures, the upper signals are the TDD reference signal generated by the signal generator. Figure 16 shows the result of operating the implemented system in the communication environment without multipath fading. Figure 16(a) shows the condition when the envelope signal is detected. According to the bottom figure of Fig. 16(a), the signal has the amplitude of 800 mV. When this signal is amplified and clamped, the signal



(a) (b)

Fig. 17. Communication condition with multipath fading (Ped_A PA3): (a) detected original envelope signal and (b) signal after amplification and clamping.



(a) (b)

Fig. 18. TDD synchronization signal output: (a) two periods and (b) RTG region.

shown in Fig. 16(b) is obtained. According to Fig. 16(b), the signal is actually distorted. Such signal distortion can be removed through filtering and masking.

Figure 17 shows the result of operating the implemented system in the communication environment with multipath fading. At the bottom of Fig. 17(b), it is shown that the signal is distorted much more than the signal in Fig. 16(a). Furthermore, although not expressed in the figure, the signal in Fig. 17(a) has as much fluctuation as 1 V at maximum, while the signal in Fig. 16(a) has an output. Therefore, when compared to each other, the actual experiment result shown in Fig. 16(a) greatly differs from that in Fig. 17(a). The result shown in Fig. 17(b) also shows that the signal has much more distortion than the result shown in Fig. 16(b). Particularly, it is shown that a large noise element is inserted in the UL region. Because of this noise element, it is not easy to distinguish DL regions from UL regions in the multipath fading environment. However, when filtering and masking proposed in this paper are applied, it is possible to detect a reliable TDD signal as shown in Fig. 18, even under the communication conditions shown in Figs. 16 and 17. Figure 18(a) shows a TDD signal generated through the implemented system, while Fig. 18(b) shows that in the RTG region, the TDD signal is exactly 39 μs faster than the original signal.

The test result is detailed in Table 6. In conclusion, the result proves that the implemented system can fully satisfy the conditions of WiBro services under various environments. In each multipath fading condition, the initial synchronization was

Table 6. Experimental result of TDD synchronization detection.

Fading condition		Veh_A VA120	Veh_A VA30	Ped_A PA3	Ped_B PB3
Input level (dBm)		–80	–80	–80	–80
First sync. detect (s)		< 2	< 2	< 3	< 3
Stability (μs)		± 5	± 4	± 3	± 2
Adjust accuracy (μs)		1	1	1	1
Desyncronization (s)		< 3	< 3	< 3	< 3
Resyncronization (s)		< 3	< 3	< 3	< 3
Symbol rate change	30	3,539	3,539	3,539	3,539
	27	3,193	3,193	3,193	3,193
	24	2,848	2,848	2,848	2,848
Min input level (dBm)		–90	–90	–90	–90

acquired within 3 s and the stability of maximum ±5 μs to minimum ±2 μs as obtained, which could be adjusted at a precision of 1 μs in each condition. Even when the number of OFDM symbols changed, the implemented system adaptively responded to the synchronization change and accurately restored its period. As the minimum synchronization acquisition level was –90 dBm, it was possible to fully satisfy the minimum input level that WiBro RF repeater should have, which is –80 dBm.

The level where the implemented system could consistently perform detection of the synchronization signal was –90 dBm. The level that the system could maintain the synchronization after detection was –100 dB. Although the initial synchronization acquisition time was measured to be about 3 s, it was during this 3 s in which the delay by the source generator on/off was considered. When the input level was –80 dBm and there was no fading, the detected TDD signal maintained the stability of ±1 μs. In the communication environment with fading, it could maintain the stability of ±2 μs. If the WiBro signal is lost or its level becomes very low, the implemented system analyzes the signal for about 5 s and then stops generating the TDD signal. When the DL symbol changes, TDD synchronization for the changed symbol is detected about 1 to 2 s later, and thus, the mode changes.

Figure 19 shows that the test environment verifies the implemented system. As there has been no research that proposed to detect a TDD signal of WiBro which used it as synchronization signal for the repeater and implemented it with the hardware, it was not possible to compare the performance of the proposed and implemented system with another. However, it has been shown that TDD signals can be provided to a WiBro RF home repeater at a moderate cost if the

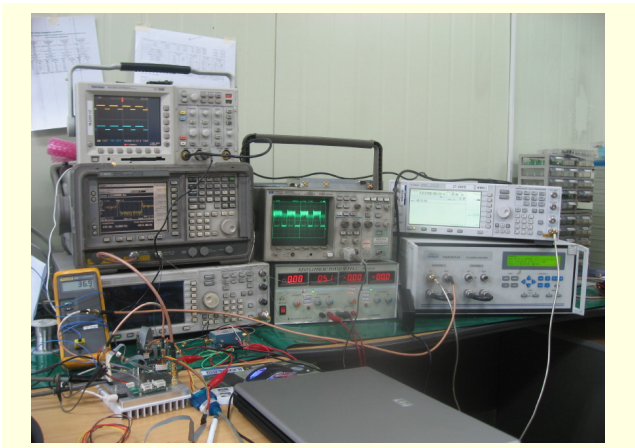


Fig. 19. Test environment.

implemented system is used.

VI. Conclusion

This paper proposed a method of synchronization between base station and DL, UL, and idle period signals in TDD-based WiBro RF repeater. In addition, it implemented a system in which RF and digital parts were integrated. It also proposed an algorithm to detect and amplify the envelope signal of a DL signal, restore the signal distorted by the wireless channel environment by refining and filtering, and then acquire a TDD signal. The digital circuit was implemented using Altera's Cyclone EP1C3T144C6 FPGA. It showed a hardware utilization rate of 2,641/2,910 (91%) and was capable of operating at a maximum frequency of 91.34 MHz. According to experimental results, the implemented circuit satisfied all the specifications for the WiBro communication environment currently in service. The proposed system needs less number of parts than the existing systems. This means that having relatively lower costs for implementation, it is highly economical. In addition, if IF signal can be supplied stably through a WiBro RF repeater, there would be no need for an RF circuit in the proposed system, which reduces the cost even more. Therefore, it is expected that it could be used as an essential part in the Wibro RF repeater field.

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