High-Gain Double-Bulk Mixer in 65 nm CMOS with 830 µW Power Consumption

Kurt Schweiger and Horst Zimmermann

A low-power down-sampling mixer in a low-power digital 65 nm CMOS technology is presented. The mixer consumes only 830 µW at 1.2 V supply voltage by combining an NMOS and a PMOS mixer with cascade transistors at the output. The measured gain is (19 ±1 dB) at frequencies between 100 MHz and 3 GHz. An IIP3 of –5.9 dBm is achieved.

Keywords: Down-sampling mixer, low power, nanometer CMOS, bulk mixer.

I. Introduction

In modern radio receivers, especially in mobile devices, it is important to have very low-power consumption to extend the battery lifetime. The analog frontend of a radio receiver consists of a low-noise amplifier, a mixer, and a filter before the digital baseband processing. The fast development of multi standard receivers and digital CMOS technology leads to the needs of analog circuits in digital nanometer CMOS technology. The poor transistor characteristics in those technologies give more challenges for analog designers, for example, low supply voltage and high threshold voltages. This letter focuses on the down-sampling mixer in the receiver chain which down-converts the high frequency signal into baseband. The mixer is one of the key building blocks of every receiver and is also often the limiting part for good performance. A new circuit is presented in the next section to achieve a high gain in the mixer itself while operating with very low power consumption.

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II. Circuit Description

A novel circuit for an active mixer, based on a single-bulk mixer [1]-[4], is proposed. The RF signal is connected to the gates, and the LO frequency is connected to the bulk (wells, back-gates) of the input transistors or vice versa. The bulk-driven mixer uses the body effect of the MOS transistors to achieve the frequency transformation through modulating the threshold voltage of the input transistors.

$$V_{\mathrm{th}} = V_{\mathrm{th0}} + \gamma \cdot \left[\sqrt{2\Phi_{\mathrm{f}} + V_{\mathrm{SB}}} - \sqrt{2\Phi_{\mathrm{f}}} \right]. \qquad (1)$$

In [1]-[4], the tail current source was removed to gain more voltage headroom for the mixer operation and allow for a low supply voltage.

The schematic of the proposed double-bulk mixer is shown in Fig. 1. The operation principle of the double-bulk mixer is based on two complementary mixers. The additional PMOS

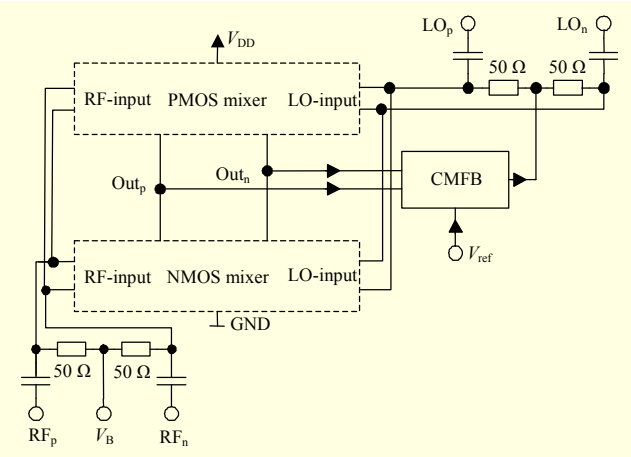

Fig. 1. Schematic of the proposed double-bulk mixer with common-mode feedback.

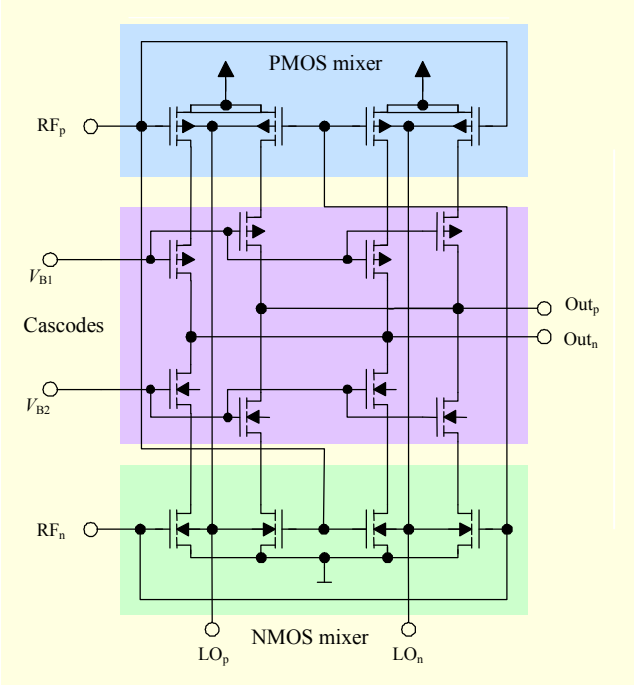

Fig. 2. Schematic of the mixer including the cascode stage.

mixer operates as the active load of the NMOS mixer, and the NMOS mixer forms the active load of the PMOS mixer. Thus, the bias current through the circuit is used in both mixers, and their transconductances add up to generate the down converted output signal. To enhance the gain of this simple double-bulk mixer, which has a relatively low gain due to its low bias current, cascode stages were added. The trade-off between lower IF bandwidth, caused by the cascade, and conversion gain is acceptable in narrowband applications. The details of the circuit schematic are shown in Fig. 2. The RF input is applied to the gate at both mixer stages, while the clock signal LO is applied to the bulk terminals of both mixer stages. Both signals are differential. The LO is applied to the bulk to achieve a high gain in the circuit. The bulk connection is done in the layout with a ring-contact around the entire transistor. This is possible for both NMOS and PMOS in the used triple-well technology.

A common mode feedback, which senses the output common-mode voltage, is necessary to keep the bias condition of the circuit constant within process corners and operation temperature range. The common-mode feedback utilizes an NMOS differential amplifier with PMOS current mirror load. The common mode feedback is dynamically adjusting the DC bias level of the clock input.

The adjusted DC bias voltage of the LO signal controls the gate voltage of the input transistors to a level to keep the bias current constant and the output voltage at $V_{DD}/2$. The DC voltage at the RF input applied to the bulk can be adjusted externally via an additional pin V_B.

III. Results

The mixer with an active area of 120 μm×180 μm was fabricated in a 65 nm triple-well low-power digital CMOS technology with the threshold voltages V_{tn}=0.5 V and V_{tp}= 0.4 V.

Figure 3(a) shows the layout plot of the fabricated chip. For measurement purposes, a printed circuit board (PCB) was designed where the chip was directly bonded. The differential input signals were created with off-chip baluns. Gain measurements were performed at a clock frequency of 1.5 GHz with an RF signal at 1.501 GHz which generates a down converted signal at 1 MHz. A gain of 19 dB was measured with the nominal supply voltage of 1.2 V with a power consumption of 830 μW.

Gain measurements at different supply voltages have been performed as well. The results show a slightly higher conversion gain (21 dB) at 1.1 V, and the mixer still operates at 0.8 V with a conversion gain of 11 dB. Those results are shown in Fig. 4(a).

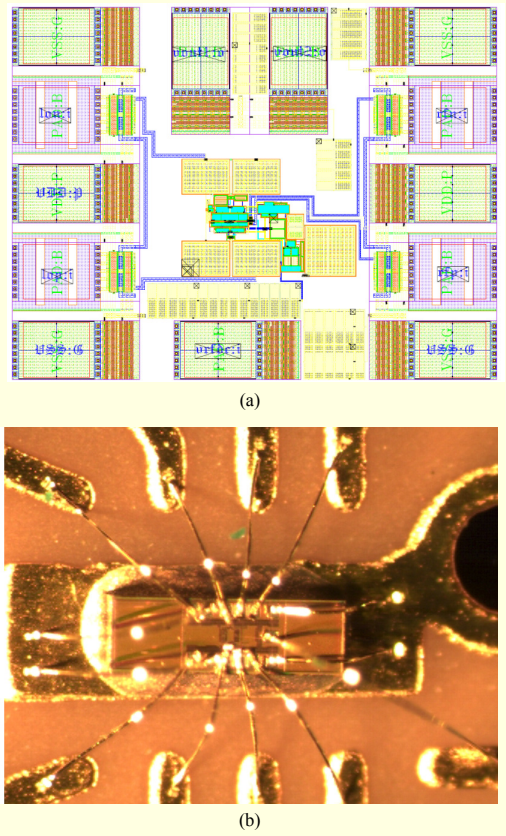

Fig. 3. (a) Layout plot and (b) photograph of the fabricated chip bonded to the measurement board.

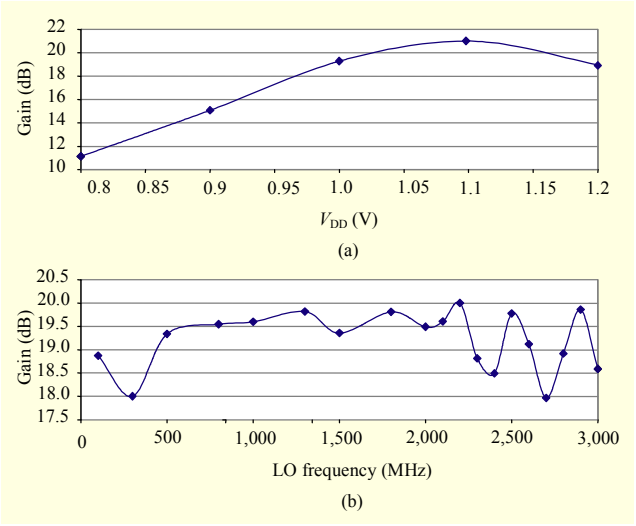

Fig. 4. Measurement results: (a) gain versus supply voltage at 1.5 GHz and (b) gain versus clock frequency (V_{DD}=1.2 V).

Measurements at different clock frequencies were also performed with a constant IF-frequency of 1 MHz at a V_{DD} of 1.2 V. The circuit shows a gain of 19 dB ±1 dB between 100 MHz and 3 GHz. The measurement results are shown in Fig. 4(b). Measurements above 3 GHz could not be performed because of the available signal generators. Simulations show that the mixer can work up to 7 GHz with a gain decrease of 3 dB. Noise simulations show an input referred noise of 12.9 nV/√Hz for the bandwidth from 500 Hz to 4 MHz. The 1/f noise corner frequency is 200 kHz.

Linearity measurements were done with two input signals that are spaced 10 kHz apart. The close proximity of the signals ensures the 3rd order harmonics to appear in-band of the output. Extrapolation of the wanted signal and the distortion lead to an input referred intercept point of 3rd order at –5.9 dBm.

IV. Comparison

In Table 1, a comparison is given of our work with previous work. References [1], [4]-[6] show simple-bulk mixer realizations. They all show low-power consumption, but also relatively low gain. The proposed double-bulk mixer structure achieves a considerably higher gain compared to the simple-bulk mixer implementations with lower power consumption.

Table 1. Comparison with other works.

Reference	V_{DD}	Power	Gain	IIP3	Technology
[1]	1 V	1 mW	13 dB	–4 dBm	0.18 µm
[4]	1.2 V	670 µW	–2 dB	8 dBm	65 nm
[5]	1.2 V	1.8 mW	3.2 dB	–2.1 dBm	90 nm
[6]	0.77 V	480 µW	5.7 dB	–5.7 dBm	0.18 µm
This work	1.2 V	830 µW	19 dB	–5.9 dBm	65 nm

V. Conclusion

A double-bulk mixer was designed and fabricated with a low-power digital 65 nm CMOS technology. The circuit concept is based on two mixers using the same current for higher gain at a low current consumption. Measurement results show a high gain of 19 dB over a frequency range of 3 GHz. The circuit is also operational at a supply voltage of 0.8 V with a lower gain. Linearity measurements show an IIP3 of –5.9 dBm. The power consumption at the nominal supply voltage of 1.2 V is only 830 µW.

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