Temperature-Adaptive Back-Bias Voltage Generator for an RCAT Pseudo SRAM

Jong-Pil Son, Hyun-Geun Byun, Young-Hyun Jun, Kinam Kim, and Soo-Won Kim

In order to guarantee the proper operation of a recessed channel array transistor (RCAT) pseudo SRAM, the back-bias voltage must be changed in response to changes in temperature. Due to cell drivability and leakage current, the obtainable back-bias range also changes with temperature. This paper presents a pseudo SRAM for mobile applications with an adaptive back-bias voltage generator with a negative temperature dependency (NTD) using an NTD VBB detector. The proposed scheme is implemented using the Samsung 100 nm RCAT pseudo SRAM process technology. Experimental results show that the proposed VBB generator has a negative temperature dependency of –0.85 mV/℃, and its static current consumption is found to be only 0.83 μA@2.0 V.

Keywords: Pseudo SRAM, memories, RCAT, temperature, back-bias voltage generator.

I. Introduction

Recently, the density of memories for mobile applications has continuously increased with the downward scaling of process technology, but there is still a need for less power consumption and simultaneously, higher operating speed. Further scaling of the process causes short channel effects in the cell transistors and increases their leakage currents. This increased leakage makes the data retention time shorter and makes the memory consume more power. The pseudo SRAM is a memory for mobile applications using the SRAM interface with the 1T or 2T cell array of DRAM instead of the 6T SRAM cell array. Using a DRAM cell array makes the die size small and reduces the cost. However, it also requires hidden refresh operations and lower standby current because it uses the SRAM interface. The recessed channel array transistor (RCAT) pseudo SRAM that has been generally used in recent years has the advantages of lower leakage and scalability compared to the planar transistor RAM [1]-[3]. Even though the RCAT process reduces the leakage drastically, it still has several kinds of leakage that should be considered to determine the data retention time. Using the RCAT process, the cell drivability (cell saturation current) should also be considered because the source and drain contacts are made narrow to prepare for the worst case of gate misalignment. This produces complications such as a read/write failure which restricts the bandwidth of DRAM. This contact resistance increases continuously with the process scaling.

The back-bias voltage (VBB) is generated by the VBB generator and supplied to the pseudo SRAM's substrate. It heightens the reverse bias of the p-n junction between the source and the substrate, which is applied to lower the drain-to-source leakage.

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Unfortunately, a high reverse bias also reduces the cell drivability by increasing the threshold voltage of the cell transistor. Temperature is another factor that can affect both leakage and cell drivability, so the VBB level must be limited in order to guarantee the retention time and high speed operation over the operating temperature range (–30°C to 100°C).

There have been many studies that have focused on the optimization of the VBB generator [4]-[6], but they have concentrated on improving the efficiency of the VBB generator itself. In [7], the VBB generator was considered according to the temperature from the view point of the latch up, but the VBB level cannot be controlled accurately by the oscillator without the detection of its level.

This paper presents a pseudo SRAM for mobile applications with a simple temperature-adaptive VBB generator that guarantees the proper operation of the memory over the operating temperature range.

In section II of this paper, the leakage characteristics of the recently developed RCAT pseudo SRAM are shown along with the temperature dependency of these characteristics. This section also describes the write operation (which is affected by the VBB level), and a suitable VBB level for guaranteeing the write operation is revealed.

Section III proposes a temperature-adaptive VBB generator using the transistor's mutual compensation of mobility and threshold voltage temperature effect.

II. Dynamic Refresh and Operation of the RCAT Pseudo SRAM

1. Leakage of the RCAT Pseudo SRAM

The recessed channel array transistor (RCAT) is widely used to make pseudo SRAM cells in processes on a scale under 100 nm. By etching the channel area and supplying a longer effective channel length, the subthreshold leakage due to the short channel effect can be substantially reduced. Figure 1 shows the major leakage paths of the RCAT pseudo SRAM. They consist of the subthreshold leakage (I_{sub}) through the channel, the PN junction leakage from the cell node to the substrate, and the gate induced drain leakage (GIDL) that is caused by the strong electric field between the gate (biased low) and the drain (biased high). The p-n junction leakage is not a serious leakage source compared to the GIDL in the Samsung RCAT DRAM process [1].

In the GIDL, if the voltage between the drain and the gate is kept low (such as 1.4 V), its leakage would constitute a small portion of the total leakage and doesn't significantly affect the retention time [7]. These two leakages determine the static

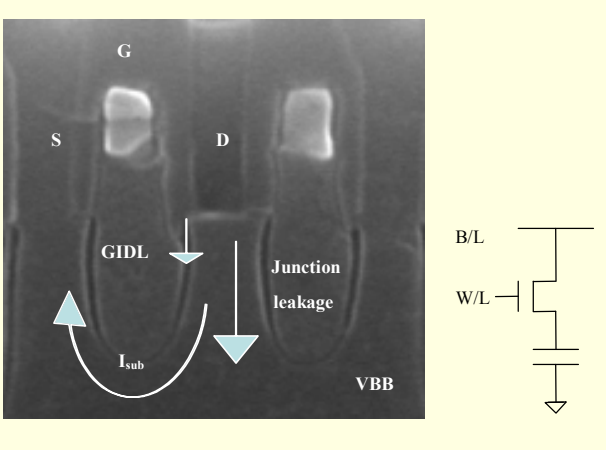


Fig. 1. Major leakage paths of the RCAT pseudo SRAM cell.

refresh time of the pseudo SRAM in its quiescent state with no read or write operations.

The dynamic refresh time of the pseudo SRAM with frequent operations is determined by the subthreshold leakage (I_{sub}). There is a ground bounce due to the charge from the bitline in the short operating cycle. This ground bounce is transferred to the unselected wordline that is connected to the same ground potential, and the stored cell data will be discharged by the subthreshold leakage. It is difficult to quantify the ground bounce accurately because it depends on the complicated ground net status of the memory cell array among many other factors. Therefore, the easiest way to improve the dynamic refresh is to reduce I_{sub}.

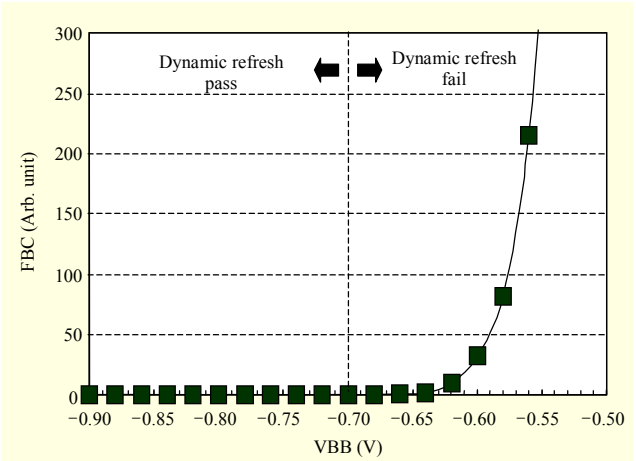
I_{sub} is given as

$$I_{\text{sub}} = \frac{W_{\text{eff}}}{W_{\text{o}}} I_{\text{o}} \times 10^{(V_{\text{gs}} - V_{\text{th}})/S}, \quad (1)$$

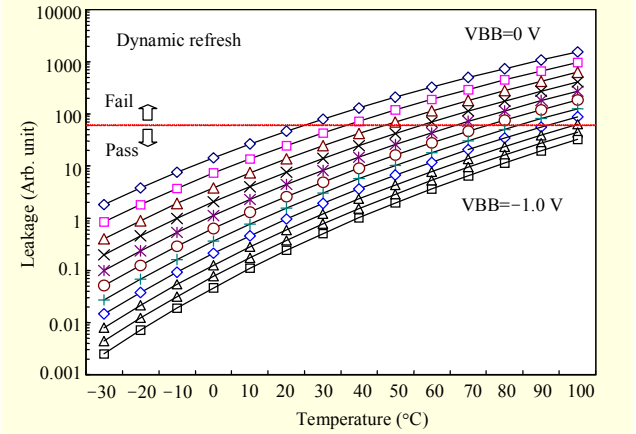
where W_{o} is the reference channel width, I_{o} is the reference current level to determine the threshold voltage, W_{eff} is the effective channel width, and S is the subthreshold swing parameter. I_{sub} can be reduced by raising the threshold voltage in (1) [8].

The threshold voltage is affected by the back-bias voltage and temperature. At a fixed temperature, the threshold voltage increases with an increase in the reverse bias between the source and the substrate because a high reverse bias makes it difficult to form the inversion layer in the channel area. In contrast, at a fixed VBB, the threshold voltage decreases as the temperature increases because of the bandgap of silicon; the Fermi level and intrinsic potential are changed as well [9].

Figure 2 shows the measured fail bit count (FBC) of the dynamic refresh and the simulated I_{sub} versus VBB and temperature using the Samsung 100 nm RCAT pseudo SRAM process. The FBC of the dynamic refresh increases as the magnitude of VBB decreases because I_{sub} also increases as the



(a) Measured FBC of the dynamic refresh versus VBB@100°C



(b) Subthreshold leakage versus VBB and temperature (simulation)

Fig. 2. Dynamic refresh and leakage characteristics as a function of temperature for various VBB levels using Samsung 100 nm RCAT pseudo SRAM process.

magnitude of VBB decreases. Figure 2(a) shows that the actual critical level of VBB is –0.7 V@100°C. Figure 2(b) shows that I_{sub} decreases almost exponentially as the temperature decreases and the magnitude of VBB increases. So, the magnitude of VBB can be decreased (that is, VBB can become less negative) if the amount of I_{sub} at a given temperature does not exceed I_{sub}@100°C with –0.7 V VBB, which is the critical level that is known from Fig. 2(a). The simulation shows that VBB can be raised above 0 V at 25°C, but in practice it is limited to 0 V to avoid a forward bias between the source and the substrate of MOSFET.

2. High Speed Write Operations of the RCAT Pseudo SRAM

Using the Samsung 100 nm RCAT pseudo SRAM process, the source and drain contacts should have enough space from the gate to prepare for the worst case of gate misalignment. Due to the reduced feature size of the contact, its resistance (R_c) is inevitably higher. The increase of this resistance reduces the cell drivability, so it is difficult to operate the pseudo SRAM in a short clock cycle while satisfying the timing specifications. In practice, the high speed write time is a bottleneck in the pseudo SRAM operations with such a weak cell. When a write command is asserted during the active state, the data of the I/O line is transferred to the accessed bitline by the column select signal and then the bitline starts to write the data into the cell node through the cell transistor. This write operation speed depends on the CLK frequency, so the weak cell cannot finish writing the cell data from the bitline on time with a higher CLK frequency. The write operation is one of the major items that restrict the pseudo SRAM operation at a high CLK frequency. High frequency write operation failures are particularly liable to happen at cold temperatures because the threshold voltage of the cell transistor goes up and the cell drivability weakens at cold temperature.

There are some methods to enhance the cell drivability at cold temperatures. The first method consists of pumping the wordline voltage to a higher level, but this may create a reliability problem such as a break in the gate oxide layer or drivability degradation by hot carrier injection. Another method is to lower the reverse bias between the source and the substrate. By doing this, the inversion layer between the drain and source is easily formed and the threshold voltage can be lowered, so the cell drivability can be enhanced.

Figure 3 shows the simulation results for the cell drivability as a function of the temperature and VBB. If there are no differences in the wordline level and the wordline enable time between the hot and cold temperatures, then the cell drivability must be kept constant for the operating temperature range (–30°C to 100°C) in order to prevent write operation failures caused by weak cell drivability. The VBB level at which the pseudo SRAM's cell drivability permits write operations with a high CLK frequency is no more than –0.8 V at 100°C. However this level should not be fixed at –0.8 V for operation at 0°C. The VBB level at 0°C for safe write operations is beyond at least –0.72 V. In order to guarantee the success of the high speed write operation over the operating temperature range, the VBB level must have a negative temperature dependency.

Figure 4 shows that the allowable VBB range is restricted by both the dynamic refresh and the high speed write operation using the Samsung 100 nm RCAT pseudo SRAM process. This range is marked as 'Pass' for the operating temperature range. The upper limit is set by the failure of the dynamic refresh. It is discussed in section II and shown in Fig. 2(b). The lower limit is determined by the cell drivability variations according to the temperature. It is discussed in section III and illustrated in Fig. 3, which shows the VBB level enabling the high speed write operation of the pseudo SRAM. So, it is not

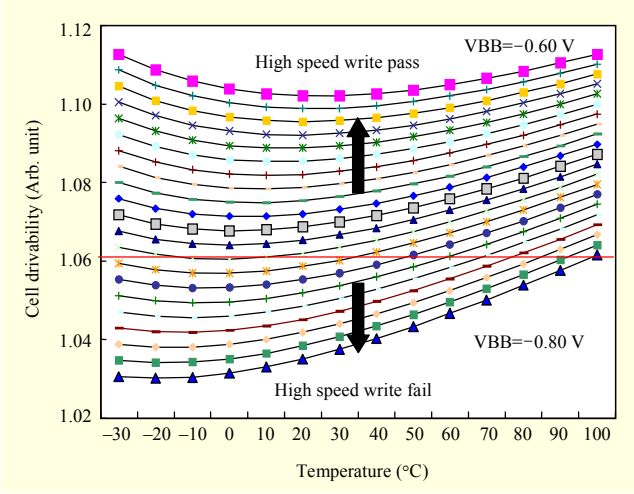


Fig. 3. Cell drivability variations as a function of the temperature and VBB using the Samsung 100 nm RCAT pseudo SRAM process (simulated).

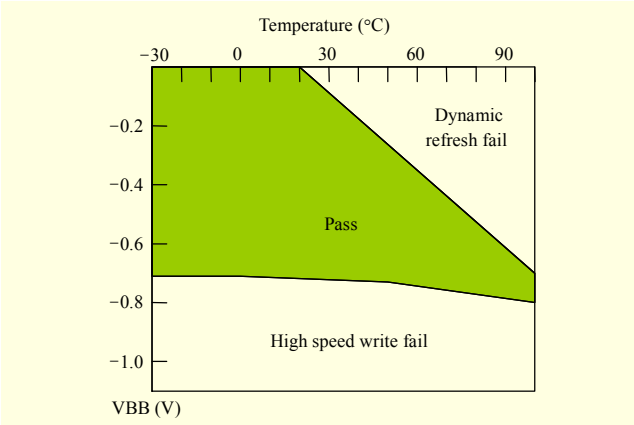


Fig. 4. Allowable VBB range for the operating temperature range.

necessary for the VBB generator to show the same temperature dependency of NMOS. We have only to set the VBB level between the upper limit and lower limit.

As an example, the VBB level must be set to more than –0.8 V and less than –0.7 V at 100°C, and it must be set to more than –0.72 V and less than 0 V at 0°C to avoid a dynamic refresh failure and a high speed write operation failure.

The allowable VBB range for guaranteeing the write operation therefore has a negative temperature dependency that is estimated at roughly –0.8 mV/°C using the Samsung 100 nm RCAT pseudo SRAM process.

III. Temperature Adaptive VBB Generator

1. VBB Generator Structure

The previous section illustrated the allowable VBB range

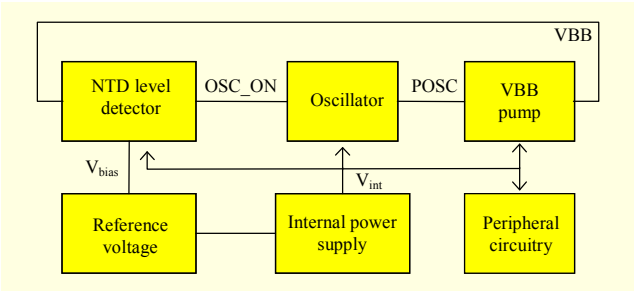


Fig. 5. Block diagram of the proposed VBB generator with the NTD level detector.

that satisfies both the dynamic refresh and the high speed write operation. From this result, the VBB level must have a negative temperature dependency to guarantee the success of the write operation. In order to realize this negative temperature dependency, this paper presents a simple VBB generator having a negative temperature dependency (NTD) level detector.

Figure 5 shows the block diagram of the proposed VBB generator. The NTD level detector compares the present VBB level with the target level and produces the output signal OSC_ON. This output signal can be '1' only if the present VBB is higher than the target level, which means that the present VBB does not reach the target level. The OSC_ON signal wakes up the oscillator and generates the POSC signal to enable the VBB pump to draw down the present VBB level. This consecutive operation of the VBB generator is stopped when the VBB level reaches the target level.

The process variations must be considered for the VBB generator. In this paper, we use fusing methods after a chip test and do not use an additional process compensation circuit [10] which consumes more power. This circuit requires additional compensation circuits to compensate its own PVT variations.

2. Temperature Dependency of the MOSFET

The long channel PMOSFET's source-to-drain current (I_{sd}) in the saturation region is given by [11]

$$I_{sd} = \frac{\mu_P C_{OX}}{2}\frac{W}{L}(V_{sg} - V_{tp})^2. \quad (2)$$

In this paper, we used the long channel PMOSFET to give immunity from the short channel effect and process variations and Shockley's MOSFET model is used for analysis instead of the alpha-power law model [12].

Carrier mobility and the threshold voltage are well known functions of temperature. Within the operating temperature range (–30°C to 100°C), the carrier mobility tends to decrease as the temperature increases because of the increased phonon scattering effect. Its relation with the temperature is given by the proportional equation $\mu \propto T^{-3/2}$.

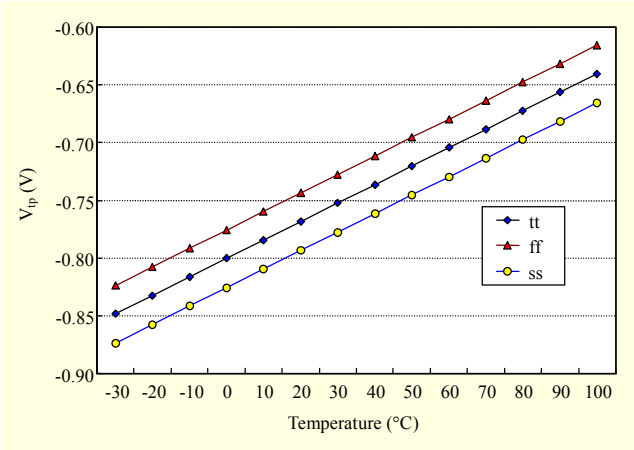


Fig. 6. Temperature dependence of the threshold voltage of PMOSFET for different corner conditions (length= 10 μm).

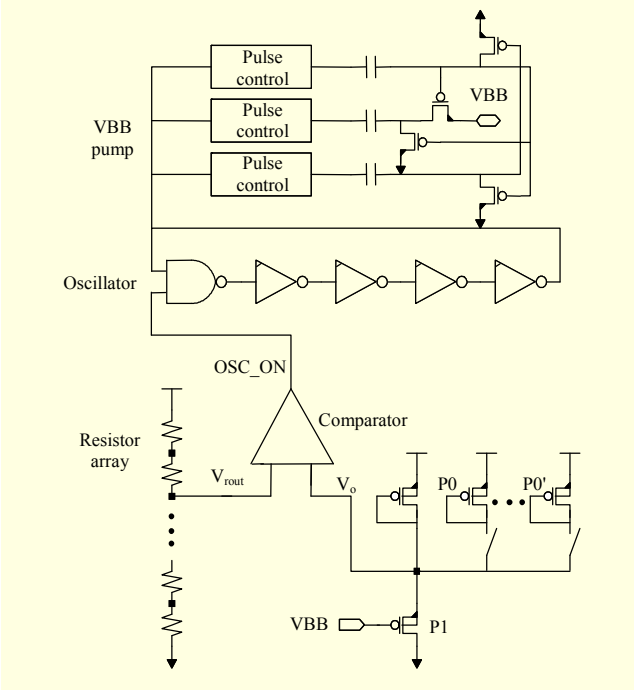


Fig. 7. Simplified VBB generator with negative temperature dependence level detector.

The temperature dependency of the threshold voltage is mainly related to the temperature dependency of the bandgap of silicon (*Eg*), and the difference between the Fermi potential and the intrinsic potential (ψ_B). These factors show different temperature dependencies for different doping concentrations. Typically, the total temperature dependency of the threshold voltage is inversely proportional to the temperature over the operating temperature range and given as

$$V_{tp}(T) = V_{tp_0} - \alpha_P (T - T_0), \quad (3)$$

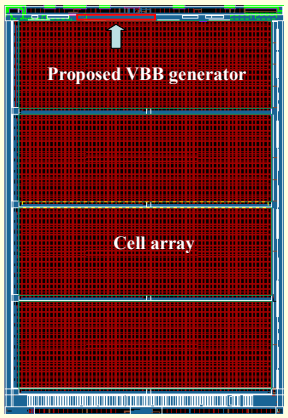


Fig. 8. Layout of the 256 MB pseudo SRAM using the Samsung 100 nm RCAT pseudo SRAM process technology.

where α_P is nearly constant [9], [13].

Figure 6 shows the temperature dependency of the threshold voltage of the process. The threshold voltage decreases almost linearly with the temperature increase. From the result, α_P is found to be 1.61 mV/℃ and shows good immunity from the process variations as shown in Fig. 6.

3. NTD Level Detector

From the previous section, we find that the temperature dependency of the MOSFET's saturation current is changed by the carrier mobility and threshold voltage. If the effect of the carrier mobility variation could be eliminated, the threshold voltage would be a dominant factor which determines the total temperature dependency. By using this characteristic, we proposed the simple NTD level detector.

Figure 7 shows the VBB generator with a simplified NTD level detector.

The first stage's output (V_o) is a diode connected to MP0, and the substrate bias (VBB) is connected to MP1. This output is then compared with the other output (V_{rout}) which is determined from the resistor array. The comparator compares these two outputs and generates the signal, OSC_ON, which enables the oscillator when V_o is higher than V_{rout}. Both MP0 and MP1 in the first stage are long channel transistors and must operate in saturation mode. The VBB can be obtained from (2), so it can be given as

$$VBB = V_o - T_{tp} - \gamma(V_{dd} - V_o - V_{tp}), \quad (4)$$

where the beta ratio

$$\gamma = \sqrt{(\mu_P C_{OX} W_0 / L_0)/(\mu_P C_{OX} W_1 / L_1)} = \sqrt{\beta_0 / \beta_1} \text{ and } V_o = V_{rout},$$

when the OSC_ON turns to '1.' From (4), the variation of the carrier mobility can be neglected, and the variation of the

threshold voltage can only change the VBB level among the process variations.

To obtain the temperature dependency of the VBB, (4) is differentiated by the temperature and given as

$$\frac{\partial VBB}{\partial T} = \alpha_P(1-\gamma), \quad (5)$$

where α_P is a coefficient from (3).

From (5), the temperature dependency can be controlled by changing the beta ratio. In order to change this beta ratio, we connect or disconnect the dummy identical transistor (MP0') to the output of the first stage. This switching method is very important because the allowable VBB range can be changed after the chip test.

So, we can obtain enough temperature dependency of the VBB by changing the beta ratio. It is also required that the V_{rout} be changed to set the target VBB given from (4). The proposed scheme has a laser fusing method to tune the V_{rout} after the chip test.

The following oscillator generates the POSC signal so as to enable the VBB pump which then pumps down the VBB level until the target level is reached.

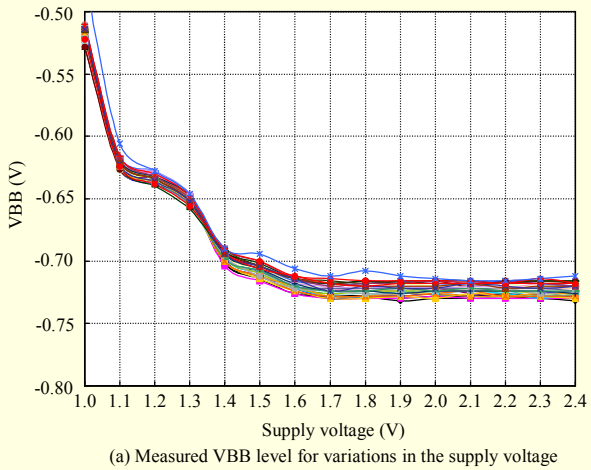
IV. Experimental Results

The proposed NTD VBB generator is implemented on a 256 MB pseudo SRAM for mobile applications with the Samsung 100 nm RCAT pseudo SRAM process technology. Figure 8 shows the layout of the total pseudo SRAM chip, whose area is 5,125 μm × 7,507 μm. The proposed NTC VBB generator occupies 1,350 μm × 43.5 μm including the VBB pump circuit.

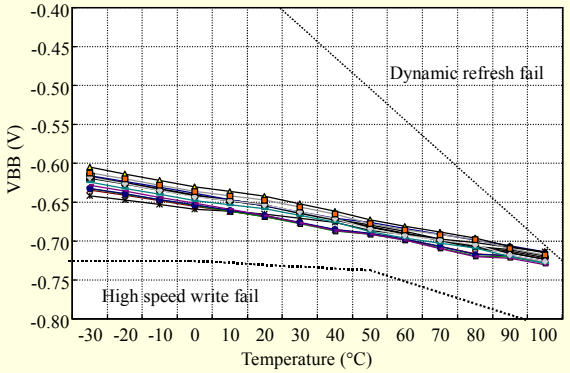
Experimental results are shown in Fig. 9. The supply dependencies of five samples that use the proposed NTD VBB generator at 95℃ are shown in Fig. 9(a). The maximum VBB level difference is only 14 mV over the operating voltage range (1.65 V to 2.2 V).

Figure 9(b) shows the temperature dependencies using the proposed scheme. The maximum VBB level difference is –108 mV, so we can derive the temperature dependency as –0.85 V/℃.

As previously illustrated, this negative temperature dependency is desirable for guaranteeing the proper operation of the pseudo SRAM. It meets the specifications for dynamic refresh failure and high speed write failure over the operating temperature range. The static current consumption of the proposed NTD VBB generator is found to be only 0.83 μA @2.2V, which demonstrates its power efficiency. Table 1 summarizes the performance of the 256 MB pseudo SRAM.



(a) Measured VBB level for variations in the supply voltage



(b) Measured VBB level for variations in the temperature

Fig. 9. Measured VBB level using the proposed scheme.

Table 1. Measured characteristics of the 256 MB pseudo SRAM using the negative temperature dependence VBB generator.

Process	Samsung 100 nm RCAT pseudo SRAM process
Density/application	256 MB pseudo SRAM for mobile application
Chip size (die)	5,127 μm × 7,507 μm = 38.5 mm^2
Operation voltage	1.65 V to 2.2 V
Operating temperature	–30°C to 100°C
Operation frequency	104 MHz
Average operating current	35 mA
VBB static current (simulation)	0.83 μA
VBB supply dependency	–25.5 mV/V @ 1.65 V to 2.2 V
VBB temperature dependency	–0.85 mV/°C

V. Conclusion

A low power temperature-adaptive back-bias voltage generator is proposed in the present work. The proposed back-

bias voltage generator has a negative temperature dependency which guarantees the proper operation of the pseudo SRAM. It is suitable for mass production because of its simple structure and tuning method. The proposed scheme is implemented on the pseudo SRAM for mobile applications using the Samsung 100 nm RCAT pseudo SRAM process technology, and we obtained results showing that it has a temperature dependency of –0.85 mV/℃ over the operating range, and its static current consumption is found to be only 0.83 μA@2.0 V.

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Samsung group award grand prize for the successful developments of 1 Mb DRAM and 1 Gb DRAM in 1986 and 1996, respectively. From 2007 to 2008, he was in charge of the DRAM products and technology. He has published more than 430 technical papers in the field of memory technology. He has applied for and holds more than 130 patents related to memory technology. He is recipient of ISI's citation award for a highly cited paper. He is the recipient of the 2008 Professional Achievement award of the UCLA School of Engineering. Dr. Kim has served as a committee member or program vice chair for premier conferences such as IEDM, SSDM, etc. He is an IEEE fellow and a Samsung fellow.

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