Partial EBG Structure with DeCap for Ultra-wideband Suppression of Simultaneous Switching Noise in a High-Speed System

Jong Hwa Kwon, Sang Il Kwak, Dong-Uk Sim, and Jong-Gwan Yook

To supply a power distribution network with stable power in a high-speed mixed mode system, simultaneous switching noise caused at the multilayer PCB and package structures needs to be sufficiently suppressed. The uni-planar compact electromagnetic bandgap (UC-EBG) structure is well known as a promising solution to suppress the power noise and isolate noise-sensitive analog/RF circuits from a noisy digital circuit. However, a typical UC-EBG structure has several severe problems, such as a limitation in the stop band's lower cutoff frequency and signal quality degradation. To make up for the defects of a conventional EBG structure, a partially located EBG structure with decoupling capacitors is proposed in this paper as a means of both suppressing the power noise propagation and minimizing the effects of the perforated reference plane on the signal quality. The proposed structure is validated and investigated through simulation and measurement in both frequency and time domains.

Keywords: Electromagnetic bandgap (EBG), signal integrity (SI), power integrity (PI), simultaneous switching noise (SSN), decoupling capacitor (DeCap).

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I. Introduction

The simultaneous switching noise (SSN) or ground bounce noise (GBN) that occurs in the power/ground (P/G) planes used to deliver power in multilayer PCBs and packages has become an issue of major concern with regard to high-speed digital circuits with higher clock frequencies, faster edge rates, faster device switching speed, and lower driving voltage levels. SSN caused by fast time-varying currents can excite the cavity resonance modes between parallel plate waveguide-shaped P/G planes and can cause significant problems for the signal/power integrity (SI/PI) as well as electromagnetic interference (EMI) [1], [2]. To build a stable power distribution network (PDN) in high-speed digital circuits with analog/RF circuits, SSN should be sufficiently suppressed in the entire frequency range up to several gigahertz.

Several researchers have contributed toward coping with SSN. Adding decoupling capacitors between the P/G planes is a typical approach to eliminate SSN, but they cannot suppress SSN effectively above a few hundred megahertz due to the unavoidable parasitic inductances. Although using a moat on the P/G planes or selecting the location of a shorting via can suppress SSN at higher frequencies, these approaches are narrowband solutions and are suitable only to suppress SSN at specific local regions [3], [4]. Recently, electromagnetic bandgap (EBG) structures have been proposed as a promising solution to properly cope with SSN problems within gigahertz frequency ranges. An EBG has a periodic structure that can block the propagation of surface currents within a specific frequency range, namely, the stopband, due to its high

impedance property. The initial model was a mushroom-shaped EBG consisting of metal pads connected to a P/G plane with blind vias [5]-[7]. However, these multilayer EBG structures with vias are difficult to implement. Furthermore, they require an additional layer to achieve the EBG patches, thereby making the EBG structures an expensive solution. To overcome the mechanical defects of these conventional structures, uni-planar compact EBG (UC-EBG) structures have been proposed [8]-[13], which consist of a two-dimensional lattice pattern on a single plane, namely, the power plane. However, a typical UC-EBG structure has several severe drawbacks, which obstruct its practical use. One drawback is a limitation in the expansion of the lower bandgap frequency due to its physical size. EBG structures cannot suppress noise at a lower frequency range below about 300 MHz in typical PCBs because the lower limit of an EBG structure's bandgap is inversely proportional to the physical size of the unit cell. The other drawback is the possibility of signal quality degradation. The P/G planes with periodically etched slots used to form EBG structures may degrade the signal quality of a high-speed signal due to their imperfection [9]-[13].

In this paper, a partially placed EBG structure with a decoupling capacitor (DeCap) only near a critical noise source is proposed as a means of both suppressing the noise propagation from DC to several gigahertz and minimizing the effect of the perforated reference plane on high-speed signal lines. The noise suppression performance of the proposed structure is compared using conventional P/G planes with fully located EBG unit cells on the entire plane and a bare reference board. The SSN suppression performance of the proposed structure was validated and investigated through simulation and measurement in both frequency and time domains.

II. Design Concept

Even if an EBG structure is adopted at the P/G planes, the cavity resonant modes still exist in the parallel plate waveguide-shaped PDN outside the stopband of the EBG. Moreover, the resonant frequencies in a PDN with EBG structures appear at lower frequencies than those of a bare board because the EBG structure affects the electrical length of the wave propagating within the PDN. Therefore, when the EBG pattern is used at the P/G planes, the noise propagation problem can be more severe within the lower frequency range below the stopband. To solve the lower frequency problem, a conventional DeCap is used in this study. As is well known, DeCap is used to decouple the power/ground noise within a low frequency range. By using DeCaps, power plane noise is sufficiently suppressed within a lower frequency range which is not within the operating range of typical EBG structures.

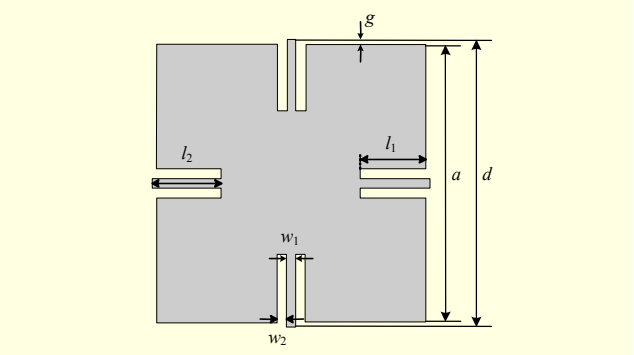

Fig. 1. UC-EBG unit cell structure and parameters.

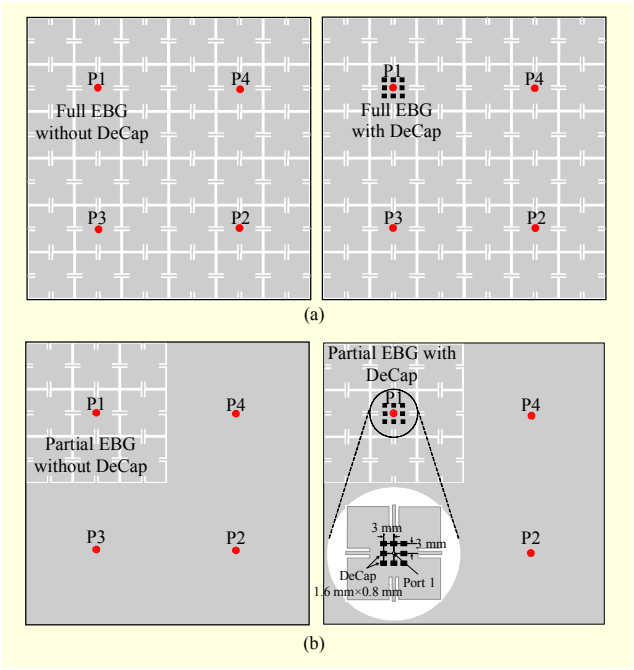

Fig. 2. EBG-patterned test boards: (a) fully and (b) partially located EBG boards with/without DeCaps around a noise source (port 1).

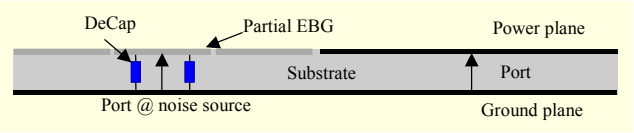

Fig. 3. Side view of the EBG-patterned PCB board.

Next, SSN is mainly generated in digital circuits using a fast clock such as a CPU chip, and noise-sensitive analog/RF devices are generally located in a specific area. In this case, the partial placement of EBG unit cells on only the critical areas of P/G planes not only mitigates SSN sufficiently, but also minimizes the effects of the EBG-patterned reference plane on signal quality by using the solid portion as the return current path of the high-speed signal.

The main objective of this study is to investigate the effects of partial placement of EBG cells with DeCaps near the noise source, on the assumption that the noise source exists only in a specific area. Thus, the well-known UC-EBG unit cell [9], [10] was used as shown in Fig. 1. The unit cells were etched onto the power plane with their corresponding geometrical parameters: d=30 mm, a=28.5 mm, g=0.75 mm, l_1=6.5 mm, l_2=7.5 mm, w_1=1.5 mm, and w_2=1.5 mm. As shown in Fig. 2, the four types of test PCBs used to verify the performance of the proposed structure were designed as follows: (a) fully located EBG (FEBG) boards with/without DeCaps throughout the entire power planes and (b) partially located EBG (PEBG) boards with/without DeCaps near the noise source. A bare PCB board was used as a reference. The four ports were located at P1 (45, 135, 0 mm), P2 (135, 45, 0 mm), P3 (45, 45, 0 mm), and P4 (135, 135, 0 mm), respectively. The point of origin was situated in the lower left-hand corner of the PCB as shown in Fig. 2. These ports were used to evaluate the insertion loss of the structure between ports through simulation and measurement. For clarity, Fig. 3 shows a side view of the PCB with the proposed EBG placement, in which the dimensions of the two-layer PCB were 180 mm × 180 mm with a 1.0 mm FR4 (ε_r=4.5) substrate.

Generally, ideal decoupling capacitors are expected to behave as a short circuit between the P/G planes at high frequencies [3]. However, it has been found that the parasitic inductance of the leads and mounting pads of the decoupling capacitors strongly limits their power supply noise mitigation ability. In fact, the decoupling capacitor behaves as a series RLC resonant circuit, which comes close to being a short circuit only around its self-resonant frequency. To maximize the decoupling effect in the lower frequency range in this study, eight SMT-type DeCaps were symmetrically placed on the power plane around the noise source (port 1) and connected to the power plane through a pad and to the ground plane through a via as shown in Fig 2. The values of the DeCap parameters are C=100 nF, L_{ESL}= 0.55 nH, and R_{ESR}= 0.02 Ω.

III. Simulated and Measured Results

1. Frequency Domain Analysis

The suppression property of power noise can be confirmed using the insertion loss between the ports in the frequency domain. To validate the SSN suppression properties of the proposed structure, EBG-patterned test boards with/without DeCaps and a reference bare board were fabricated. A commercial 3D full-wave EM simulator, HFSS (Ansoft, USA) [14], and a vector network analyzer (Agilent 8236B) were used to obtain the insertion loss between ports.

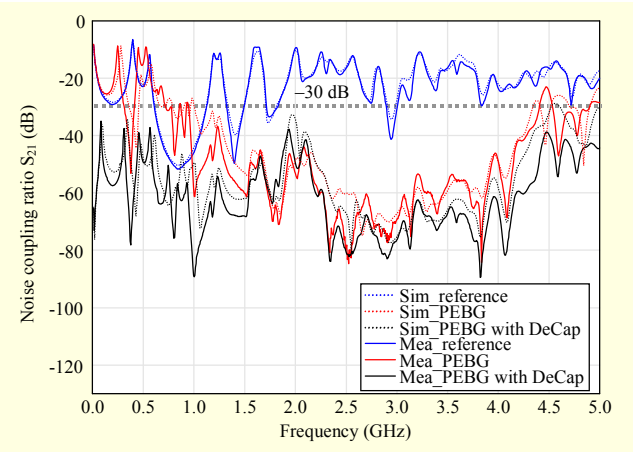

Fig. 4. Comparison of simulated and measured insertion loss S_{21} results for the PEBG boards with and without DeCaps.

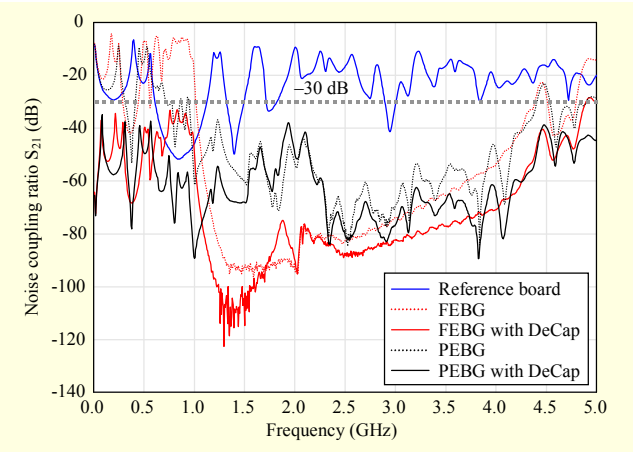

Fig. 5. Measured insertion loss S_{21} results of EBG-patterned test boards.

Figure 4 shows the simulated and measured insertion loss results, S_{21}, for the proposed partial EBG board with/without DeCaps. The insertion loss of the reference board with both power and ground planes solid is also presented in this figure for comparison. As shown in the figure, reasonable agreement is obtained from DC to 5 GHz between measurements and simulations. Because the dispersion property of the FR4 substrate and the conduction loss were not considered in the simulation, a slight difference between the simulated and measured values was seen at higher frequencies.

Compared with the reference board, the test board with only partially located EBG unit cells provides a wide bandgap from about 0.95 GHz to 4.40 GHz (3.45 GHz bandwidth). Moreover, the proposed PEBG board with DeCaps behaves with highly efficient SSN suppression with an average of 50 dB in a wideband range from DC to about 5.0 GHz (5 GHz bandwidth). In this paper, the bandwidth is defined by S_{21} which is lower than −30 dB. As shown in Fig. 4, the

Table 1. Stop frequency bandwidth and ratio of occupation.

EBG placement	Stop frequency band (GHz)		Ratio of occupation
	Simulation	Measurement	
FEBG without DeCap	1.13 to 4.63 (3.50)	1.02 to 4.38 (3.36)	50 %
FEBG with DeCap	DC to 4.67 (4.67)	DC to 4.90 (4.90)	50 %
PEBG without DeCap	1.01 to 4.34 (3.33)	0.95 to 4.40 (3.45)	12.5 %
PEBG with DeCap	DC to 4.52 (4.52)	DC to 5.0 (5.0)	12.5 %

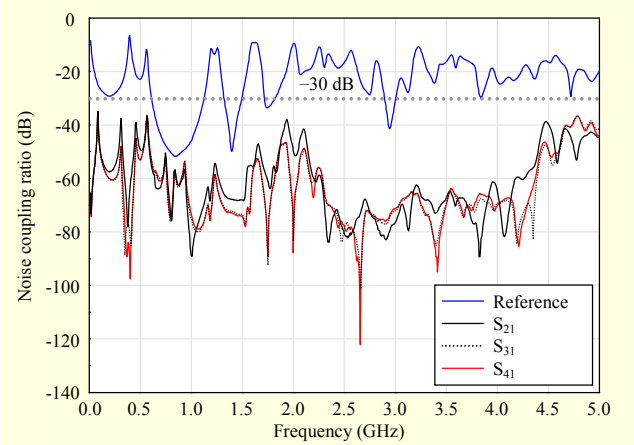

Fig. 6. Measured insertion loss in a partial EBG with DeCaps for noise reception ports at different locations (ports 2, 3, and 4).

suppression property of the proposed structure superposes the properties of the EBG planes and DeCaps. That is, the stop bandwidth of the proposed structure is the sum of bandgaps due to both the DeCaps at a lower frequency range and the partial EBG unit cells at a higher frequency range, and the average suppression level of the proposed structure within the forbidden bandgap is higher than that of the PEBG structure.

Next, to verify the noise suppression properties of the PEBG board compared with the FEBG board, the test boards shown in Fig. 2 were fabricated and measured. Figure 5 compares the measured insertion loss S_{21} results of the FEBG and PEBG boards. The measured insertion loss of the reference board is also presented in this figure for comparison. As shown in Fig. 5, both fully and partially EBG-patterned P/G planes with DeCaps suppressed the SSN from DC to 5 GHz, which is almost the entire noise band defined in [6] and [7]. In the case of the fully EBG-patterned PCB, only one of the P/G planes (that is, the power plane) was used to design the EBG patterns, so their ratio of EBG unit cell occupation on both P/G planes is 50%. Although the proposed partial EBG structure uses only 12.5% of the entire planes, it is confirmed based on the simulated and measured results that the SSN suppression properties of the PEBG board can be very similar to those of the FEBG board as shown in Table 1. Thus, the PEBG board near the noise sources can be a good solution to deal with SSN problems, on the assumption that noise sources and noise-sensitive devices exist only in specific areas.

Figure 6 shows the measured SSN suppression behavior in the case of the partial EBG board with DeCaps for noise reception ports at different locations (ports 2, 3, and 4). The noise excitation port is port 1. Although the EBG cells do not exist at their positions, the proposed structure provides a similar SSN suppression behavior for different positions. This behavior demonstrates that the proposed design can omnidirectionally suppress SSN on the PDN.

2. Time Domain Analysis

We tried to understand the SSN suppression characteristics in the time domain for the proposed EBG-patterned PDN with DeCaps. Figure 7 shows the experimental setup for power integrity analysis in the time domain. The P/G planes of the test boards are excited with 1 $V_{p\text{-}p}$ clock signals as a cavity noise source using a pulse pattern generator (Anritsu MP1763C) at port 1, and the coupling noise at the receiving port (port 2) is measured in the time domain using an oscilloscope (LeCroy SDA6020). The induced noise voltages at port 2 of all the test boards including the reference board are measured.

In Fig. 8, the measured peak-to-peak magnitudes of the induced power noise are compared with the clock frequencies from 50 MHz to 5 GHz with 50 MHz steps. Comparing the power noise magnitude from the EBG boards with DeCap with the magnitude from those without DeCap, as well as with the reference board, much of the power noise was reduced over all frequency ranges from DC to 5 GHz due to the bandgap of EBG structures and the decoupling property of DeCaps as

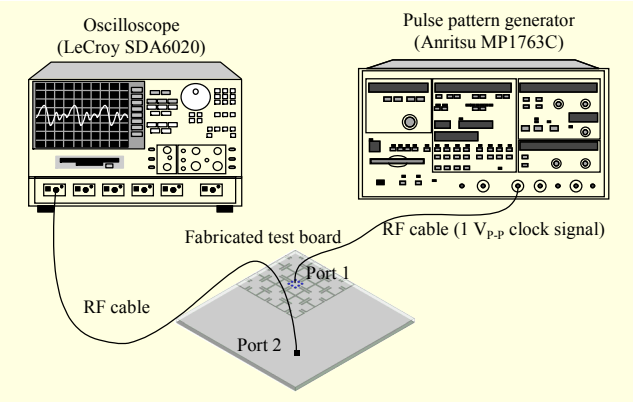

Fig. 7. Experimental setup for a time domain analysis of power noise isolation.

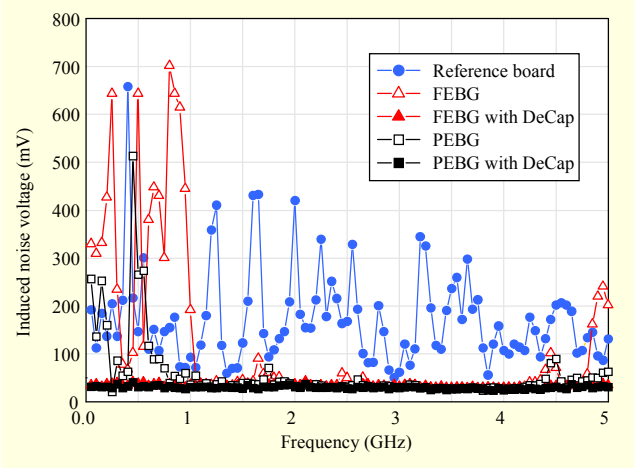

Fig. 8. Measured peak-to-peak magnitudes of the induced power noise at the test board's receiving port, port 2, in the time-domain.

shown in Figs. 4 and 5. The PEBG board with DeCaps has a sufficient noise suppression property in spite of having partially located EBG unit cells in only a specific area. That is, in the case of having the same SSN suppression performance, the PEBG structure has an advantage in comparison with the FEBG structure in terms of signal integrity. If the solid portion of the partially EBG-patterned PDN is used as the return current path for a high-speed signal, SSN can be sufficiently suppressed, and the signal quality can be improved further than in the case of the fully EBG-patterned PDN.

3. Effect on Signal Quality

Although a P/G plane with typical UC-EBG unit cells demonstrates a wideband suppression of SSN with a cost effective design using only two metal layers, P/G planes with slots etched periodically to form UC-EBG structures could degrade the signal quality in a high-speed system because of the imperfect reference plane [13].

To verify that the quality of the high-speed signal passing over a P/G plane with the proposed partial EBG pattern is superior to that of the conventional fully EBG-patterned boards, the test boards were designed and fabricated as shown in Figs. 9 and 10. To evaluate the UC-EBG's effect on signal quality, we considered a signal trace of 315 mm passing over the EBG-patterned power plane. The signal line lay on the top layer. The second and third layers were the fully or partially EBG-patterned power plane and solid ground plane, respectively. The dimensions of the four-layer PCB were 180 mm × 180 mm with a 1.4 mm FR4 (ε_r=4.5) substrate. To show the effects of the EBG-patterned power plane on the high-speed signal, the power plane underneath the high-speed signal was considered as a reference plane to that signal in this study. Thus,

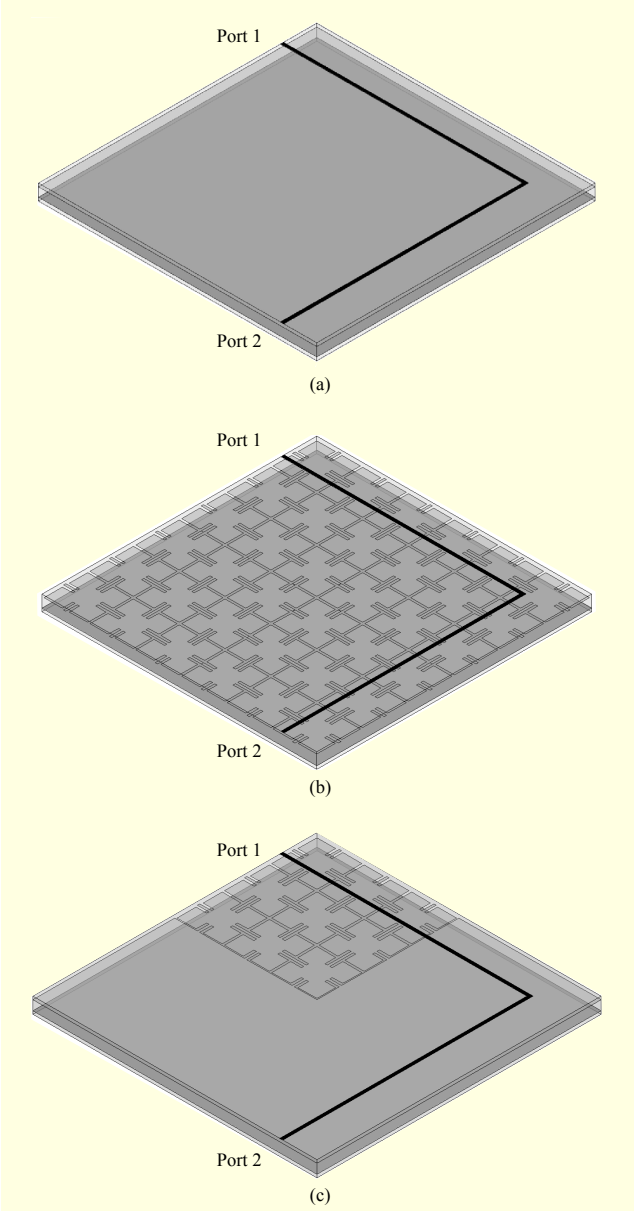

Fig. 9. Four-layer structure with signal line over the EBG-patterned power plane: (a) reference board, (b) fully and (c) partially located EBG boards.

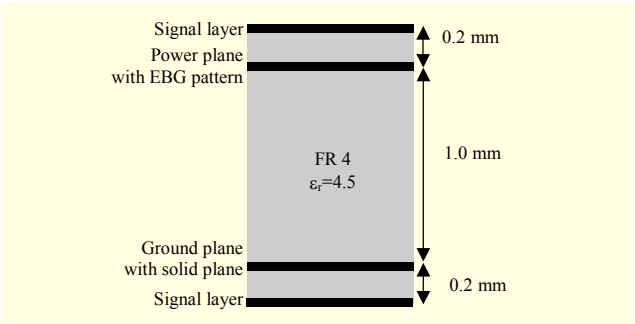

Fig. 10. Stack-up for a four-layer structure with signal line over EBG-patterned power plane.

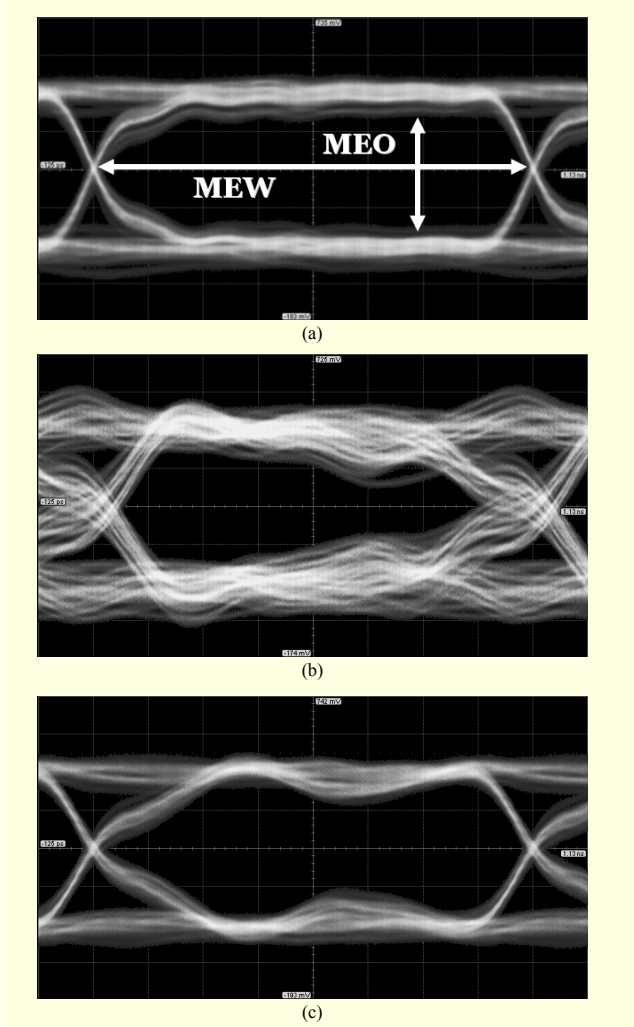

Fig. 11. Measured eye patterns: (a) reference board (continuous power plane), and PCB boards with (b) fully and (c) partially located EBG unit cells.

the signal and the ground pins of the connector at each port in Fig. 9 were connected to the signal line and the power plane, respectively.

The setup in Fig. 7 was used to evaluate the impact of the UC-EBG power plane on the signal quality, referring to the perforated reference plane. To obtain an eye pattern, the pattern source of a 2^7–1 pseudo-random bit sequence (PRBS) non-return to zero (NRZ) coded at 1.0 GHz was launched at port 1 using a pattern generator (Anritsu MP1763C). The bit sequence swing is 1.0 V and the nominal rise/fall time is 120 ps. By launching the pattern source, the eye patterns were measured at the output port (port 2) using an oscilloscope (LeCroy SDA6020).

Figure 11 shows the measured eye patterns for the signal quality analysis. Figure 11(a) shows the measured eye patterns for the reference board with a continuous power plane for comparison. Figures 11(b) and (c) show the eye patterns for the PCB board with fully and partially located EBG unit cells, respectively. In this paper, two parameters, maximum eye open (MEO) and maximum eye width (MEW), are used as metrics of the eye pattern quality. Table 2 shows the measured MEW and MEO with the relative ratio based on the reference board.

Table 2. Measured MEO and MEW in the eye pattern results.

EBG placement	MEO (mV)		MEW (ps)	
Reference board	374.02	100 %	956	100 %
Full EBG board	308.23	82.4 %	710	74.3 %
Partial EBG board	344.93	92.2 %	933	97.6 %

The MEO and MEW are 374.02 mV and 956 ps for the reference board. The MEO and MEW are 308.23 mV and 710 ps for the full EBG board, and 344.93 mV and 933 ps for the partial EBG board. For the full EBG board, the degradation of the MEO is about 17.6% and that of the MEW is about 25.7%. These results show that as the signal line passing over EBG-patterned boards is lengthened, the signal quality is further degraded. For a partial EBG board, the degradation of the MEO is about 7.8% and that of the MEW is about 2.4%. Compared with the reference board, it is clearly seen that there is no severe degradation of the signal quality for the proposed partial EBG board. Therefore, when the proposed partial EBG-patterned board with DeCaps is used in high-speed digital systems, the SSN could be sufficiently suppressed without the signal integrity problem. The signal integrity performance will be better if the signal trace is shorter or if the data transmission rate is slower than 1.0 Gbps.

IV. Conclusion

In this paper, a partially placed EBG structure with a DeCap only near the critical noise source was proposed as a means of both suppressing the noise propagation from DC to several gigahertz and minimizing the effect of a perforated reference plane on high-speed signal lines. The noise suppression performance of the proposed structure was compared with conventional fully located EBG unit cells on the entire plane with and without DeCaps, and with a bare reference board. From the simulated and measured results, the PEBG board with DeCaps had a wide suppression bandwidth ranging from DC to more than 5 GHz. The stop bandwidth of the proposed structure is the sum of bandgaps due to both DeCaps at a lower frequency range and the partial EBG board at a higher frequency range. From the time domain signal analysis, we confirmed that there is no severe degradation of the signal

quality for the proposed partial EBG board. The SSN suppression performance of the proposed structure was validated and investigated by simulation and measurement in both time and frequency domains.

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