Measurement Accuracy of Oscillation-Based Test of Analog-to-Digital Converters

Peter Mrak, Anton Biasizzo, and Franc Novak

Oscillation-based testing of analog-to-digital converters represents a viable option for low-cost built-in self-testing in mixed-signal design. While numerous papers have addressed implementation issues, little attention has been paid to the measurement accuracy. In this letter, we highlight an inherent measurement uncertainty which has to be considered when deriving the parameters from the oscillation frequency.

Keywords: mixed-signal test, analog-to-digital converter, (ADC) oscillation-based test (OBT), measurement accuracy.

I. Introduction

In the oscillation-based test (OBT) proposed in [1], a circuit-under-test is transformed into an oscillator, and the frequency of oscillation is compared to a reference value obtained from a known-good circuit operating in the same measurement conditions. Discrepancy between the oscillation frequency of a circuit-under-test and the reference value indicates possible faults.

The OBT technique has been applied to various kinds of mixed-signal circuits [2]-[8].

In OBT of an analog-to-digital converter (ADC), a feedback loop is provided which forces the ADC to oscillate around a selected code i [7]. The feedback loop is fed to a circuit which generates a triangle wave signal of symmetrical slope as shown in Fig 1. The slope of the triangle wave signal is inverted one sample time after the sampled input signal attains or crosses the threshold voltage as shown in Fig. 2.

The measured frequency of the triangle wave signal can serve as the basis of a go/no-go ADC test. Furthermore, it can be used to determine static ADC parameters such as differential
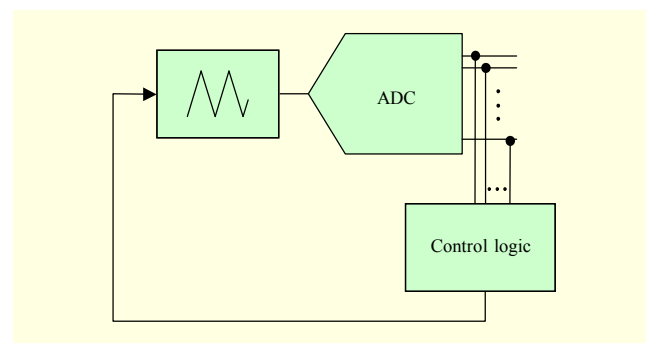

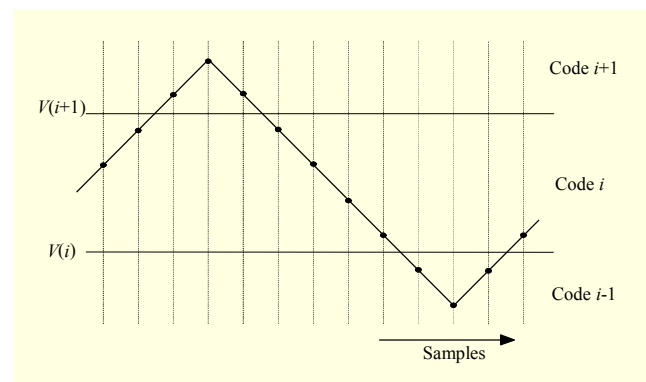Fig. 1. Oscillation-based test structure of ADC.

Fig. 2. Sampling of triangle wave input signal.

nonlinearity (DNL) and integral nonlinearity (INL). While other authors have studied implementation issues of OBT, such as input signal generation, digital comparators, and feedback circuitry, none of them have addressed the measurement accuracy of the test method.

In this letter, we focus on the mechanism of generating the triangle waveform signal and demonstrate an inherent measurement uncertainty which has to be considered when deriving the parameters from the oscillation frequency.

II. Preliminaries

An ADC generates a single output code for a range of input voltages. The voltage level where the ADC output changes to code i is defined as the threshold voltage $V(i)$. The difference between the threshold voltages $V(i+1)$ and $V(i)$ is called the code width $Q(i)$. The code widths of an n-bit ideal ADC are equal and are determined by dividing the full scale range (FSR) by the number of ADC codes:

$$Q_N(i) = Q_N = \frac{FSR}{2^n} . \qquad (1)$$

DNL is a figure of merit that describes the uniformity of steps between ADC codes. The deviation of the threshold voltages from their nominal values causes different sizes of code widths. DNL for a selected code i is given by

$$DNL(i) = \frac{Q(i) - Q_N}{Q_N} . \qquad (2)$$

Without loss of generality, we assume that the slope S of the triangle wave signal is generated such that the signal traverses the nominal code width Q_N in a whole number k_N of sample periods T_S:

$$Q_N = S \cdot k_N \cdot T_S . \qquad (3)$$

The actual code width $Q(i)$ is obtained by determining the time $k \cdot T_S$ of the input signal passing between $V(i)$ and $V(i+1)$:

$$Q(i) = S \cdot k \cdot T_S . \qquad (4)$$

Evaluation of k from the measured oscillation frequency represents the basis of our further discussion.

III. Evaluation of Measurement Accuracy

The conversion of an ADC is not instantaneous; the acquired code is delayed for the conversion time. The output of the ADC is compared to the selected code i at the sampling instances, and the slope of the triangle signal is inverted depending on the result. The triangle wave signal is sampled periodically at $T(j)$ as shown in Fig. 3.

Let us denote the first sample time as $T(-1)$, where the input signal is equal to or greater than the threshold voltage $V(i+1)$. Since the output code of the ADC is delayed for the sample time T_S, the slope of the input signal is inverted at the sample time $T(0)$. In general, the transition of the input signal over the threshold voltage occurs at $T(-1)$ or somewhere within the interval between $T(-2)$ and $T(-1)$. For further analysis, let us denote the time between the transition of the threshold voltage $V(i+1)$ and the sample time $T(-1)$ as $\delta \cdot T_S$, where the values of δ are

$$0 \le \delta < 1 . \qquad (5)$$

The time from the transition of the threshold voltage $V(i+1)$ to the inversion of the slope at $T(0)$ is $(1+\delta) \cdot T_S$. Since the rising and the falling slopes are equal, the transition of the threshold voltage $V(i)$ occurs at $(1+\delta+k) \cdot T_S$ after $T(0)$. Depending on the values of k and δ, we distinguish two different cases:

$$k + \delta < \lceil k \rceil , \qquad (6)$$

$$k + \delta \ge \lceil k \rceil , \qquad (7)$$

where $\lceil \ \rceil$ is the ceiling operator which rounds a number to its nearest integer value in an upwards direction. This results in two different signals, which are represented in Fig. 3 by the continuous and the dashed lines. The first case refers to the situation in which the signal transition of the threshold voltage $V(i)$ occurs before $T(\lceil k \rceil +1)$, while the second case refers to the situation in which the signal transition of the threshold voltage $V(i)$ occurs after $T(\lceil k \rceil +1)$. Consequently, the inversion of the slope of the two signals differs for one sample time, which leads to two different oscillation periods:

$$T_1 = (2 \cdot \lceil k \rceil + 4) \cdot T_S , \qquad (8)$$

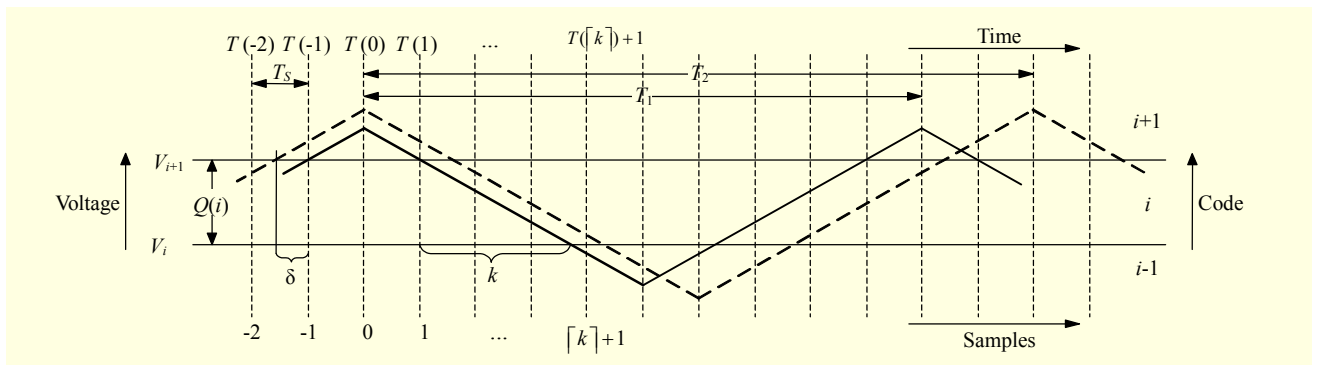$$T_2 = (2 \cdot \lceil k \rceil + 6) \cdot T_S . \qquad (9)$$

Fig. 3. Detailed timing diagram.

Table 1. Simulated results for $DNL(2) = 0.3$.

δ k_N	Measured $DNL(2)$								Meas. uncert.
	0.062	0.188	0.312	0.438	0.562	0.688	0.812	0.938	
2	0.00	0.00	0.00	0.50	0.50	0.50	0.50	0.50	0.500
3	0.00	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.333
4	0.25	0.25	0.25	0.25	0.25	0.25	0.50	0.50	0.250
6	0.17	0.17	0.33	0.33	0.33	0.33	0.33	0.33	0.167
8	0.25	0.25	0.25	0.25	0.25	0.38	0.38	0.38	0.125
16	0.25	0.25	0.31	0.31	0.31	0.31	0.31	0.31	0.062
32	0.28	0.28	0.28	0.31	0.31	0.31	0.31	0.31	0.031

For an ideal ADC, the input signal traverses the code width in a whole number k_N of sample periods T_S as assumed in (3). Since k_N is a whole number, the first of the two considered cases described by (6) and (7) is not feasible. The only oscillation period, denoted by T_N, is thus

$$T_N = (2 \cdot k_N + 6) \cdot T_S. \tag{10}$$

The actual measured oscillation period T is either T_1 or T_2. Because we cannot distinguish between the two cases, the computation of k from expressions (8) and (9) gives

$$k = \frac{T}{2 \cdot T_S} - 3 \pm 1. \tag{11}$$

The two possible outcomes are reflected in the code width $Q(i)$:

$$Q(i) = S \cdot \left(\frac{T}{2 \cdot T_S} - 3 \right) \cdot T_S \pm S \cdot T_S. \tag{12}$$

From the definition of DNL we obtain

$$DNL(i) = \frac{T - T_N}{2 \cdot k_N \cdot T_S} \pm \frac{1}{k_N} \tag{13}$$

for the selected code i.

For illustration, an 8-bit ADC with $DNL(2) = 0.3$ was considered. The OBT technique was modeled in the Matlab Simulink environment. We simulated the OBT for different values of k_N and δ. Obtained values of $DNL(2)$ and the corresponding measurement uncertainty are given in Table 1.

IV. Conclusion

An oscillation-based test of ADC manifests in two different oscillation periods depending on the time of the transition of the threshold voltage relative to the sampling. Since we cannot distinguish between the two cases, the ambiguity of the frequency of oscillation should be considered in OBT implementations. We demonstrated that the measurement uncertainty of the DNL due to this ambiguity is $1/k_N$.

References

[1] K. Arabi and B. Kaminska "Oscillation-Test Strategy for Analog and Mixed-Signal Circuits," *Proc. VLSI Test Symp.*, 1996, pp. 476-482.

[2] K. Arabi and B. Kaminska, "Design for Testability of Integrated Operational Amplifiers Using Oscillation-Test Strategy," *Proc. Int. Conf. Comput. Design*, 1996, pp. 40-45.

[3] K. Arabi and B. Kaminska, "Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 16, no. 7, 1997, pp. 745-753.

[4] G. Huertas et al., "Effective Oscillation-Based Test for Application to a DTMF Filter Bank," *Proc. Int. Test Conf.*, 1999, pp. 549-555.

[5] M. Santo Zarnik, F. Novak, and S. Macek, "Design of Oscillation-Based Test Structures for Active RC Filters," *IEE Proc. Circuits Devices Syst.*, vol. 147, no. 5, 2000, pp. 297-302.

[6] P.M. Dias, J.E. Franca, and N. Paulino, "Oscillation Test Methodology for a Digitally-Programmable Switched-Current Biquad," *Proc. IEEE Int. Mixed Signal Testing Workshop*, 1996, pp. 221-226.

[7] K. Arabi and B. Kaminska, "Oscillation Built-In Self Test (OBIST) Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits," *Proc. Int. Test Conf.*, 1997, pp. 786-795.

[8] G. Huertas et al., "Oscillation-Based Test in Bandpass Oversampled A/D Converters," *Microelectron. J.*, vol. 34, no. 10, 2003, pp. 927-936.