Effects of Channel Electron In-Plane Velocity on the Capacitance-Voltage Curve of MOS Devices

Ling-Feng Mao

The coupling between the transverse and longitudinal components of the channel electron motion in NMOS devices leads to a reduction in the barrier height. Therefore, this study theoretically investigates the effects of the in-plane velocity of channel electrons on the capacitance-voltage characteristics of nano NMOS devices under inversion bias. Numerical calculation via a self-consistent solution to the coupled Schrödinger equation and Poisson equation is used in the investigation. The results demonstrate that such a coupling largely affects capacitance-voltage characteristic when the in-plane velocity of channel electrons is high. The ballistic transport ensures a high in-plane momentum. It suggests that such a coupling should be considered in the quantum capacitance-voltage modeling in ballistic transport devices.

Keywords: Quantum coupling, metal-oxide-semiconductor structure, capacitance.

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I. Introduction

As metal-oxide-semiconductor (MOS) devices continue to shrink, new physical phenomena are becoming increasingly important in the device performance. For a very thin gate oxide, direct tunneling results in an exponential increase in gate leakage current, and the series resistance in MOS capacitors becomes significant due to the low impedance of the capacitors [1]. As a result, experimental capacitance-voltage curves for ultrathin gate MOS devices show capacitance attenuation [2]. Because capacitance-voltage measurement is a fundamental technique for MOS devices characterization, capacitance-voltage curves are crucial in providing device information. For example, the extraction of the gate oxide thickness by classical treatment of low-frequency capacitance-voltage data is significantly inaccurate because the quantum nature of the surface space-charge region is ignored. The most accurate way of incorporating the quantum confinement in the inversion layer of a MOS structure is to solve a set of coupled Schrödinger-Poisson equations [3]-[7].

Most works on numerical solution of the coupled Schrödinger-Poisson equations in the literature [3]-[7] are restricted by an assumption that the components of electron motion in the three directions are decoupled. Such an approximation can result in a larger error in the estimation of the gate leakage current [8], [9]. A reduction in the Si/SiO_2 barrier height caused by the coupling between the longitudinal and transverse components of thermal energy of tunneling electrons has been discussed in [8]. Such a coupling has also been applied to study the reduction in the Si/SiO_2 barrier height

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caused by the channel electron velocity and its effects on the gate leakage current through the oxide in MOS devices [9]. The quantum coupling between the transverse and longitudinal components (parallel and perpendicular to the Si/SiO_2 interface) results in a reduction in the Si/SiO_2 barrier height. Such a reduction increases with increased in-plane velocity.

The channel electron velocity can reach a value as high as 4.5×10^7 cm/s [10]. The channel electron velocity calculated by using drift-diffusion, energy balance, and energy transport models varies from 1×10^7 cm/s to 9×10^7 cm/s [11], and an experimental value higher than 1×10^7 cm/s at 85 K has been demonstrated [12]. A ballistic transport in a MOS device can ensure a near scattering-free condition and leads to a high channel electron velocity; therefore, it is worthwhile to study how the quantum coupling in a MOS device under inversion bias affects the capacitance-voltage characteristics of nano *n*-MOS devices.

II. Method

The capacitance of a MOS device generally consists of three components in series connection [13]: the per unit area gate oxide capacitance ($C_{\text{ox}} = \varepsilon_{\text{ox}} / t_{\text{ox}}$), depleted poly-gate capacitance (C_{GD}), and surface capacitance (C_{SB}). The total capacitance C is thus given by

$$C = \left(\frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{GD}}} + \frac{1}{C_{\text{SB}}} \right)^{-1}. \quad (1)$$

Quantum mechanical effects and polydepletion delay the information of the inversion layer with respect to the applied gate bias. The combination of thinner gate oxide thickness (t_{ox}) and higher channel doping concentration results in very high electric fields at the Si/SiO_2 interface. Thus, it gives rise to splitting of the energy bands into discrete subbands due to the quantum confinement effects in the inversion layer. It can also result in an increased threshold voltage, a decreased gate capacitance caused by decreased slope of the inversion charge versus gate voltage, and a reduced drain current [14].

The capacitance is obtained as the derivative of the total sheet charge density in the Si substrate with respect to the bias voltage ($C = dQ / dV$). Frequency sensitive to space charge has not been considered in this work; thus, static capacitance has been calculated in this work. To calculate the total sheet charge density in the Si substrate of a nano-MOSFET, the quantization in the inversion layer must be considered. The Schrödinger equation for a MOS device under the parabolic band effective mass approximation can be written as

$$\left(\frac{1}{2m_{\perp}(z)} \hat{p}_{\perp}^2 + \frac{1}{2m_z(z)} \hat{p}_z^2 + \phi(z) \right) \psi = E\psi, \quad (2)$$

where $\phi(z)$ represents the potential energy along the z direction; $m_{\perp}$ and m_z denote the mass in and perpendicular to the Si/SiO_2 interface plane, respectively; z is the direction perpendicular to the Si/SiO_2 interface; $p_{\perp}$ and p_z represent the electron momentum operators parallel and perpendicular to the Si/SiO_2 interface, respectively; and E is the total energy of a channel electron.

In mathematics, a conserved quantity of a Hamiltonian system is a function of the dependent variables that is a constant. According to (2), $\left[\hat{p}_{\perp}, \hat{H} \right] = 0$. This means that the transverse momentum of the electron ($\hbar^2 k_r^2$) is conserved. The conservation of $\hbar^2 k_r^2$ requires that the three-dimensional wave function, the solution to (2), should take the following form:

$$\psi = \exp\left(i\vec{k}_r \cdot \vec{r} \right) \Phi(z). \quad (3)$$

Note that in the calculation of the capacitance-voltage curves in this work, static capacitance has been considered. To calculate the total sheet charge density, only wave function $\Phi(z)$ needs to be determined because the sheet is perpendicular to the z direction, and only gate voltage is applied to the device in the calculation. Similar to the deduction in [9], $\Phi(z)$ in the silicon substrate region, the oxide region, and the gate region satisfies

$$\left[-\frac{\hbar^2}{2m_{z-Si}^*} \frac{\partial^2}{\partial z^2} + \phi(z) \right] \Phi(z) = E_z^s \Phi(z), \quad (4)$$

$$\left[-\frac{\hbar^2}{2m_{\text{ox}}^*} \frac{\partial^2}{\partial z^2} + \left(\phi(z) - \frac{\hbar^2 k_r^2}{2m_{\perp-Si}^*} \left(1 - \frac{m_{\perp-Si}^*}{m_{ox}^*} \right) \right) \right] \Phi(z) = E_z^s \Phi(z), \quad (5)$$

$$\left[-\frac{\hbar^2}{2m_{\text{g}}^*} \frac{\partial^2}{\partial z^2} + \left(\phi(z) - \frac{\hbar^2 k_r^2}{2m_{\perp-Si}^*} \left(1 - \frac{m_{\perp-Si}^*}{m_{\text{g}}^*} \right) \right) \right] \Phi(z) = E_z^s \Phi(z), \quad (6)$$

where m_{z-Si}^* and $m_{\perp-Si}^*$ are the longitudinal and transverse effective masses of channel electrons in the substrate region, respectively; m_{g}^* is the longitudinal effective mass of electrons in the gate region; and E_z^s is the energy of a channel electron along the z direction in the silicon substrate. The combination of thinner gate oxide thickness (t_{ox}) and higher channel doping concentration leads to very large electric fields at the Si/SiO_2 interface. This gives rise to splitting of the energy bands into discrete subbands, which means that E_z^s is quantized.

Note that $\hbar^2 k_r^2 / 2m_{\perp-Si}^*$ is the transverse energy of a channel electron in the plane parallel to the Si/SiO_2 interface. Thus, the Si/SiO_2 barrier height seen by the channel electrons changes with the in-plane velocity according to (4), (5), and (6). The effective Si/SiO_2 barrier height can be obtained as

$$\phi_{\text{eff}} = \phi(z) - \frac{\hbar^2 k_r^2}{2m^*_{\perp-Si}}\left(1 - \frac{m^*_{\perp-Si}}{m^*_{\text{ox}}}\right). \quad (7)$$

Therefore, the quantization energy level in the inversion layer will change due to the reduction in the Si/SiO_2 barrier height. It is well known that the energy quantization changes the carrier density of the inversion layer. This means that the in-plane velocity via quantum coupling will affect the total sheet charge density in the Si substrate of a MOS device. It indicates that there will be a greater change in the total sheet charge density of ballistic transport MOS devices compared that in conventional MOS devices at the same gate voltage. It implies that both the quantized energy level and the electron density profile will be affected by in-plane velocity. According to $C = dQ / dV$, the capacitance of a ballistic transport MOS device will change compared to that of a conventional MOS device at the same gate voltage. In other words, such a coupling can affect the quantization in the inversion layer and results in a change in the capacitance-voltage curve.

An accurate description of the channel electrons in the inversion layer of *n*-channel MOS devices with a *p*-type silicon substrate requires a self-consistent solution of the coupled Poisson and Schrödinger equation. A one-dimensional Poisson equation along the *z* direction can be written as

$$\frac{\partial}{\partial z}\left[\varepsilon(z)\frac{\partial \varphi}{\partial z}\right] = -e\left[N_D^+(z) - N_A^-(z) + p(z) - n(z)\right], \quad (8)$$

where φ is the electrostatic potential; $\varepsilon(z)$ is the spatially dependent dielectric constant; $N_D^+(z)$ and $N_A^-(z)$ are the ionized donor and acceptor concentrations, respectively; and $n(z)$ and $p(z)$ are the electron and hole densities, respectively.

The iteration procedure used in this paper to obtain self-consistent solutions to coupled Schrödinger-Poisson equations is described in the following section. Starting with a trial potential, the wave functions and their corresponding eigenenergies can be calculated. Thus, the eigenenergies can be used to calculate the electron density distribution in the silicon substrate. The calculated electron density distribution and a given acceptor donor concentration can be used to calculate potential using (8). The subsequent iteration results in the final self-consistent solution. The maximum allowed correction (in eV) to the band diagram in the calculations for the converged structure is 1×10^{-10} eV.

III. Results and Discussion

In this study, the coupled Schrödinger-Poisson equations from the metal/SiO_2 interface with the silicon substrate in an *n*-MOS device with metal gate are numerically solved using the finite-difference method [6], [7]. Such solutions are carried out after the quantum coupling between the longitudinal and transverse components of channel electron motion is considered. The conduction band offset between Si and SiO_2 and the barrier height at the metal/SiO_2 interface were chosen as 2.9 and 3.1 eV, respectively. The transverse mass of $0.19m_0$, the longitudinal mass of $0.98m_0$ of electrons in silicon [15], and the effective electron mass of $0.5m_0$ in SiO_2 were used in the calculations.

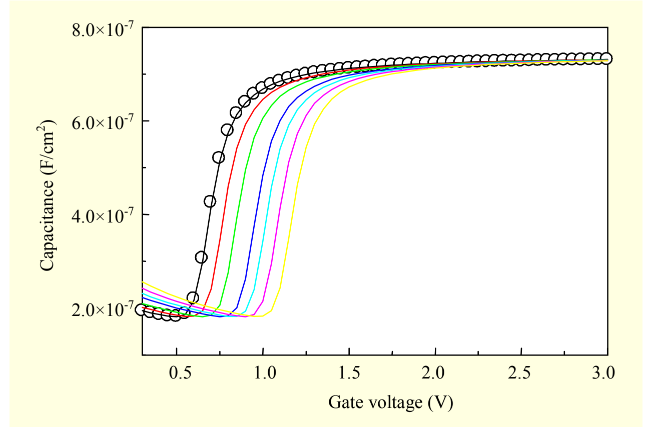

Fig. 1. Simulated capacitance under inversion bias when coupling is considered and when it is ignored as a function of gate voltage. Open circles represent the capacitance when coupling is ignored. Solid lines represent various channel electron velocities with an acceptor concentration in Si of 5×10^{17} cm^{-3} and an oxide thickness of 2.0 nm. The in-plane channel electron velocities from left to right are 1×10^7, 5×10^7, 7×10^7, 9×10^7, 1×10^8, 1.1×10^8, and 1.2×10^8 cm/s.

Figure 1 shows the capacitance-voltage curves of an *n*-MOS under inversion bias. Results were obtained for the capacitance when the coupling between the longitudinal and transverse components of channel electron motion was considered and when it was ignored. This figure clearly demonstrates that a higher in-plane channel electron velocity results in the capacitance shifting to a higher voltage. Therefore, it can be concluded that the quantum coupling will have an obvious influence on the capacitance-voltage curve. Such an influence is obvious when the in-plane channel electron velocity is higher than 1×10^7 cm/s. This implies that the in-plane channel electron velocity effects on the capacitance-voltage curve can be ignored for a conventional *n*-MOS device. On the other hand, they need to be considered for a nanometer *n*-MOS device where the ballistic transport ensures that the in-plane channel electron velocity is higher than the thermal injection velocity. This figure also clearly demonstrates that a higher in-plane momentum channel electron momentum leads to a higher threshold voltage due to the quantum coupling between the longitudinal and transverse components of channel electron motion.

Figure 2 shows how the relative change in capacitance

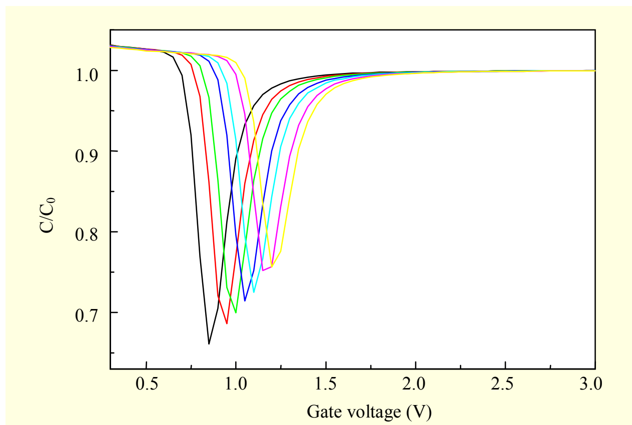

Fig. 2. Ratio of the simulated capacitance under inversion bias when coupling is considered and when it is ignored as a function of the gate voltage. Solid lines represent various oxide thicknesses with in-plane channel electron velocities of 4.5×10^7 cm/s and an acceptor concentration in Si of 1×10^{18} cm^{-3}. The oxide thicknesses from left to right are 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, and 4.0 nm.

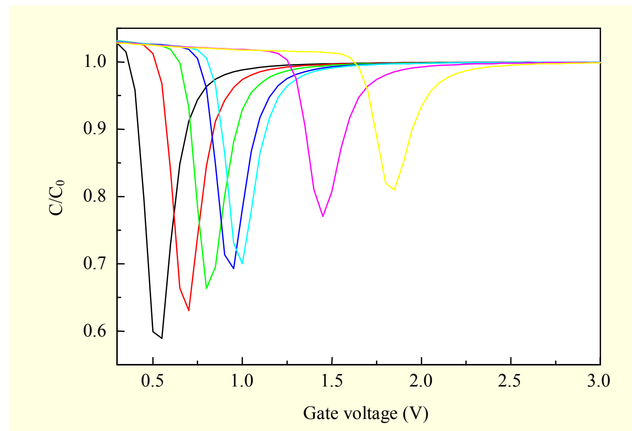

Fig. 3. Ratio of the simulated capacitance under inversion bias with considering the coupling and to those without considering the coupling as a function of gate voltage. Solid lines represent different acceptor concentration in Si with the in-plane velocity of channel electron being 4.5×10^7 cm/s and oxide thickness being 2.0 nm. The acceptor concentrations from left to right are 3×10^{17}, 5×10^{17}, 7×10^{17}, 9×10^{17}, 1×10^{18}, 2×10^{18}, and 3×10^{18} cm^{-3}.

caused by the coupling between the longitudinal and transverse components of channel electron motion change with the gate voltage for various oxide thickness. In the calculations of this figure, the in-plane channel electron velocity is 4.5×10^7 cm/s, and the acceptor concentration in Si is 1×10^{18} cm^{-3}. This figure clearly demonstrates that the capacitance region that is most effected by the quantum coupling between the longitudinal and transverse components of channel electron motion shifts to a higher gate voltage with increased oxide thickness.

Figure 3 demonstrates that the relative change in capacitance caused by the coupling between the longitudinal and transverse components of channel electron motion changes with gate voltage for various acceptor concentrations. In the calculations of this figure, the in-plane channel electron velocity is 4.5×10^7 cm/s and the oxide thickness is 2.0 nm. This figure clearly shows that the capacitance region most effected by the quantum coupling between the longitudinal and transverse components of channel electron motion shifts to a higher gate voltage with increased acceptor concentration.

Now we discuss the origin of the change in the capacitance-voltage curve of *n*-MOS devices. The quantum coupling effect with a high in-plane channel electron momentum has been found to strongly affect the quantization in the version layer of *n*-channel MOS devices [16]. This means that a higher in-plane channel electron momentum causes a redistribution of channel electrons. Thus, it results in a change in the number of inversion electrons. Also, quantum coupling results in a change in the capacitance-voltage curve of *n*-MOS devices. In other words, the coupling effect on the capacitance-voltage curve of *n*-MOS devices can be ignored for conventional MOS devices but needs to be considered for nanometer MOS devices because the ballistic transport ensures that the in-plane channel electron velocity is higher than the thermal injection velocity 1.2-2 $\times10^7$ cm/s. In summary, the change in the capacitance-voltage curve of *n*-MOS devices originates from the quantum coupling effect on the quantization in the version layer of MOS devices with *p*-type silicon substrates.

IV. Conclusion

To summarize, the in-plane channel electron velocity is found to strongly affect the capacitance-voltage relation of *n*-MOS devices. It originates from the quantum coupling between the longitudinal and transverse components of electron motion based on the analysis of the three-dimensional Schrödinger equation. Such an effect is obvious when the in-plane channel electron velocity is higher than 1×10^7 cm/s. The calculations demonstrate that the capacitance-voltage curve shifts to a higher gate voltage when the in-plane channel electron velocity increases due to the quantum coupling effect. The calculations also show that the capacitance-voltage curve affected by such a coupling is sensitive to the oxide thickness and acceptor concentration.

Basically, the quantum coupling between the transverse and longitudinal components of the channel electron motion in MOS devices results in a reduction in the Si/SiO_2 barrier height. Such a reduction increases with increased in-plane velocity. Note that such a reduction in the barrier height can cause a phase shift of the electron waves in the inversion layer of a MOS device [17], and this can lead to an energy shift of the quantized energy level [17]. A higher in-plane

velocity can result in a larger phase shift of the electron waves [17], a larger energy shift in the quantized energy levels, and a larger change in the total sheet charge density. The change in the total sheet charge density causes a change in the capacitance-voltage curve.

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