Direct Digital Control of Single-Phase AC/DC PWM Converter System

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Abstract

This paper presents a new technique for directly designing a linear digital controller for a single-phase pulse width modulation (PWM) converter systems, based on closed-loop identification. The design procedure consists of three steps. First, obtain a digital current controller for the inner loop system by using the error space approach, so that the power factor of the supply is close to one. The outer loop is composed of a voltage controller, a current control loop including a current controller, a PWM converter, and a capacitor. Then, all the components, except the voltage controller, are identified by a discrete-time equivalent linear model, using the closed-loop output error (CLOE) method. Based on this equivalent model, a proper digital voltage controller is then directly designed. It is shown through PSim simulations and experimental results that the proposed method is useful for the practical design of PWM converter controllers.

Key Words: direct digital control, AC/DC PWM converter, closed-loop identification, characteristic ratio assignment (CRA)

I. INTRODUCTION

PWM AC/DC converters have been widely used for applications such as PWM inverter fed induction motor drives and interruptible power supply (UPS) systems. The main objectives of a PWM AC/DC converter are to regulate the DC voltage level while maintaining a sinusoidal AC current waveform and a unity power factor.

For the control of voltage source converters, the current controlled PWM techniques have been widely used due to their advantages, such as the control of instantaneous current waveforms and high accuracy, peak current protection, extremely good dynamics, and compensation of effects due to parameter changes and AC source voltage changes, etc. [1]. Current controlled PWM techniques can be divided into two groups: linear and nonlinear. The linear controllers include the ramp comparison current controller [2], the synchronous vector controller [3], the state feedback controller [4], and the predictive and dead-beat controllers [5], [6]. The hysteresis controller [2], the pulse density modulation algorithm [7], and the neural networks and fuzzy logic based controllers belong to the nonlinear controller group [8], [9]. Each controller has its advantages and limitations, but as the trend favors fully digital control, the methods which allow digital implementation are preferred, despite some sacrifices in accuracy and dynamic performance. In particular, for low switching frequency ap-

plications in large power systems, such as traction drives, the digitally implemented cascaded inner/outer structure PI controllers are recommended [10], [11].

In the cascaded structure of the DC output voltage and AC input current controllers of a PWM converter are generally constructed with double feedback loops, which consist of an inner AC current feedback loop and an outer DC voltage feedback loop. Each feedback loop is usually designed with a PI controller. The reference waveform of the AC current is generated by multiplying the error output of the DC voltage controller as the amplitude of the AC current waveform with the unit sinusoidal waveform in phase with the AC line voltage. Then the AC current controller operates to follow the reference current waveform not only to meet the sinusoidal current waveform and unity power factor but also to regulate the DC voltage. These kinds of current controlled PWM techniques have advantages, such as the control of instantaneous current waveforms and high accuracy, peak current protection, extremely good dynamics, and compensation of effects due to parameter changes and AC source voltage changes, etc. [1], [11]. However the converter includes a switching component, which has nonlinear characteristics, and both the inner loop and the outer loop cannot be handled in a single framework. It could be modeled in a single nonlinear system using a power balance, but the small signal model is valid only around specified operating points [12]. Otherwise, it could be linearized by using input-output feedback, but the design of the included PI controllers was not investigated [13].

This paper presents a new technique for designing direct digital controllers so that they provide good transient re-

sponses for DC voltage regulation under practical severe load change conditions. The inner current control loop can be designed using the error-space approach [14] independently of the outer voltage loop [15]. Then, the whole inner loop system, including the current controller, can be replaced by an equivalent transfer function. The inner loop system, from the right end of the voltage controller to the capacitor, is identified from the input-output data using the CLOE identification algorithm presented in [16]. Based on identified linear model $\bar{G}_o(z)$, a voltage controller satisfying the desired time response specifications is designed, using the w-transform [17], [18] and the characteristic ratio assignment (CRA) [19]. The reference transfer function $H^*(w)$ that meets the prescribed time response is preliminarily generated in the w-domain using the CRA, then this is transformed into the z-domain as $H^*(z)$ so that a controller is obtained directly in the z-domain by solving the Diophantine equation. A similar approach has been presented in [20]. However, the method in [20] can not be referred to the fully direct digital control of a PWM converter because the design of the inner loop controller is carried out by an indirect method in the manner that a continuous-time current controller is first designed and then converted to a digital approximation. In this paper, the fully direct digital design of both the inner and the outer-loop controllers is considered.

For verification of the proposed control algorithm, a prototype of a 4.5kW single phase PWM converter is tested considering the application of an urban light railway system. Through the simulation and experimental results, it is shown that the proposed method is useful for the practical design of PWM converter controllers.

This paper is organized as follows. A single-phase AC/DC PWM converter model is introduced in Section II. In Section III, the direct digital controller design method is presented. The design procedures for the inner current control and the outer voltage control for a PWM converter system are presented in Section IV. In Section V, simulation and experimental results will be followed, as a practical example. Finally, some conclusions are given in Section VI.

II. PWM CONVERTER MODEL

The configuration of a power circuit for a single-phase PWM converter model is shown in Fig. 1. Figure 2 shows the double loop feedback control system, which consists of an inner AC-current loop and an outer DC-voltage loop.

The current controller C_i and the voltage controller C_v are used to force the input current to follow the referenced current waveform and to regulate the output voltage even under the condition of a sudden load change.

In general, the current controller is designed so that the power factor at the supply terminal is close to one. That is, it is required that the supply voltage v_s and the current i_s be in-phase as close as possible. This means that both the current loop and the voltage loop cannot be handled in a single framework because of the nonlinearity due to the 60Hz modulator. This is the main reason that a simple controller of the PID type for a PWM converter is difficult to obtain analytically.
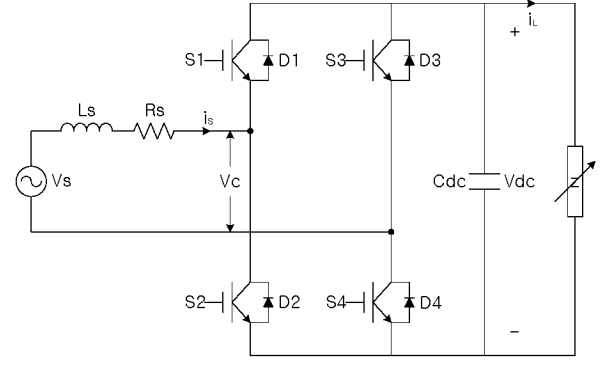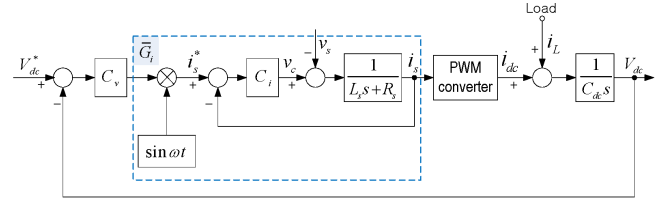

Fig. 1. Typical circuit for a PWM converter.

Fig. 2. Block diagram of the PWM converter control system.

In the next section, the design technique of a direct digital controller is introduced, which will meet the given time response specifications in a single loop feedback system. This approach will be used for the digital control problem of the PWM converter.

III. DIRECT DIGITAL CONTROL WITH TIME RESPONSE REQUIREMENTS

Consider the discrete-time feedback control system shown in Fig. 3. A linear time invariant (LTI) plant and an R-S-T type controller [16] are described by

$$\frac{B(z^{-1})}{A(z^{-1})} = \frac{b_1 z^{-1} + b_2 z^{-2} + \cdots + b_{n_B} z^{-n_B}}{1 + a_1 z^{-1} + a_2 z^{-2} + \cdots + a_{n_A} z^{-n_A}}, (1)$$

$$S(q^{-1}) u(k) = -R(q^{-1}) y(k) + T(q^{-1}) r(k) \quad (2)$$

where q denotes the shift operator defined by $qy(k) := y(k+1)$, and

$$\begin{aligned} S(z^{-1}) &= 1 + s_1 z^{-1} + \cdots + s_{n_S} z^{-n_S}, \\ R(z^{-1}) &= r_0 + r_1 z^{-1} + \cdots + r_{n_R} z^{-n_R}, \quad (3) \\ T(z^{-1}) &= t_0 + t_1 z^{-1} + \cdots + r_{n_T} z^{-n_T}. \end{aligned}$$

The closed-loop transfer function is given by

$$\begin{aligned} H(z^{-1}) &= \frac{T(z^{-1}) B(z^{-1})}{A(z^{-1}) S(z^{-1}) + B(z^{-1}) R(z^{-1})} \\ &= \frac{T(z^{-1}) B(z^{-1})}{P(z^{-1})}. \quad (4) \end{aligned}$$

The characteristic polynomial $P(z^{-1})$ is

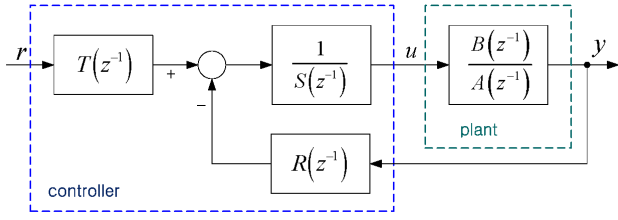$$\begin{aligned} P(z^{-1}) &= A(z^{-1}) S(z^{-1}) + B(z^{-1}) R(z^{-1}) \\ &= p_0 + p_1 z^{-1} + \cdots + p_n z^n. \quad (5) \end{aligned}$$

Fig. 3.   Feedback system with R-S-T type controller.

Fig. 4.   Block diagram of the inner loop system.

Suppose that the design problem here is to find a digital controller R, S, T for the given discrete time response specifications, such as the maximum overshoot and the settling time limitation.

Applying the model matching method to this problem, it can be described by

$$
\begin{aligned}
H\left(z^{-1}\right) & = \frac{T\left(z^{-1}\right) B\left(z^{-1}\right)}{P\left(z^{-1}\right)} \\
& \equiv \frac{T\left(z^{-1}\right) B\left(z^{-1}\right)}{P^*\left(z^{-1}\right)} = H^*\left(z^{-1}\right).
\end{aligned} \qquad (6)
$$

where $H^*\left(z^{-1}\right)$ and $P^*\left(z^{-1}\right)$ are the reference model and the reference characteristic polynomial, respectively. To proceed with (6), it is necessary to find a reference model $H^*(z^{-1})$ that satisfies the time response specifications. In [18], a simple technique for this problem has been proposed. This method consists of three steps. Firstly, the prospective closed-loop transfer function $H(z^{-1})$ is transformed into the w-domain by the w-transform. The transformed function is given by

$$
H(w) = \frac{\bar{B}(w)}{P(w)} = \frac{t_0 \sum_{i=0}^{n} b_i (w+C)^i (w-C)^{n-i}}{\sum_{j=0}^{n} p_j (w+C)^j (w-C)^{n-j}} \qquad (7)
$$

where $C = \frac{2}{T_s}$.

Here, it is notable that $\bar{B}(w)$ is a fixed known polynomial whose coefficients are functions of only $B(z^{-1})$ for a given $T(z^{-1})$. The second step is to find a reference polynomial $P^*(w)$ so that the reference model $H^*(w) = \bar{B}(w)/P^*(w)$ meets the design specifications. Such a reference model can be easily found by means of the CRA, as presented in [18]. In the third step, $H^*(z^{-1})$ is obtained by transforming $H^*(w)$ into the z-domain inversely. Then the controller, $S(z^{-1})$ and $R(z^{-1})$ can be determined by solving the following algebraic equation.

$$
\begin{aligned}
P^*\left(z^{-1}\right) & = A\left(z^{-1}\right) S\left(z^{-1}\right) + B\left(z^{-1}\right) R\left(z^{-1}\right) \\
& = p_0^* + p_1^* z^{-1} + \cdots + p_n^* z^n.
\end{aligned} \qquad (8)
$$

This polynomial equation has a unique solution with a minimal degree (when $A\left(z^{-1}\right)$ and $B\left(z^{-1}\right)$ do not have common factors) for $n_P \leq n_A + n_B - 1$, $n_R = n_A - 1$, and $n_S = n_B - 1$.

To achieve zero steady state error to a step reference input, the overall system must be of *Type* 1. Then $T(z^{-1})$ can be
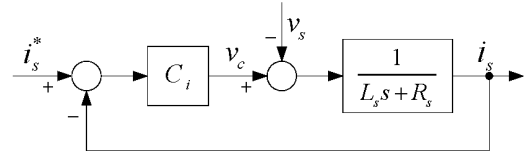
obtained by

$$
T\left(z^{-1}\right) = t_0 = \frac{P(1)}{B(1)} = R(1). \qquad (9)
$$

IV. PWM CONVERTER CONTROL SYSTEM DESIGN

This section describes the design process for the double loop controller. In the first step, the inner current controller is designed, based on the error space approach, independently of the outer control loop. Subsequently, an equivalent linear model of the inner loop system, which includes some nonlinear components, is obtained. After selecting a temporary voltage controller that makes the overall system stable, the CLOE identification method is applied to identify the linearized model from the input-output data. Once the model is identified, a direct digital voltage controller is designed by using the w-transform and the CRA method [18].

A. Inner Loop Design

The error-space feedback scheme is a well known state-feedback method that allows a controller to perfectly track a non-decaying input, and to reject non-decaying disturbances such as sinusoidal inputs. Since this method solves the control problem in the error space, it has robustness because the error approaches zero against the variation of some parameters provided that the system keeps stable.

The state equation of the inner loop system in Fig. 4 can be expressed as

$$
\begin{cases}
\dot{x}(t) & = -\frac{R_s}{L_s} x(t) - \frac{1}{L_s}\left[u(t) - v_s(t)\right], \\
y(t) & = x(t)
\end{cases} \qquad (10)
$$

where $x(t) = i_s(t)$ and $u(t) = v_c(t)$.

The discrete-time state equations of (10) with a sample time T_s are given by

$$
\begin{cases}
x(k+1) & = \Phi x(k) + \Psi \bar{u}(k), \\
y(k) & = x(k)
\end{cases} \qquad (11)
$$

where

$$
\begin{cases}
\Phi & = e^{-\frac{R_s}{L_s} T_s}, \\
\Psi & = -\frac{1}{L_s} \int_0^{T_s} e^{-\frac{R_s}{L_s} t} dt = -\frac{1}{R_s}\left[1 - e^{-\frac{R_s}{L_s} T_s}\right], \\
\bar{u}(k) & := \left[u(k) - v_s(k)\right].
\end{cases} \qquad (12)
$$

Let the reference input of the current controller be $r(k) = i_s^*(k) = I_s \sin\left(\omega_0 k T_s\right)$. It follows that

$$
\Gamma(q) r(k) = 0 \qquad (13)
$$

where

$$
\Gamma(q) = q^2 - 2\cos\left(\omega_0 T_s\right) q + 1. \qquad (14)
$$

Letting $\beta = \cos(\omega_0 T_s)$, then (14) is rewritten as

$$\Gamma(q) = q^2 - 2\beta q + 1. \tag{15}$$

The tracking error is defined as

$$e(k) := r(k) - y(k) = i_s^*(k) - i_s(k). \tag{16}$$

From (13) and (16), the error is formulated in terms of the plant state,

$$\Gamma(q)e(k) = -\Gamma(q)y(k) = -\Gamma(q)x(k). \tag{17}$$

Now, a new state vector and a control input in the error space are defined as

$$\xi(k) := \Gamma(q)x(k), \tag{18}$$
$$\mu(k) := \Gamma(q)u(k). \tag{19}$$

Then (17), (18), and (19) lead to

$$\Gamma(q)e(k) = -\xi(k), \tag{20}$$
$$\xi(k+1) = \Phi\xi(k) + \Psi\mu(k). \tag{21}$$

In the derivation of (21), the relation $\Gamma(q)v_s(k) = 0$ is used as long as $v_s(k)$ keeps the same frequency as $i_s^*(k)$. Equations (20) and (21) show the overall system in error space. Rewriting them in the state variable form, they can be described as

$$z(k+1) = Fz(k) + G\mu(k) \tag{22}$$

where $z(k) = \begin{bmatrix} e(k) & e(k+1) & \xi(k) \end{bmatrix}^T$ and

$$F = \begin{bmatrix} 0 & 1 & 0 \\ -1 & 2\beta & -1 \\ 0 & 0 & \Phi \end{bmatrix}, \quad G = \begin{bmatrix} 0 \\ 0 \\ \Psi \end{bmatrix}. \tag{23}$$

It is obvious that $\{F, G\}$ is controllable. Therefore, there exists a controller that can assign closed-loop poles to any desired location. Let the state feedback controller be

$$\mu(k) = -Kz(k), \tag{24}$$

where $K := [k_1 \ k_2 \ k_3]$.
From (18), (19) and (24), it is shown that

$$\Gamma(q)u(k) + k_3\Gamma(q)x(k) = -k_1 e(k) - k_2 e(k+1). \tag{25}$$

Then (25) can be rearranged as

$$[u(k) + k_3 x(k)]q^2 - 2\beta[u(k) + k_3 x(k)]q$$
$$+ [u(k) + k_3 x(k)] = -(k_1 + k_2 q)e(k). \tag{26}$$

Let us define

$$\eta(k) := u(k) + k_3 x(k). \tag{27}$$

Using (27), (26) yields

$$\eta(k) = [2\beta\eta(k) - k_2 e(k) + \eta_1(k)]q^{-1} \tag{28}$$

where

$$\eta_1(k) = [-\eta(k) - k_1 e(k)]q^{-1}. \tag{29}$$

Let $\eta(k) = \eta_2(k)$, from (27), (28), and (29), the control law is given by

$$\begin{bmatrix} \eta_1(k+1) \\ \eta_2(k+1) \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ 1 & 2\beta \end{bmatrix}\begin{bmatrix} \eta_1(k) \\ \eta_2(k) \end{bmatrix} - \begin{bmatrix} k_1 \\ k_2 \end{bmatrix}e(k), \tag{30}$$
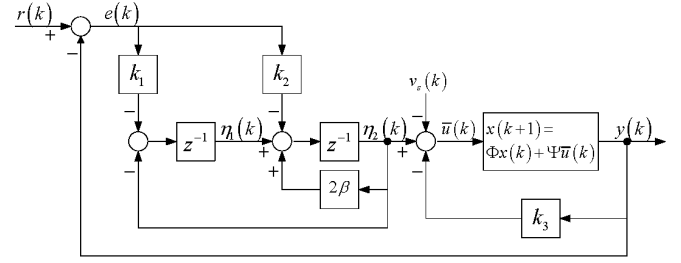$$u(k) = \eta_2(k) - k_3 x(k). \tag{31}$$

Fig. 5. Current controller for PWM converter.

A block diagram of the current controller law (30) and (31) is shown in Fig. 5. The remaining problem is to determine the controller gain vector K such that it satisfies the given time response requirements.

The closed loop dynamics of the current control loop are determined by combining (30) and (31) with (11) to yield

$$\begin{cases} \begin{bmatrix} x(k+1) \\ \eta_1(k+1) \\ \eta_2(k+1) \end{bmatrix} = \begin{bmatrix} \Phi - \Psi k_3 & 0 & \Psi \\ k_1 & 0 & -1 \\ k_2 & 1 & 2\beta \end{bmatrix}\begin{bmatrix} x(k) \\ \eta_1(k) \\ \eta_2(k) \end{bmatrix} \\ + \begin{bmatrix} 0 \\ -k_1 \\ -k_2 \end{bmatrix}r(k) + \begin{bmatrix} \Psi \\ 0 \\ 0 \end{bmatrix}v_s(k), \\ y(k) = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}\begin{bmatrix} x(k) \\ \eta_1(k) \\ \eta_2(k) \end{bmatrix} \end{cases} \tag{32}$$

The closed-loop transfer function from $r(k)$ to $y(k)$ is given by

$$T_i(z) = \frac{I_s(z)}{I_s^*(z)} = \frac{Y(z)}{R(z)} = \frac{-\Psi(k_2 z + k_1)}{\delta(z)} \tag{33}$$

where

$$\delta(z) = z^3 + (\Psi k_3 - \Phi - 2\beta)z^2 + (-\Psi k_2 - 2\beta\Psi k_3 + 2\beta\Phi + 1)z + (-\Psi k_1 + \Psi k_3 - \Phi). \tag{34}$$

Here, the current controller gain K is easily obtained from $\delta(z) \equiv \delta^*(z)$ while the target polynomial $\delta^*(z)$ can be generated by the K-polynomial [18] using the CRA approach. The definition of the K-polynomial is referred to the Appendix VI-A.

Remark 1: The design objective of the current control loop is to make the AC supply voltage and the source current in phase. In order to accomplish this purpose, the internal model control (IMC) approach shown in (13) to (24) has been occupied. In this section, i_s^* and v_s in Fig. 2 have been assumed to be sinusoidal waves of $\omega_0[rad/sec]$. For the cases where these signals include several harmonics due to distortions and sags, there may be some error because the IMC here is used for tracking only one frequency, $\omega_0[rad/sec]$. ▽

B. Outer Loop Design

In the previous subsection, it was presented that the current controller can be designed independently of the voltage controller. As shown in Fig. 2, two nonlinear components are included in the outer loop. Since the output voltage must be kept constant, it is possible to characterize this nonlinear system by a linear model, $\bar{G}_0(z^{-1})$, as shown in Fig. 6.
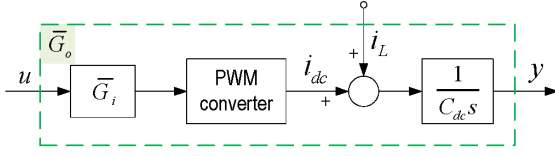
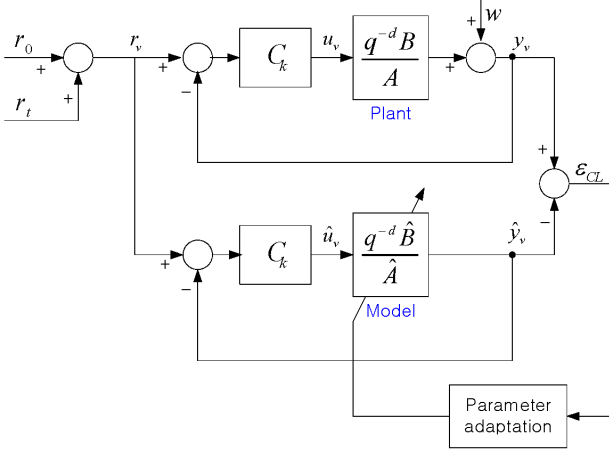Fig. 6.   An equivalent linearized model of the inner loop system.

Fig. 7.   Closed-loop output error (CLOE) identification method

Because the identification should be carried out while the switching components are in operation, the following closed-loop identification scheme is utilized.

1) Closed-loop identification: The principles of the closed-loop identification method are illustrated in Fig. 7.

Let the plant to be identified be

$$
\begin{aligned}
\bar{G}_o\left(q^{-1}\right) &= q^{-d}\frac{B\left(q^{-1}\right)}{A\left(q^{-1}\right)} \\
&= q^{-d}\frac{b_1 q^{-1}+\cdots+b_{n_B}q^{-n_B}}{1+a_1 q^{-1}+\cdots+a_{n_A}q^{-n_A}}. \quad (35)
\end{aligned}
$$

In Fig. 7, C_k denotes the voltage controller and the hatted letters indicate the identified model.

At this point, the controller C_k is not known yet. Thus, in order to carry out the closed loop identification, a simple controller, for example, a proportional controller can be chosen temporarily. It does no matter what C_k is chosen provided that it makes the closed loop system stable, so that the input and output data of the closed loop operation can be acquired. In this procedure, a small perturbed test signal should be injected into either the r or u signal. A pseudo-random binary sequences (PRBS), r_t, is added to the reference DC input. The PRBS is a good test input for identification. Then, the controller output u_v and the system output y_v are measured to estimate the parameters $\{A, B\}$.

Let us define an unknown parameter vector,

$$
\theta\left(k\right) = \left[a_1,\cdots,a_{n_A},b_1,\cdots,b_{n_B}\right]^T, \quad (36)
$$

and the vector of the measured data,

$$
\begin{aligned}
\phi\left(k\right) &= \left[-y_v\left(k\right),\cdots,-y_v\left(k-n_A+1\right),\right. \\
&\quad \left. u_v\left(k-d\right),\cdots,u_v\left(k-d-n_B\right)\right]^T. \quad (37)
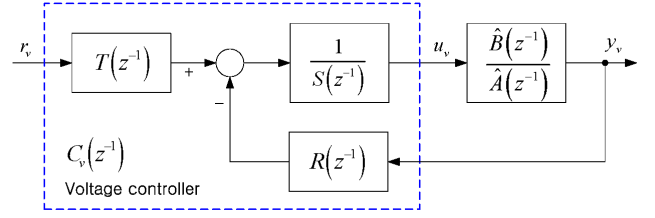\end{aligned}
$$

Fig. 8.   Closed-loop system of the PWM converter.

Then the a priori predicted output is defined by

$$
\hat{y}_v^0\left(k+1\right) = \hat{\theta}^T\left(k\right)\phi\left(k\right). \quad (38)
$$

And the estimated controller output is obtained as

$$
\hat{u}_v\left(k\right) = C_k\left[r\left(k\right)-y\left(k\right)\right]. \quad (39)
$$

Furthermore, the a priori closed-loop prediction output error is given by

$$
\hat{\varepsilon}_{CL}^0\left(k+1\right) = y_v\left(k+1\right)-\hat{y}_v^0\left(k+1\right), \quad (40)
$$

The parameter adaptation algorithm of the CLOE identification is given in the following recursive form [16].

$$
\begin{aligned}
\varepsilon_{CL}^0\left(k+1\right) &= y_v\left(k+1\right)-\hat{\theta}^T\left(k\right)\phi\left(k\right) \\
\hat{\theta}\left(k+1\right) &= \hat{\theta}\left(k\right)+F\left(k+1\right)\Phi\left(k\right)\varepsilon_{CL}^0\left(k+1\right) \\
F\left(k+1\right) &= \frac{1}{\lambda_1}\left[F\left(k\right)-\frac{F(k)\Phi(k)\Phi^T(k)F(k)}{\frac{\lambda_1}{\lambda_2}+\Phi^T(k)F(k)\Phi(k)}\right] \\
\Phi\left(k\right) &= \phi\left(k\right)
\end{aligned}
$$

Herein, the forgetting factors are given by $0 < \lambda_1 \leq 1$, $0 < \lambda_2 \leq 2$.

As a result, the identified equivalent model $\bar{G}_0$ is obtained.

2) Voltage Controller Design: Based on the identified model $\hat{G}_o\left(z^{-1}\right) = \frac{\hat{B}(z^{-1})}{\hat{A}(z^{-1})}$, a direct digital controller that satisfies the transient response specifications is designed.

A block diagram of a PWM converter feedback system is shown in Fig. 8.

The main idea of the direct digital design in [18] is to extend the continuous time CRA to the discrete time case. The controller structure of the R-S-T type is considered and it is assumed that the design objective is to directly find a digital controller of fixed order that meets certain time and frequency response requirements.

As explained in Section III, the prospective closed-loop transfer function $H\left(z^{-1}\right)$ is transformed into the w-domain by using the w-transformation. After regarding $H(w)$ as a function of the s-domain $H(s)$, a reference transfer function associated with a fixed numerator $\bar{B}\left(w\right)$ is composed by using the CRA technique [21], so that it satisfies the design specifications. It is shown in [18] that the mapping error of the w-transform between the s-and w-domains is less than 3% for $|w| \leq 0.6/T_s$ and $|s| \leq 0.6/T_s$. In other words, $H(w) \approx H(s)$ is concluded if a sampling time T_s is selected so that all the poles and zeros of $H(w)$ lie in the region of $|w| \leq 0.6/T_s$ in left half plane of the w-domain. Once such a reference model $H^*(w) = \bar{B}(w)/P^*(w)$ is obtained, then

TABLE I
THE PARAMETERS OF THE MODEL

System parameters	values
Input voltage (V_s)	$150V$(peak), $60Hz$
Output voltage (V_{DC})	$200 \sim 300V$
Switching frequency	$540Hz$
Sampling frequency	$1080Hz$
Resistor	0.08Ω
Inductor (L_s)	$1mH$
Capacitor (C_{DC})	$6000\mu F$
Load (R_L)	$12/24\Omega$

$P^*(w)$ is transformed into the z-domain using the inverse w-transformation, which results in $P^*\left(z^{-1}\right)$.

$$P^*\left(z^{-1}\right) = 1 + p_1^* z^{-1} + \cdots + p_n^* z^{-n}. \tag{41}$$

Solving the following Diophantine equation with $P^*\left(z^{-1}\right)$ from above, the digital controller of (3) is determined.

$$P^*\left(z^{-1}\right) = \hat{A}\left(z^{-1}\right) S\left(z^{-1}\right) + \hat{B}\left(z^{-1}\right) R\left(z^{-1}\right). \tag{42}$$

V. SIMULATION AND EXPERIMENTAL RESULTS

Both simulation and experimental demonstrations have been carried out for a single-phase PWM converter model, the parameters of which are given in Table I. This converter has been designed as a laboratory model of a AC/DC converter for using as a high power urban light railway application with a low switching frequency which has a $860{\sim}1040V$ AC input and a $1600V$ DC output voltage.

The design specifications are as follows:

(i)   the maximum settling time of the current loop system is 10msec,

(ii)   the overshoot limitation of the DC output is less than 5%,

(iii)   the minimum rising time and the maximum settling time of the overall system are 20msec and 200msec, respectively,

(iv)   the stability margins are $GM \geq 10dB$ and $PM \geq 45deg$.

As a simulation tool, the PSiM utility was used. Figure 9 shows the experimental setup of a converter system.

A. Design of the inner loop controller

As described in Section IV-A, in order to design the current controller gain K using the CRA, it is necessary to make a reference characteristic polynomial $\delta^*(z)$ satisfying a settling time of $10msec$. According to the CRA method in [18], when $\alpha_1 = 3$ and $\tau = 3.2 \times 10^{-3}$ are selected, such a reference polynomial in the w-domain is obtained as follows:

$$\delta^*(w) = w^3 + 2.8125 \times 10^3 w^2 + 2.637 \times 10^6 w + 8.24 \times 10^8. \tag{43}$$

The detailed derivation of (43) is referred to Appendix VI-B. The inverse w-transformed polynomial $\delta^*(z)$ is given by

$$\delta^*(z) = z^3 - 1.184 z^2 + 0.4673 z - 0.00615. \tag{44}$$

Solving the identity $\delta(z) \equiv \delta^*(z)$ from (34) and (44), the current controller gain K is determined by

$$K = [k_1 \quad k_2 \quad k_3] = [-0.8480 \quad 0.8674 \quad -1.8196]. \tag{45}$$
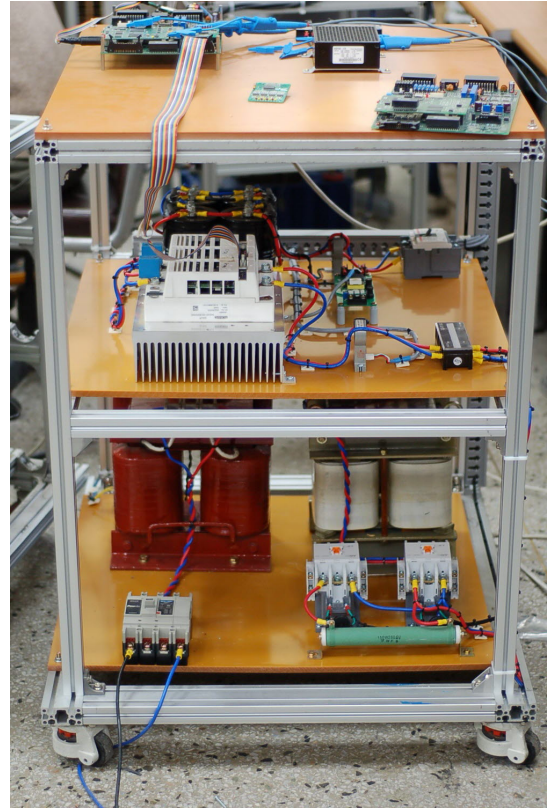

Fig. 9.   Experimental setup of the PWM converter.

As a result of (44) and (45), the inner loop control system has three poles at 0.3947, $0.3947 \pm j3.59 \times 10^{-6}$ and a zero at 0.9776, respectively. It is easy to see from the Bode plot that the bandwidth of the inner loop system is about $f_{BW} = 309Hz$. Generally, the sampling frequency can be chosen by the rule [16], $f_s = (6 \sim 25) \times f_{BW}$, where f_s and f_{BW} are the sample frequency and the closed loop system bandwidth, respectively. Therefore, the sample frequency for the inner loop system needs to be greater than $1,854Hz$. However, the sample frequency given in this example is $1,080Hz$ which is much lower than the recommended value. This is a case where the direct digital control prefers to the digitization approach [16]. This inner loop controller was simulated using the PSiM toolbox. As shown in Fig. 10, the controller makes the current i_s and the supply voltage v_s be in phase. The total harmonic distortion (THD) of the current i_s obtained at the steady state by this controller was less than 0.45 %. Fig. 11 shows that the current controller accomplishes perfect tracking within $10msec$.

B. Design of the outer loop controller

Before going to design a voltage controller, an equivalent model of the outer loop has to be identified. To do this, a proportional voltage controller was temporarily selected. Using the CLOE identification method described in Section IV-B2, the linear equivalent model is obtained by

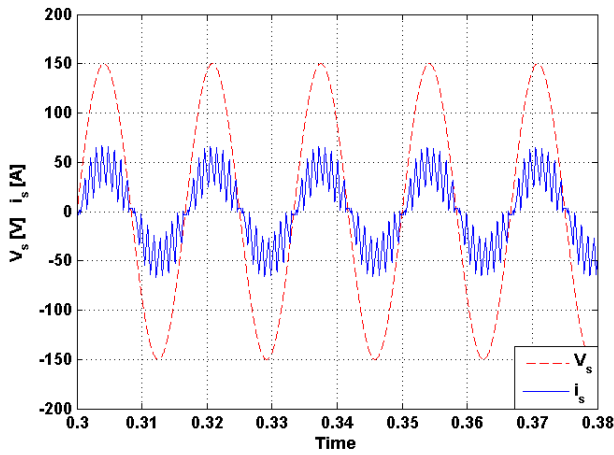$$\hat{G}\left(z^{-1}\right) = \frac{0.04227 z^{-1}}{1 - z^{-1}}. \tag{46}$$
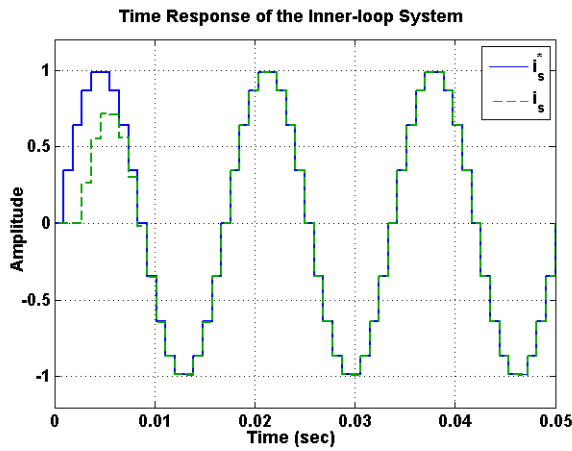
Fig. 10.   The simulation results of the v_s and i_s.

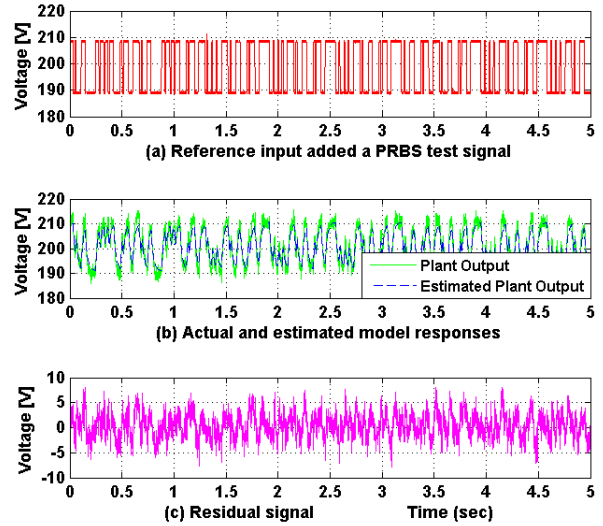Fig. 11.   Time responses of the i_s^* and i_s.

Fig. 12.   Time response of the estimated output.
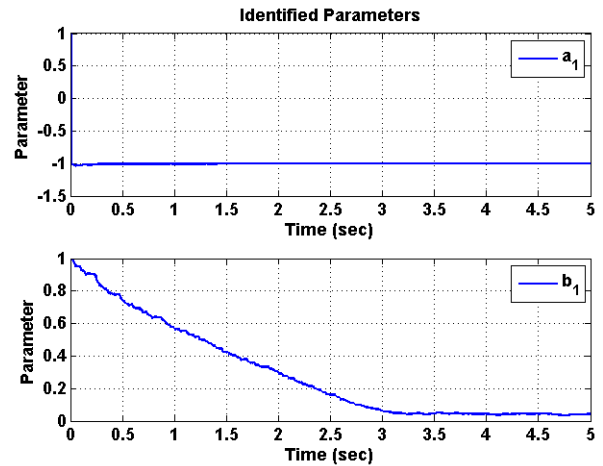
Fig. 13.   Convergence of the identified parameters.
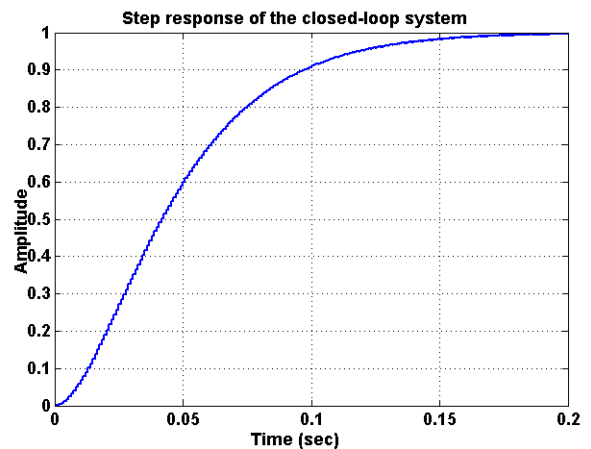
Fig. 14.   Step response of the closed-loop system.

A PRBS test signal of $\pm 10V$ for identification was added to the reference input r (where $r = 200V$ DC), as shown in Fig. 12-(a). Fig. 12-(b) shows the actual output data and the estimated output, while the bottom curve shows the residual which is the difference between the output of the real system and that of the estimated model.

Fig. 13 shows the profiles about how the identified parameters in the CLOE algorithm converge.

Since the equivalent model (46) is of the first order, a RST type PI controller is considered for an outer loop controller. Similar to the design of the inner loop controller, the reference characteristic polynomial $P^*(z)$ below is obtained, so that it meets a settling time of $200msec$ and no overshoot.

$$P^*(z) = z^2 - 1.9273z + 0.9286. \qquad (47)$$

By solving (42) with (47), the voltage controller is

$$
\begin{aligned}
R\left(z^{-1}\right) &= 1.7205 - 1.6893z^{-1}, \\
S\left(z^{-1}\right) &= 1 - z^{-1}, \qquad\qquad (48) \\
T\left(z^{-1}\right) &= 0.0313.
\end{aligned}
$$

The step and frequency responses of the closed-loop system are shown in Figs. 14 and 15, respectively.

The overall system results in no overshoot, a rising time of 84msec and a settling time of 145msec. Also, both the

Fig. 15. Bode diagram of the closed-loop system.
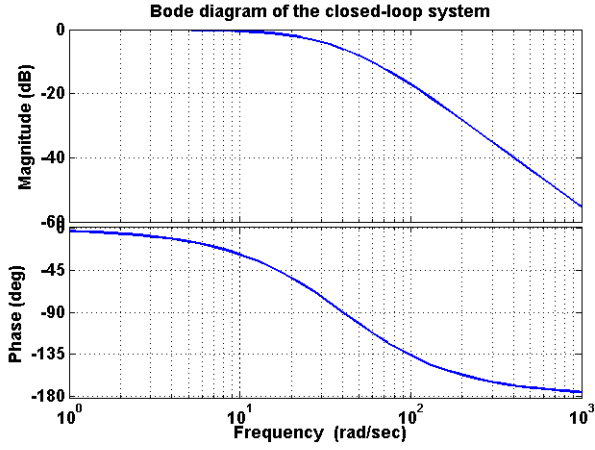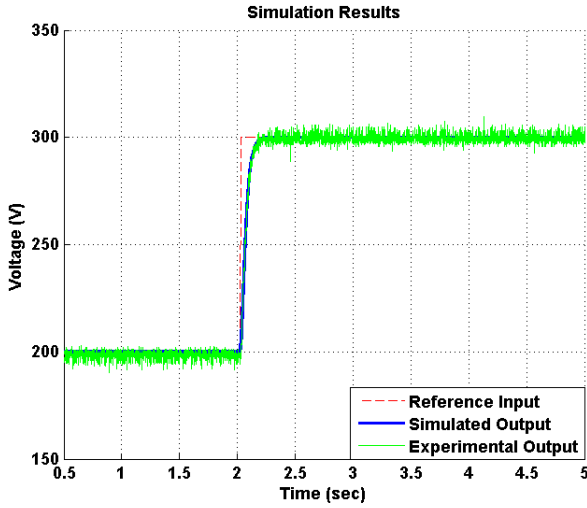

Fig. 16. Simulated and experimental input and output voltages.

Fig. 17. The output voltages with respect to the load changes.

Fig. 18. The experimental results of the v_s and i_s corresponding to Fig. 10.

gain and the phase margins for stability are $69.3dB$ and ∞, respectively. From these results, it has been verified that the time and stability performances are satisfactory.

Figure 16 shows both the simulation and experimental results for the case where the reference voltage is changed from $200VDC$ to $300VDC$ at $t = 2sec$. Both responses coincide with each other and have almost no overshoot.

The time domain performance, subject to abrupt load changes, was experimentally examined. When the load is changed from no load to a half load ar $t = 1.25sec$, from a half to full load at $t = 2.3sec$, and from full load to no load at $t = 3.3sec$, the output voltage consistently remains the same as the reference voltage, as shown in Fig. 17. In this case, the maximum overshoot is less than 4.6%. Figure 18 shows the experimental results of v_s and i_s which correspond to those of Fig. 10. It is seen that these experimental curves are very similar to the simulated ones.

VI. CONCLUSION

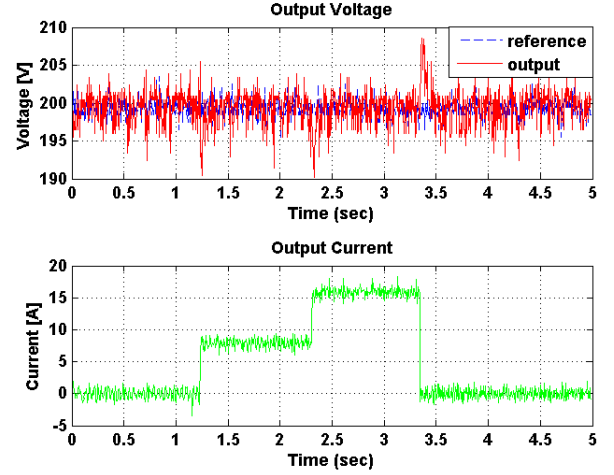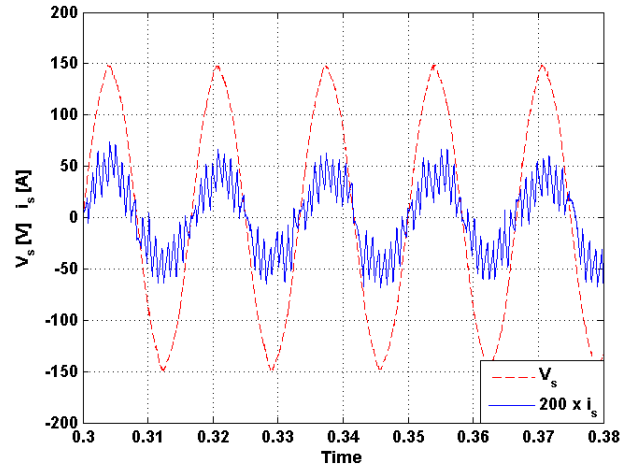In this paper, a direct digital controller design method for a single-phase AC/DC PWM converter system, using closed-loop identification, has been proposed. An error space approach, with the CRA method, is applied for the current control. To identify the linearized model for the outer loop system, which includes an inner loop controller and a switching circuit for the nonlinear component, the CLOE identification method is adapted. Then, the w-transform and the CRA method are used to design a direct digital controller for the identified model. The converter controller is designed to meet the specified time response performances, even though the operational conditions are changed. The PSiM simulations and experiments have been carried out to verify the performance of the designed converter system. From the results, it is shown that the new proposed method achieves good performance.

APPENDIX

A. Definition of the K-polynomial

Consider a real polynomial with positive coefficients,

$$\delta(s) = \delta_n s^n + \cdots + \delta_1 s + \delta_0, \quad \text{for} \quad \delta_k > 0. \quad (49)$$

The *characteristic ratios* and the *generalized time constant* [21] are defined as

$$\alpha_1 := \frac{\delta_1^2}{\delta_0 \delta_2}, \quad \alpha_2 := \frac{\delta_2^2}{\delta_1 \delta_3}, \quad \cdots, \quad \alpha_{n-1} := \frac{\delta_{n-1}^2}{\delta_{n-2}\delta_n}, \quad (50)$$

$$\tau := \frac{\delta_1}{\delta_0}. \quad (51)$$

According to (50) and (51), the coefficient of $\delta(s)$ can be represented in terms of α_is, and τ as follows.

$$\delta_1 = \delta_0 \tau, \quad \delta_2 = \frac{\delta_0 \tau^2}{\alpha_1}, \quad \cdots, \delta_n = \frac{\delta_0 \tau^n}{\alpha_{n-1}\cdots\alpha_1^{n-1}}. \quad (52)$$

In [21], it has been shown that τ is related to the speed of the time response of the all pole system whose denominator is $\delta(s)$, and the α_is are closely related to damping and stability.

The *K-polynomial* is defined as a polynomial for which the characteristic ratios obey the following formula:

$$\begin{cases} \alpha_1 \geq 2, \\ \alpha_k = \frac{\sin\left(\frac{k\pi}{n}\right)+\sin\left(\frac{\pi}{n}\right)}{2\sin\left(\frac{k\pi}{n}\right)}\alpha_1, \quad \text{for} \quad k = 2, \cdots n-1. \end{cases} \quad (53)$$

It is important to note that the *K-polynomial* is generated by only two parameters α_1 and τ for any δ_0. For example, let us make a *K-polynomial*, $\delta_k(s)$, of degree $n = 6$ with $\delta_0 = 1$ and $\tau = 1$. If we choose $\alpha_1 = 2.5$ arbitrarily, then (53) results in

$$[\alpha_1 \ \alpha_2 \ \cdots \ \alpha_5] = [2.5 \ 1.9717 \ 1.875 \ 1.9717 \ 2.5]. \quad (54)$$

Using (52), the following *K-polynomial* is obtained.

$$\delta_k(s) = 1.058\text{x}10^{-5}s^6 + 4.818\text{x}10^{-4}s^5$$
$$+ 8.780\text{x}10^{-3}s^4 + 8.115\text{x}10^{-2}s^3 + 0.4s^2 + s + 1. \quad (55)$$

B. Synthesis of the reference polynomial $\delta^*(w)$: Derivation of (43)

As mentioned in Section IV-A, a current controller gain K that satisfies the maximum settling time and exhibits good damping can be algebraically determined only if such a reference polynomial $\delta^*(z)$ is given. Thus, this problem boils down to the problem of finding such a $\delta^*(w)$. In Section 3.1 of [18] and Section 6 of [19], the methods for synthesizing a transfer function under the conditions of the transient response requirements have been presented. Here, it will be shown how (43) is obtained by using the CRA method. In this approach, we first choose a characteristic ratio, α_1, for the *K-polynomial* of degree 3 such that the transfer function $H_k(s) = \delta_0/\delta_k(s)$ has a satisfactory damping. It was shown in [19] that any value of $H_k(s)$s has a non-overshooting step response only if $\alpha_1 > 2.836$ in (53) holds when $n = 3$. Thus, we are supposed to choose $\alpha_1 = 3.0$. Then the other characteristic ratio α_2 becomes 3.0 from (53). Assuming that $\tau_f = 0.01$ and $\delta_0 = 1$ for the first trial, the corresponding *K-polynomial* is obtained from (52) as follows;

$$\delta_k(s, \tau_f = 0.01) = s^3 + 900s^2 + 2.7\times10^5 s + 2.7\times10^7. \quad (56)$$

The step response of the transfer function, $H_k(s, \tau_f = 0.01) = 2.7\times10^7/\delta_k(s, \tau_f)$, is shown in Fig. 19. It has no overshoot but the settling time of 1 % is $28[msec]$.
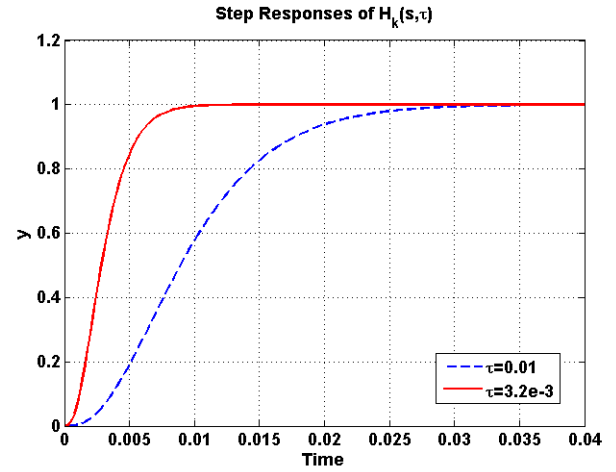

Fig. 19. Step responses of $H_k(s)$s with two τs.

It has been demonstrated in [18] and [19] that the speed of the step response of a linear all pole system can be controlled by adjusting the generalized time constant (τ) only if all of its characteristic ratios are unchanged. The smaller the value of τ, the faster the settling time becomes while its maximum overshoot holds the same. Suppose that $H_k(s, \tau_f)$ gives rise to a settling time of t_{sf}. According to the results in [18] and [21], the value of τ_d for $H_k(s, \tau_d)$ to have the desired settling time, t_{sd}, can be determined by

$$\tau_d = \frac{t_{sd}}{t_f} \tau_f. \quad (57)$$

Since the desired settling time should be less than $10[msec]$, we choose $t_{sd} = 9[msec]$. The above equation results in the following τ_d.

$$\tau_d = \frac{9\times10^{-3}}{28\times10^{-3}} \ (0.01) = 3.2\times10^{-3}.$$

Using (52) associated with α_1, α_2, and τ_d, the following *K-polynomial* is obtained.

$$\delta^*(s, \tau_d) = s^3 + 2.8125\times10^3 s^2 + 2.637\times10^6 s + 8.24\times10^8. \quad (58)$$

The step response of the transfer function, $H_k(s, \tau_d) = 8.24\times10^8/\delta^*(s, \tau_d)$, is also shown in Fig. 19. It is evident that $H_k(s, \tau_d)$ is non-overshooting and that it has a settling time of $9[msec]$. If the complex variable s in (58) is replaced by w, (58) is identical to (43). Fig. 11 shows the reference input i_s^* and the output i_s of the closed loop transfer function in (33) of which the denominator has been transformed by $\delta^*(w)$. So, we confirm that the resulting current controller exhibits non-overshooting and a settling time of about $8.3[msec]$.

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