Comparison of TDC Circuit Design Method to Constant Delay Time

Jin-Ho Choi, *Member, KIMICS*

***Abstract*— This paper describes the design method of Time-to-Digital Converter(TDC) to obtain the constant delay time and good reliability. The reliability property is described with delay elements. In TDC the time signal is converted to digital value which is based on delay elements for the time interpolation. To obtain the constant delay time, the first and the last delay elements have different structure compared to the middle delay elements. In the first and the last delay elements, the driving ability could be controlled for the different delay time. The delay element can be designed by analog and digital devices. The delay time of the element using analog devices is not sensitive to process parameters than that of the element using digital devices. And the TDC circuit by the elements using analog devices shows better reliability than that by the elements using digital devices also.**

***Index Terms*— time-to-digital converter, analog delay element, digital delay element, load balancing, process variation.**

I. INTRODUCTION

TIME interval digitization is an important technique and it has been widely used in many applications such as laser range finder, frequency analysis or phase analysis[1]-[3]. A kind of CMOS TDC with a cyclic delay line was represented the linearity is greatly improved[3]-[5]. But there is a serious disadvantage the reference pulse is required for calibration in case of using digital delay element.

In this paper, the structure of the TDC circuit is introduced to obtain the same delay time in all the delay elements. And the TDC circuits are implemented using two different delay elements type, analog and digital delay element. The characteristics of the TDC using analog and digital delay elements are introduced in the viewpoint of the process variation. In case of digital delay element the number of digital devices has to be controlled to adjust the delay time. And in case of using analog delay element the current for charging and discharging has to be controlled.

In Section II the operation of the TDC circuit is described. In Section III the structure of the TDC circuit is described to obtain the same delay time and the simulation results are presented. Section IV the reliability characteristic of the TDC circuit is described with the delay element type. Finally, the conclusions show in Section V.

II. OPERATION OF TDC CIRCUIT

Fig. 1 shows the block diagram of the conventional TDC circuit[3,5,6]. The TDC circuit is composed of delay element, flip flop and logic circuit. After t1 sec. the output signal of delay element, D_0, is high if the delay time of D_0 element is t1 sec. And after (n-2)t1 sec. the output signals of from D_0 to D_{N-1} elements are high. When the stop signal is high the output signal of delay elements is memorized in D flip flops[7].

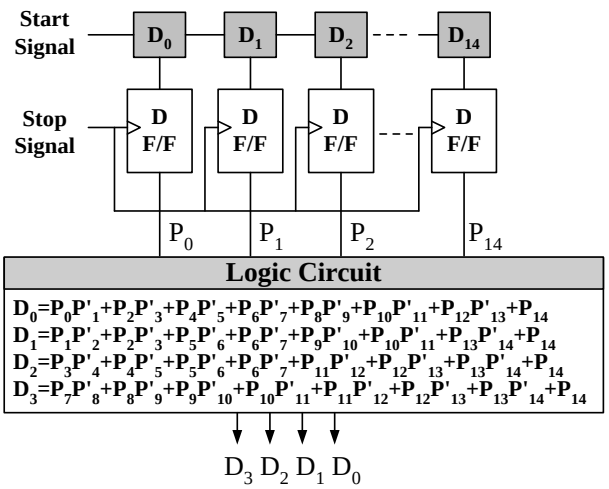

Fig. 1 Block diagram of the TDC circuit.

The digital values, D_0, D_1, D_2 and D_3, are obtained through the logic circuit from the flip flop outputs.

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Jin-Ho Choi is with the Department of Embedded IT, Pusan University of Foreign Studies, Busan, 608-738, Korea (Email: jhchoi@pufs.ac.kr)

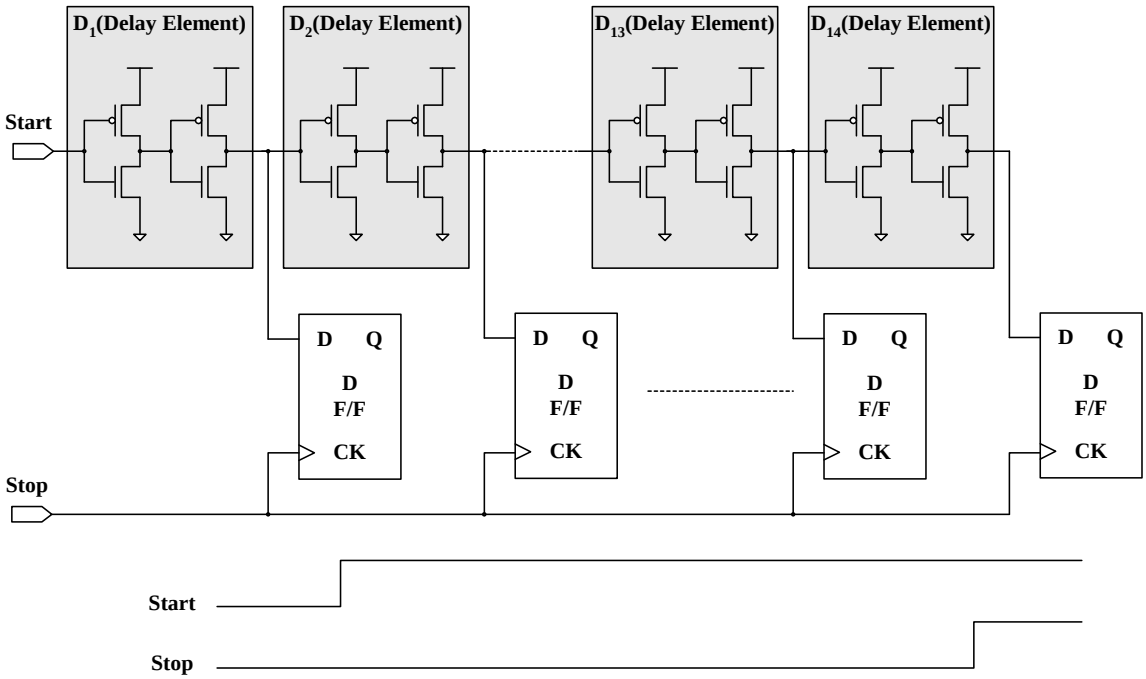


Fig. 2 TDC circuit with digital delay element

Fig. 2 shows the TDC circuit with the digital delay elements and the time signal is converted to 3 bits digital value. The output of delay elements shows in Fig. 3. The delay time of D_0 delay element is about 144 psec. and the delay time of the last delay element, D_{14}, is about 100psec. The delay time is different compared to the delay time of the middle delay elements from D_2 to D_{13}.

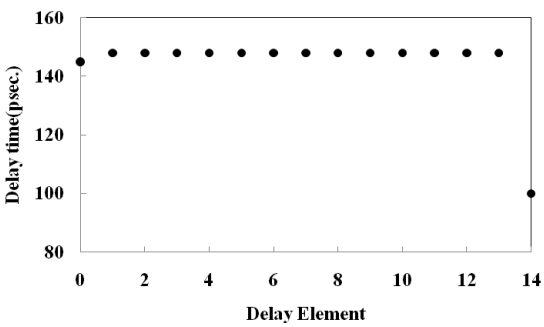
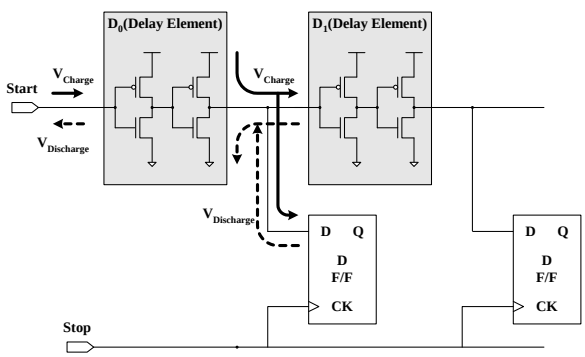


Fig. 3 digital delay element using NOT gates.

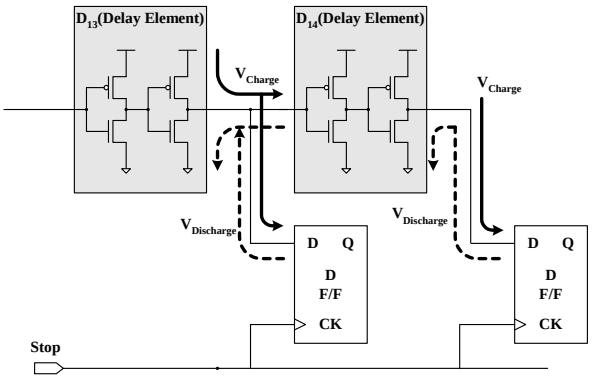
Fig. 4(a) shows the first and second delay elements circuit block. When the start signal is applied D_0 delay element is charged or discharged by the external source, start signal. But D_1 delay element is charged or discharged by the D_0 delay element. Therefore the charge time and discharge time are different because the drivability of D_0 delay element and the start signal source is different.

Fig. 4(b) shows the last delay element circuit block. In D_{13} delay element the load is the same compared to the middle delay elements. But the load of the last delay element, D_{14} delay element, is different because the load is different to drive. Thereby the delay time reduces as shown in Fig. 3. To obtain the same delay time in the first and the last delay elements the delay elements are modified as shown in Fig. 5.

The drive balancing circuit has to be controlled with the source of the start signal. The load balancing circuit has to be controlled to have the same load in the last delay element, D_{14}. This can be easily resolved by adding dummy delay element.



(a)



(b)

Fig. 4 The charge and discharge of the first and the last delay elements (a) the first delay element (b) the last delay element.

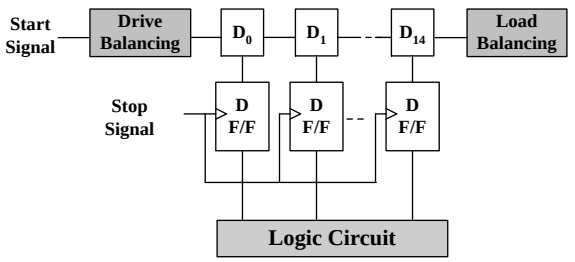


Fig. 5 TDC circuit to obtain constant delay time

III. STRUCTURE OF TDC CIRCUIT

The simple analog delay element proposed by Poki Chen in 1997[7]. Fig. 6 shows the analog delay element and the bias circuit is added to obtain the constant delay time.

In analog delay element the reference current is approximately expressed as follows:[8]

$$I_{REF} \cong \frac{V_{TN}}{R}\left(\frac{W_4 / L_4}{W_2 / L_2}\right) \quad (1)$$

where V_{TN} is the NMOS threshold voltage, W_4 and L_4 are the channel width and length of MP4. And W_2 and L_2 are the channel width and length of MP2. The delay time can be decided by controlling I_{REF}.

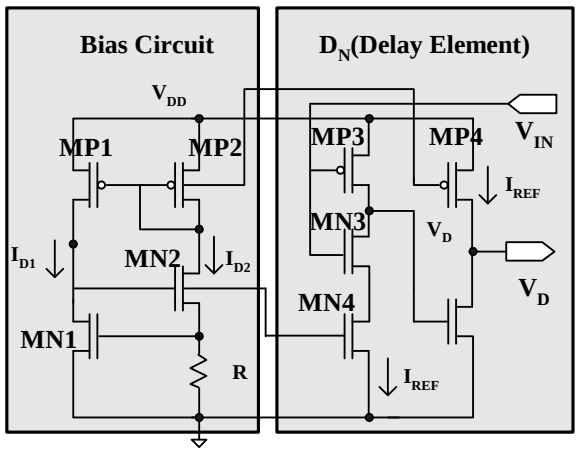
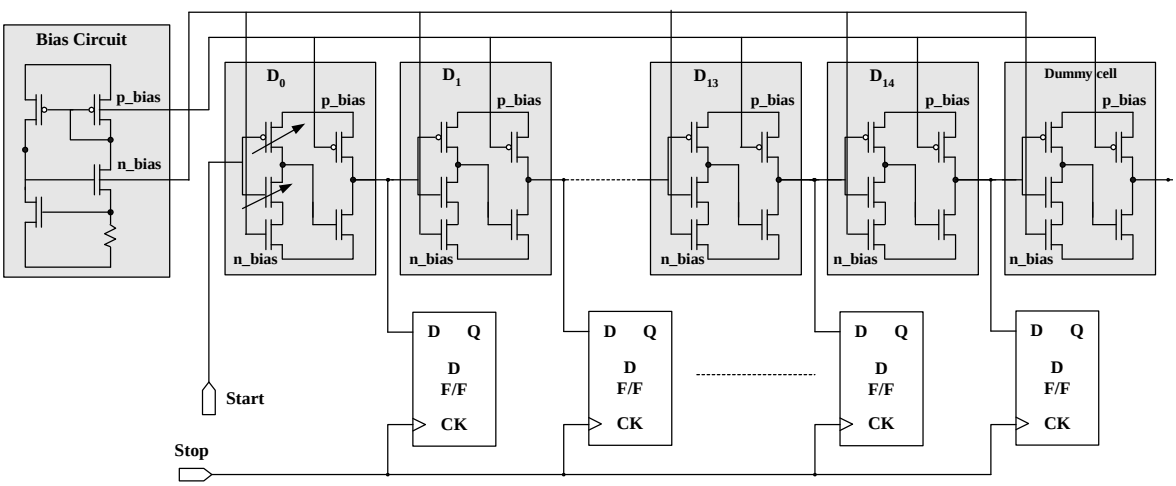
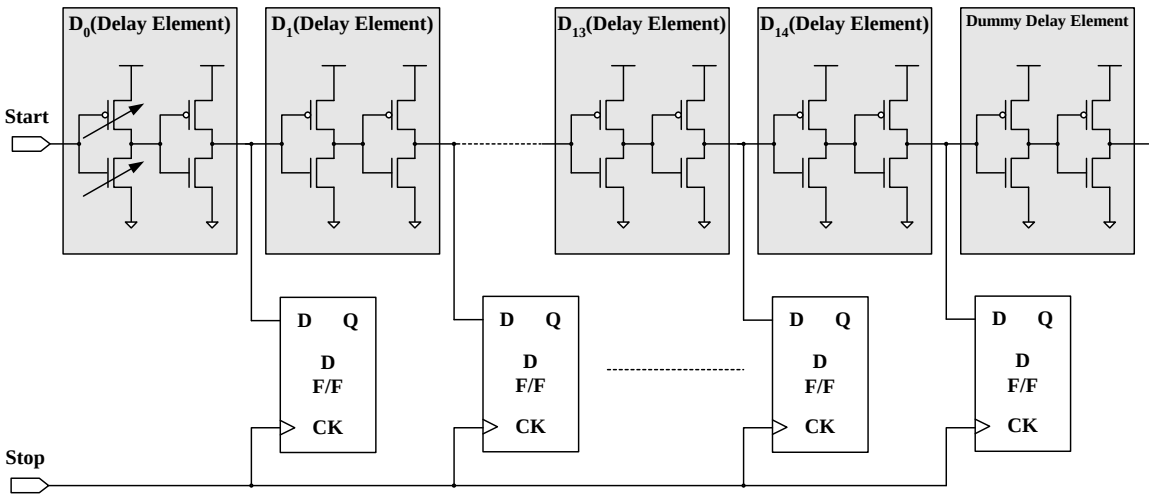


Fig. 6 analog delay element

Fig. 7 shows the TDC circuit using the digital and analog delay elements. To obtain the same delay time the channel widths of NMOS and PMOS are controlled in the first delay element, D_0. And the dummy delay cell is added to have the same delay time in the last delay element, D_{14}.

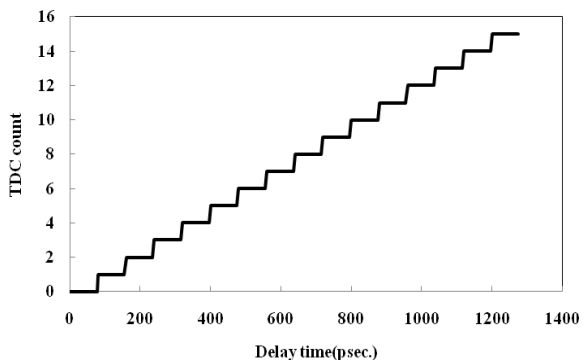


(a)

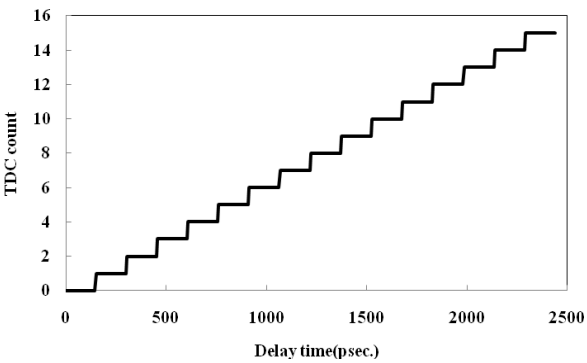


(b)

Fig. 7 TDC output as function of the input time (a) analog delay element (b) digital delay element



(a)



(b)

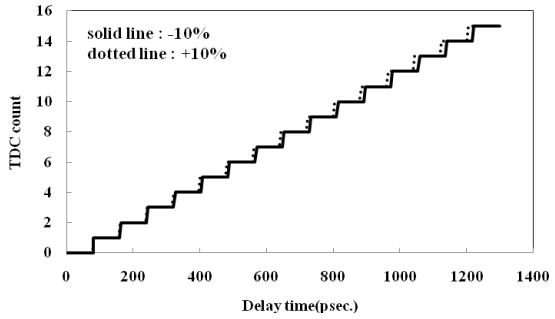
Fig. 8 TDC count output with delay element (a) analog delay element (b) digital delay element.

Fig. 8 shows the TDC output with delay element type as a function of the input signal time.

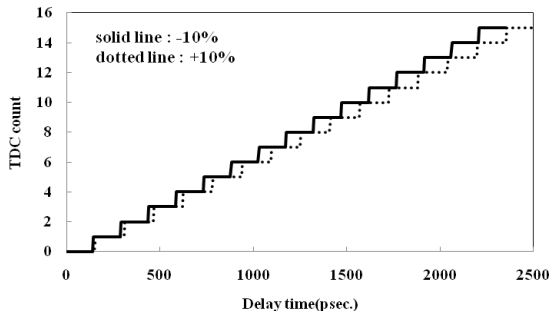
IV. CHARACTERISTICS OF TDC WITH CHANNEL WIDTH VARIATION

Fig. 9 (a) and (b) show the TDC count output when the channel width is varied from -10% to +10% compared to layout. In the analog delay element, the TDC count reaches 15 when the difference of the start time and the stop time is about 1280psec. in case of 10% channel width increase. And the TDC count reaches 15 when the difference of the start time and the stop time is about 1299psec. in case of 10% channel width decrease. The difference is about 19psec when the channel width is ±10% varied and the variation rate is about 1.47%.

In case of the digital delay element, when the channel width increases 10% the TDC count reaches 15 when the difference of the start time and the stop time is about 2359psec. And the TDC count reaches 15 when the difference of the start time and the stop time is 2212psec. in case of the 10% decrease of the channel width. The difference is about 147psec when the channel width is ±10% varied the variation rate is 6.47%.



(a)



(b)

Fig. 9 TDC output as function of the channel width variation (a) analog delay element (b) digital delay element.

From the simulation results when the analog delay element is used the TDC count output shows the stable characteristics with the channel width variation. Therefore the good reliability can be obtained when the analog delay element compared to the digital delay element.

If the bias resistor is fabricated in external the delay time of the analog delay element can be controlled by the trimming of the resistor.

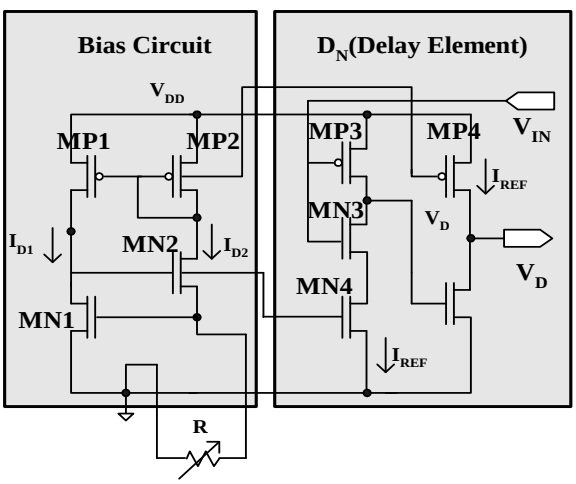


Fig. 10 TDC circuit for controlling the delay time.

The calibration of the delay time is an important point in the TDC circuit after the fabrication of the TDC circuit. The TDC count output can be calibrated easily by the trimming the resistor if the bias resistor is in the outside of chip. In case of Fig. 9(a) the same TDC characteristics can be obtained by 2.8% trimming of the bias resistor when the channel width is ±10% varied .

IV. CONCLUSIONS

A CMOS TDC has been presented with the digital and analog types of the delay element. The TDC circuit was designed by 0.5μm CMOS process and simulation carried out with HSPICE. To obtain the same delay time the drive balancing circuit and the load balancing circuit have to be added in all delay elements. After the TDC fabrication when the channel width or length is changed from the layout condition the TDC using analog delay element shows more stable characteristics compared to the digital delay element. Also the calibration of the delay time can be carried out easily by the trimming of the bias resistor.

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Jin-Ho Choi (M'85–SM'87–F'92) received the B.S. degree in electronics from Busan University in 1985, and the M.S. degree in electronics from KAIST in 1987. He received the Ph. D. degree in electronics from KAIST in 1992. From 1992 to 1996, he was a researcher at Hynix Semiconductor Inc.. Since 1996, he has been a professor in Dept. of Computer Engineering, Pusan University of Foreign Studies. His research interest includes VLSI design.