Design of DGMOSFET for Optimum Subthreshold Characteristics using MicroTec

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Abstract— **We have analyzed channel doping and dimensions(channel length, width and thickness) for the optimum subthreshold characteristics of DG(Double Gate) MOSFET based on the model of MicroTec 4.0. Since the DGMOSFET is the candidate device to shrink short channel effects, the determination of design rule for DGMOSFET is very important to develop sub-100nm devices for high speed and low power consumption. As device size scaled down, the controllability of dimensions and oxide thickness is very low. We have analyzed the short channel effects for the variation of channel dimensions, and found the design conditions of DGMOSFET having the optimum subthreshold characteristics for digital applications.**

Index Terms— **design conditions, DGMOSFET, channel length, channel dimension, subthreshold characteristics, threshold voltage.**

I. INTRODUCTION

AS CMOS device comes into sub-100nm era, the short channel effects(SCEs) become very strong obstacles to develop CMOM devices for high speed and low power consumption.[1] The SCEs mostly occur because of variation of electric fields due to small size, and the category of SCEs is the increasing of subthreshold swing, threshold voltage roll-off, DIBL(Drain Induced Barrier Lowing) and so forth. The subthreshold current depends exponentially on gate voltage, and dependence of logarithm of subthreshold current and gate voltage is linear. The slope of this graph is subthreshold swing. The threshold voltage depends on channel length and width when the channel length or width is reduced to dimensions comparable to the edge-affected region, and this dependence is threshold voltage roll-off. DIBL occurs since the electric fields from the drain also cause barrier lowing near source.[2]

In this paper, we have investigated subthreshold swing, threshold voltage roll-off for the variation channel dimensions to develop design rule of DGMOSFET using the transport models of MicroTec 4.0.[3]

Semiconductor device modeling has become a standard design tool in the microelectronics industry. A few years ago this modeling was performed primarily on supercomputers. At the present time a number of commercial 2D process and device simulators are available, mostly for UNIX based workstations. Normally they require tens of Mbytes of memory even for modest sized meshes. Increasing performance and widespread availability of IBM PCs and compatibles encourage the development of software tools that can be used for 2D modeling of semiconductor devices and processes with a rather low memory capacity and speed of computation. Recently a few efficient programs were developed for two-dimensional semiconductor process-device simulation on a PC which have now been integrated together into a package. MicroTec of Siborg is simple, but valuable models is included . We use this package to discuss design rule of DGMOSFETs.

MicroTec allows 2D silicon process modeling including implantation, diffusion and oxidation and 2D steady-state semiconductor device simulation like MOSFET, DMOS, JFET, BJT, IGBT, Schottky, photosensitive devices etc. Although MicroTec is significantly simplified compared to widely available commercial simulators, it nevertheless is a very powerful modeling tool for industrial semiconductor process/device design. In many instances MicroTec outperforms existing commercial tools and it is remarkably robust and easy-to-use.

Despite its apparent simplicity, MicroTec covers all the basic needs of semiconductor process/device design complemented with efficient and flexible graphics tools. It is much easier to use than any other tool of its kind. MicroTec is a must for those who want to understand physics of semiconductor devices without knowing much about computers or numerical methods and who do not have much time for learning new process/device simulation tools. MicroTec is an excellent tool for managers, R&D engineers, students, professors and researchers and can be referred to as a TCAD calculator.

Section II explains simulation process using MicroTec and transport models, and section III discusses simulation results, and refers the importance of design rule of DGMOSFETs. We conclude in Sec. IV.

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II. SIMULATION PROCESS USING MICROTEC

MicroTec is a shell integrating four programs for silicon process-device simulation

- SiDif : two-dimensional SImulator for DIFfusion and oxidation
- MergIC : program for MERGing fragments of IC elements
- SemSim : two-dimensional steady-state SEMiconductor device SIMulator
- SibGraf : interactive 3D and 2D graphics

It is well known that analytical approximations for doping profiles typically do not adequately reflect results of fabrication processing, especially for devices with submicron dimensions. A program named SiDif has been developed to compute two-dimensional impurity profiles of VLSI elements that have undergone various fabrication steps. The fabrication process may include processing steps such as ion implantation or surface deposition (arsenic, boron or phosphorous) with subsequent annealing under oxidizing or inert ambient. Resulting doping profiles may be used in a straightforward manner to generate the entire structure of a semiconductor device for subsequent evaluation of I-V curves in a few minutes on a PC. The algorithm is based on the finite-difference formulation and a rectangular mesh. The physical model adopted describes the diffusion process for up to three interacting charged impurities in a two-dimensional domain with moving oxide boundary and impurity segregation at the Si/SiO2 interface. In the case of implantation the initial profiles of each impurity are approximated by the conventional Runge's model

MergIC provides an interface between the process simulation tool SiDif and the device simulation tool SemSim. MergIC merges device fragments simulated by SiDif into a device domain to be used in the device simulation. The fragments may be placed arbitrarily in the device domain, symmetrized and replicated. The output file of MergIC serves as the numerical doping input file for SemSim.

SemSim, as well as its predecessors SiMOS and BiSim , is based on the Gummel-like decoupled technique and require only 4 Kbyte of memory for a 10,000 node mesh. A finite difference technique on a rectangular grid is employed. For discretization of the continuity equations the conventional Scharfetter-Gummel approximation is used. Conjugate gradient methods with preconditioning are used for solving the linear systems.

The doping concentration and sub directive for simulated devices are summarized in Table 1. This directive may include any number of DOPA: subdirectives. The analytical doping profiles are described by superposition of wells. For each well is defined by one DOPA: subdirective according to the following formula

$$N_{well} = N_0 \exp(-(\frac{f(x_l - x)}{L_x})^2 - (\frac{f(x - x_r)}{L_x})^2 - (\frac{f(y - y_b)}{L_y})^2 - (\frac{f(y_t - y)}{L_y})^2) \quad (1)$$

The concentration in every well is a constant equal N_0 in the rectangle X_{left}, X_{top}, X_{right}, Y_{bottom} and decreases as a Gaussian beyond the rectangle N_0 is the maximum concentration in the well, it is positive for donors and negative for acceptors.

TABLE I
dOPING CONCENTRATION AND SUB DIRECTIVE FOR SIMULATED DEVICES

Description \ Name	Drain	Source	Top Gate	Bottom Gate	Channel
Maximum concentration in the doping well.(cm^{-3})	10^{19}	10^{19}	10^{19}	10^{19}	-10^{15}
Left edge of the doping well.(μm)	0	0.06	0.03	0.03	0.03
Right edge of the doping well. (μm)	0.02	0.08	0.05	0.05	0.05
Top of the doping well. (μm)	0.006	0.006	0	0.014	0.01
Bottom of the doping well. (μm)	0.016	0.016	0.008	0.0221	0.012

III. SIMULATION AND RESULTS

The schematic diagram of DGMOSFET is shown in Fig. 1. The bias of two gates is determined by independent bias conditions, and the threshold voltage is defined as top gate voltage when drain current is 10^{-6}A. Deep contact needs for source and drain contact in MicroTec simulation. The channel length L_g is varied from 10nm to 100nm, and channel thickness t_{si} from 10nm to 30nm according to channel length, and oxide thickness from 1nm to 3nm. The doping concentration of channel is fixed with $10^{15} cm^{-3}$ p-type.

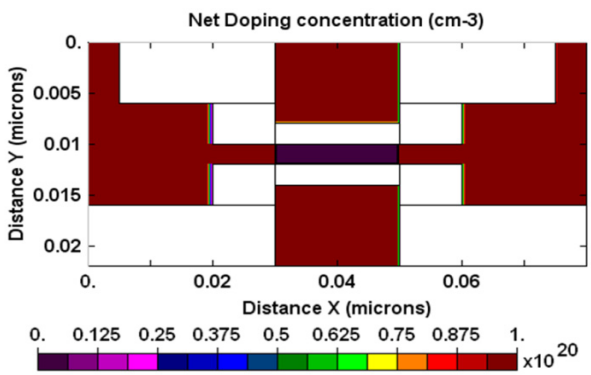

Fig. 1 Schematic diagram of DGMOSFET in MicroTec.

Figure 2 shows threshold voltage as a function of channel thickness with a variation of oxide thickness. Note the relation of threshold voltage and channel thickness is nearly linear. We show the absolute value of threshold voltage is increasing with increasing of channel thickness. Also threshold voltage variation is large when gate oxide thickness is small. Given decreasing gate oxide thickness, the absolute value of threshold voltage is increasing. As shown in Fig. 2, the variations of threshold voltage is large when channel thickness increases due to SCE in thick channel thickness, and the variation of threshold voltage according to gate oxide thickness is trivial at small channel thickness. So we know small channel thickness has to be used to design of DGMOSFET for small and consistent threshold voltage. The process is very difficult to make thin channel thickness.

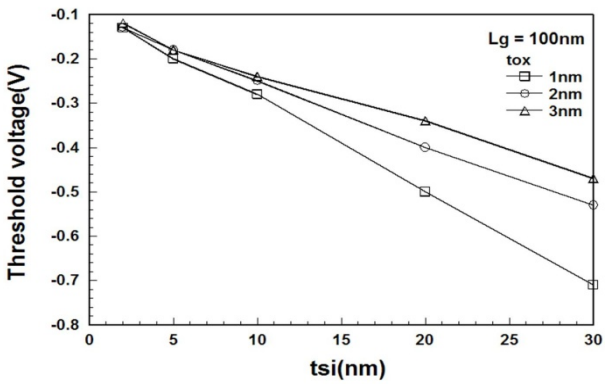

Fig. 2 Threshold voltage as a function of channel thickness with a variation of oxide thickness from 1nm to 3nm

Figure 3 shows subthreshold swing as a function of channel thickness with a variation of oxide thickness. As shown in Fig. 3, the variations of subthreshold swing is large due to SCE in thick channel thickness when channel thickness increases, and the variation of subthreshold swing according to gate oxide thickness is trivial at small channel thickness. So we know small channel thickness has to be used to design of DGMOSFET for small and consistent subthreshold swing. Note the relation of subthreshold swing and channel thickness is nearly linear. Also the variation of subthreshold swing is large at lower gate oxide thickness. Therefore small channel thickness and thick gate oxide thickness is needed to design DGMOSFET having lower subthreshold swing. Given increasing of channel thickness, the conduction of free electron is not confined to the channel center and the effective conduction path must be between surfaces and channel center since the controllability of gate voltage for spreading of carrier is weak with increasing of channel thickness. .[4]

Figure 4 shows subthreshold swing as a function of channel length with a variation of oxide thickness from 1nm to 3nm for 2nm of channel thickness. The subthreshold swings is nearly constant above gate length of 20nm regardless of gate oxide thickness, but increases rapidly below gate length of 20nm. Figure 4 shows specially rapid increase when gate oxide thickness increases.

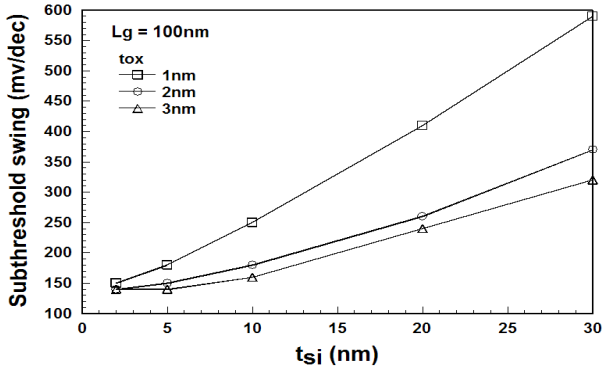

Fig. 3 Subthreshold swing as a function of channel thickness with a variation of oxide thickness from 1nm to 3nm

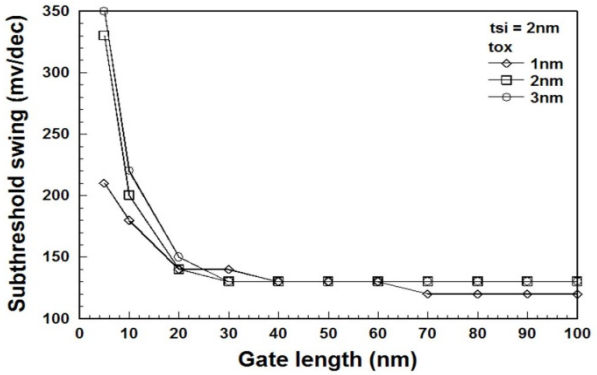

Fig. 4 Subthreshold swing as a function of channel length with a variation of oxide thickness from 1nm to 3nm for 2nm of channel thickness

To compare with the subthreshold swings for channel thickness, we have obtained the subthreshold swings for 10nm of channel thickness in the same conditions for other parameters, as shown in Fig. 5.

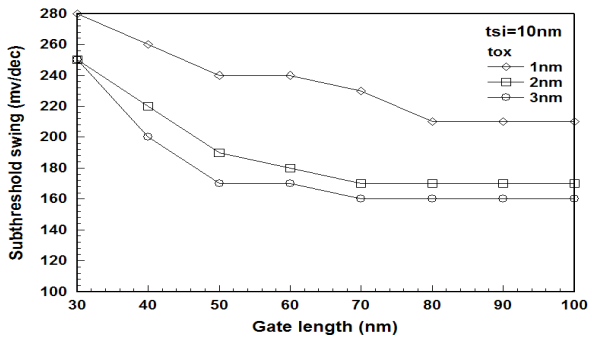

Fig. 5 Subthreshold swing as a function of channel length with a variation of oxide thickness from 1nm to 3nm for 10nm of channel thickness

As known in comparison of Fig. 4 and Fig. 5, the subthreshold swings of DGMOSFETs having thick channel thickness is variable for gate oxide thickness. In case of thick channel thickness, subthreshold swings are not converged even if gate length increases. Note thin channel thickness needs to control subthreshold swings. To analyze DGMOSFET having nano scale channel length and thickness, width dimension is not trivial. So we know nano scale simulation needs 3D model.[5]

IV. CONCLUSIONS

A analysis of subthreshold characteristics have been derived to design optimum DGMOSFETs using MicroTec. The simulator explains channel thickness, length and oxide thickness dependence of subthreshold swing and threshold voltage. We know the variations of threshold voltage is large with increasing channel thickness and the variation of threshold voltage according to gate oxide thickness is neglected at small channel thickness. Note the variation of subthreshold swing with gate oxide thickness is also neglected at small channel thickness, and the subthreshold swings is nearly constant above gate length of 20nm regardless of gate oxide thickness The results in this study can use to design optimum DGMOSFET.

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