A Study on Counter Design using Sequential Systems based on Synchronous Techniques

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***Abstract*— This paper presents a method of design the counter using sequential system based on synchronous techniques. For the design the counter, first of all, we derive switching algebras and their operations. Also, we obtain the next-state functions, flip-flop excitations and their input functions from the flip-flop. Then, we propose the algorithm which is a method of implementation of the synchronous sequential digital logic circuits. Finally, we apply proposed the sequential logic based on synchronous techniques to counter.**

***Index Terms*— *sequential logic systems, synchronous techniques, switching algebra, next-state function, flip-flop excitation, counter design*.**

Ⅰ. INTRODUCTION

The digital logic system(DLS) is classified into combinational digital logic systems(DCLS) and sequential digital logic systems(SDLS). In specially, the research of the sequential digital circuits was researched by many schaloar[1-7]. Thurman A. Iriving etc.[8] realize the flip-flop using the cycle operator and the variable operator, and Anthony S. Wojcik etc.[9] realize the asynchronous module using by the basic binary circuit design techniques. Also, L.P. Maguire[10] introduce the flip-flop that is constructed with fuzzy and higher valued concepts. and R.Drechsler etc.[11] introduce the fault simulation for the sequential networks.

In digital circuit theory, sequential logic is a type of logic circuit whose output depends not only on the present input but also on the history of the input. This is in contrast to combinational logic, whose output is a function of, and only of, the present input. In other words, sequential logic has storage (memory) while combinational logic does not. Sequential logic is therefore used to construct some types of computer memory, other types of delay and storage elements, and finite state machines. Most practical computer circuits are a mixture of combinational and sequential logic. There are two types of finite state machine that can be built from sequential logic circuits: Moore machine: the output depends only on the internal state. Mealy machine: the output depends not only on the internal state, but also on the inputs. Nearly all sequential logic today is 'clocked' or 'synchronous logic' logic: there is a 'clock' signal, and all internal memory (the 'internal state') changes only on a clock edge. The basic storage element in sequential logic is the flip-flop. The main advantage of synchronous logic is its simplicity. Every operation in the circuit must be completed inside a fixed interval of time between two clock pulses, called a 'clock cycle'. As long as this condition is met (ignoring certain other details), the circuit is guaranteed to be reliable. Synchronous logic also has two main disadvantages, as follows. 1st, The clock signal must be distributed to every flip-flop in the circuit. As the clock is usually a high-frequency signal, this distribution consumes a relatively large amount of power and dissipates much heat. Even the flip-flops that are doing nothing consume a small amount of power, thereby generating waste heat in the chip. 2nd, The maximum possible clock rate is determined by the slowest logic path in the circuit, otherwise known as the critical path. This means that every logical calculation, from the simplest to the most complex, must complete in one clock cycle. One way around this limitation is to split complex operations into several simple operations, a technique known as 'pipelining'.

This technique is prominent within microprocessor design, and helps to improve the clock rate of modern processors. In digital electronics, a clocked sequential system is a system whose output depends only on the current state, whose state changes only when a global clock signal changes, and whose next-state depends only on the current state and the inputs. Nearly all digital electronic devices (microprocessors, digital clocks, mobile phones, cordless telephones, electronic calculators, etc.) are designed as clocked sequential systems. Notable exceptions include digital asynchronous logic systems. In particular, nearly all computers are designed as clocked sequential systems. Notable exceptions include analog computers and clockless CPUs. Typically each bit of the "state" is contained in its own flip-flop.

Combinational logic decodes the state into the output signals. More combinational logic encodes the current state and the inputs into the next-state signals. The next-state signals are latched into the flip-flops under the control of the global clock signal (a wire connected to every flip-flop). A clocked sequential system is a kind of Moore machine.

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In this paper, we presented the design method using sequential logic based on synchronous techniques.

II. SWITCHING ALGEBRA

The sequential digital logic switching algebra and its operation that are used in this paper is as following.

For the higher valued(H) logic, we define the AND, OR and Literal operator.

AND : $\alpha \bullet \beta = \min(\alpha,\beta)$
OR : $\alpha + \beta = \max(\alpha,\beta)$
Literal : $X^{[\alpha+\beta]}$ = H-1 iff $\alpha \le X \le \beta$
0 iff otherwise

In special case of $\alpha=\beta$, we define Literal operator is $X^{[\alpha]}$ or $X^{[\beta]}$.

Complement : $[\alpha]^c = (H-1)- \alpha$
Cycle : $\alpha \rightarrow^{\beta} = \alpha$ plus β(mod H)
where, $\alpha, \beta \in \{0, 1, 2, \ldots\ldots, H-1\}$

Ⅲ. FLIP-FLOP

The basic electronic device of the sequential digital logic circuits is the flip-flop which is like as the basic gates in combinational circuits.

That is to say, the flip-flop operates like memory or delay devices. Therefore, in order to design the sequential digital logic circuits, first we construct the flip-flop. The H-state flip-flop which is used in this paper is represented following figure 1.

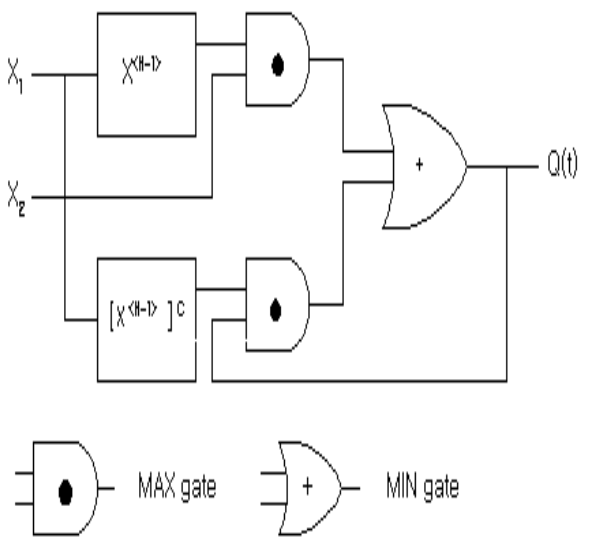

Fig. 1. H-state flip-flop

The other hand, the sequential circuit operates with the present time input as well as the previous time output.

So, we must derivate the equation which represents the relationship between the present time input and the previous time output simultaneously.

This is named by the next-state transition function and denoted following equation (1).

$$Q(t+1)=X_1^{[H-1]} \bullet X_2 + [X_1^{[H-1]}]^C \bullet Q(t) \quad (1)$$

Also, we obtain the next-state transition table which is represented the characteristics of the sequential logic systems using by switching algebras and figure 1.

This next-state transition table is represented following in table 1. And we obtain the higher valued logic sequential circuit excitation table based on the table 1. It is represented in table 2.

TABLE 1.
THE NEXT-STATE TABLE

X_1 / X_2	0 0 ..... 0 0 1 ... .. H-1	1 1 ..... 1 0 1 ..... H-1
0	0 0 0	0 0 0
1	1 1 1	1 1 1
⋮	⋮	⋮
H-1	H-1 H-1 ..... H-1	H-1 H-1 ..... H-1

continued

X_1 / X_2	2 2 ..... 2 0 1 ..... H-1	3 3 ..... 3 0 1 ..... H-1
0	0 0 0	0 0 0
1	1 1 1	1 1 1
⋮	⋮	⋮
H-1	H-1 H-1 ..... H-1	H-1 H-1 ..... H-1

continued

X_1 / X_2	....	H-1 H-1 ..... H-1 0 1 ..... H-1
0	0 0 0	0 0 0
1	1 1 1	1 1 1
⋮	⋮	⋮
H-1	H-1 H-1 ..... H-1	0 1 ..... H-1

TABLE 2.
THE EXCITATION TABLE.

Q(t)	0	1 1 1
Q(t+1)	0	1 2 ..... N-1
X_1	d N-1	N-1 N-1 ..... N-1
X_2	d^* 0	1 2 ..... N-1

continued

Q(t)	1	1	1 1 1
Q(t+1)	0	1	2 3 ..... H-1
X_1	H-1	d H-1	H-1 H-1 ..... H-1
X_2	0	d^* 1	2 3 .... H-1

continued

Q(t)	.....	H-1 H-1 H-1	H-1
Q(t+1)		0 1 2	H-1
X_1	.....	H-1 H-1 H-1	d H-1
X_2		0 1 2	d^* H-1

where, d=0, 1, 2, ... , H-2 d^*=0, 1, 2, ... , H-1

Therefore, we can represent the equation (2) with equation (1) using by the next-state table 1 and the excitation table 2 of the higher valued logic sequential circuits.

$$Q(t+1)=I_C^{<N-1>}\cdot X_2 + [I_C^{<N-1>}]^c\cdot Q(t) \quad (2)$$

Ⅳ. ALGORITHM OF SEQUENTIAL LOGIC SYSTEMS BASED ON SYNCHRONOUS TECHNIQUES

In sequential digital logic circuit, we must select the appropriate flip-flop, and implement the synchronous sequential digital circuit with the combinational digital logic circuit gates which is satisfied with expressed contents at the same time. The procedure is as following

First, we describe the verbal description of the synchronous sequential digital circuits, next, we obtain the next-state table based on the next-state of the H-state flip-flop. Also, we obtain the flip-flop excitation table based on the next-state transition table in 2nd , and we obtain the each step's input function after applied to switching algebras. Next, we obtain the next-state function based on the input function in3rd. Finally, we realize the synchronous sequential digital circuits with H-state flip-flop and the basic gates in combinational digital circuits.

The following figure 2 present the algorithm for the implement the higher valued logic sequential logic circuit based on synchronous techniques.

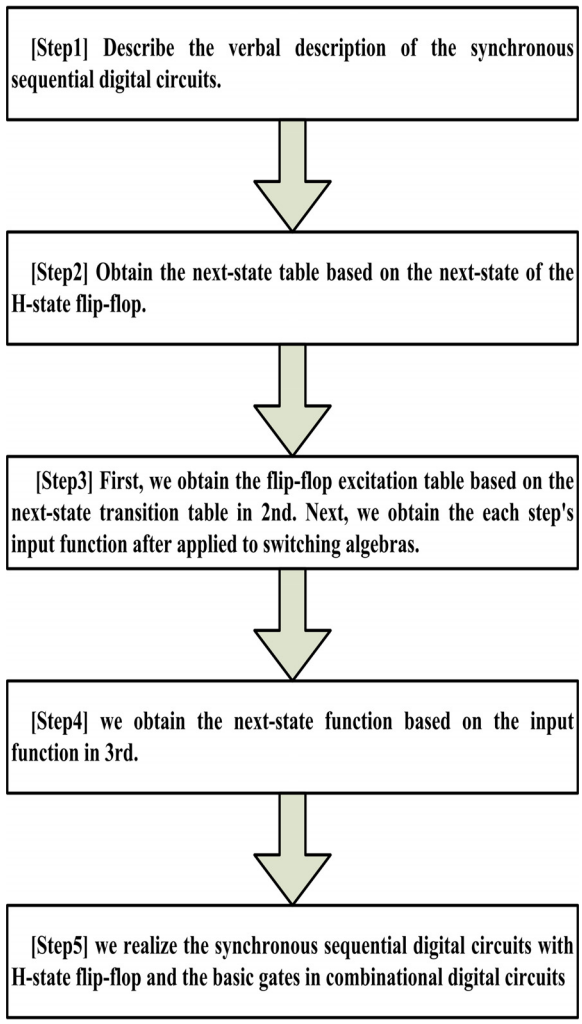

Fig. 2. The algorithm of the implement the higher valued logic synchronous sequential digital circuit.

Ⅴ. COUNTER DESIGN ALGORITHM

In according to the algorithm in Ⅲ, the counter construction procedure is as following, First, we construct the H^m counter, where, H means the higher valued logic and m means the flip-flop stage number. Next, we obtain the next-state table of the higher valued logic flip-flop. Finally, we obtain the excitation table from the next-state table in step 2, we obtain the input function for each stage.

The following figure 3 present the algorithm for the counter design.

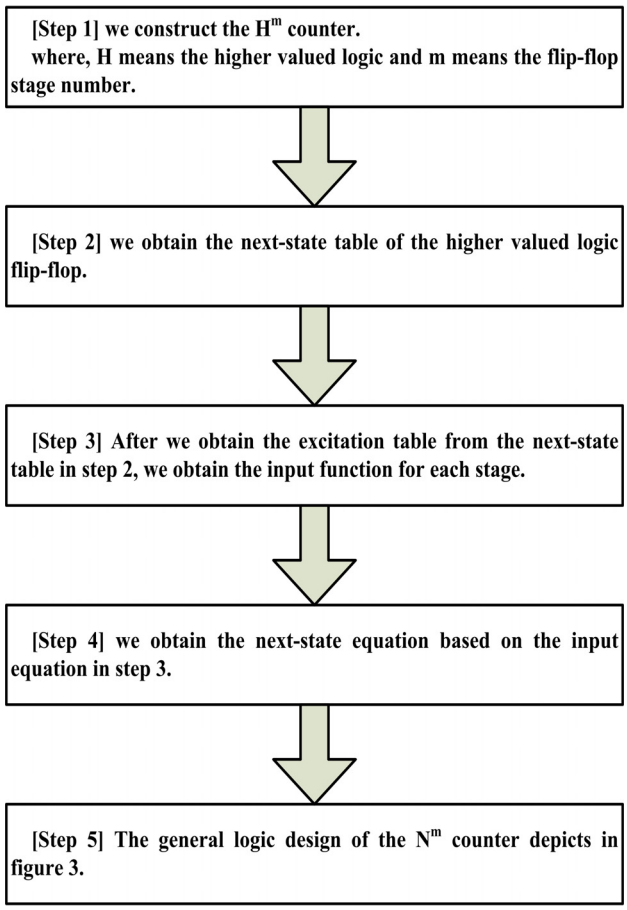

Fig. 3. The algorithm of counter design.

Input equation for the $Q_1(t)$:
$X_{11}=H\text{-}1=I_C$
$X_{12}=Q_1^{\rightarrow 1}(t)$

Input equation for the $Q_2(t)$:
$X_{21}=Q_1(t)$
$X_{22}=Q_2^{\rightarrow 1}(t)$
Input equation for the $Q_3(t)$:
$X_{31}=(Q_1Q_2)(t)^{[H-1]}$
$X_{32}=Q_3^{\rightarrow 1}(t)$

Input equation for the $Q_4(t)$:
$X_{41}=(Q_1Q_2Q_3)(t)^{[H-1]}$
$X_{42}=Q_4^{\rightarrow 1}(t)$

Input equation for the $Q_m(t)$:
$X_{m1}=(Q_1Q_2Q_3 \ldots\ldots Q_{m-1})(t)^{[H-1]}$
$X_{m2}=Q_{m-1}^{\rightarrow 1}(t)$ (3)

where, in X_{ij}, i is in Q_i, j is the 1 and 2 for input X_1 and X_2.

we obtain the next-state equation based on the input equation in step 3.

$$Q_1(t+1)=X_{11}^{[H-1]}\cdot X_{12}+[X_{11}^{[N-1]}]^C\cdot Q_1(t)$$
$$=I_C^{[H-1]}\cdot Q_1^{\rightarrow 1}(t)+[I_C^{[H-1]>}]^C\cdot Q_1(t)$$
$$Q_2(t+1)=X_{21}^{[H-1]}\cdot X_{22}+[X_{21}^{[H-1]}]^C\cdot Q_2(t)$$
$$=Q_1(t)^{[H-1]}\cdot Q_2^{\rightarrow 1}(t)+[Q_1(t)^{[H-1]}]^C\cdot Q_2(t)$$

$$Q_3(t+1)=X_{31}^{[H-1]}\cdot X_{32}+[X_{31}^{[H-1]}]^C\cdot Q_3(t)$$
$$=(Q_1Q_2)(t)^{[H-1]}\cdot Q_3^{\rightarrow 1}(t)+[(Q_1Q_2)(t)^{[H-1]}]^C\cdot Q_3(t)$$

$$Q_4(t+1)=X_{41}^{[H-1]}\cdot X_{42}+[X_{41}^{[H-1]}]^C\cdot Q_3(t)$$
$$=(Q_1Q_2Q_3)(t)^{[H-1]}\cdot Q_4^{\rightarrow 1}(t)+[(Q_1Q_2Q_3)(t)^{[H-1]}]^C\cdot Q_4(t)$$
$$\vdots$$
$$\vdots$$
$$\vdots$$
$$Q_m(t+1)=X_{m1}^{[H-1]}\cdot X_{m2}+[X_{m1}^{[H-1]}]^C\cdot Q_m(t)$$
$$=(Q_1Q_2Q_3 \ldots\ldots Q_{m-1})(t)^{[H-1]}\cdot Q_m^{\rightarrow 1}(t)$$
$$+[(Q_1Q_2Q_3 \ldots\ldots Q_{m-1})(t)^{[H-1]}]^C\cdot Q_m(t) \quad (4)$$

The equation (3) and (4) represent the each general input and next-state equation.

The general logic design of the N^m counter depicts in figure 4.

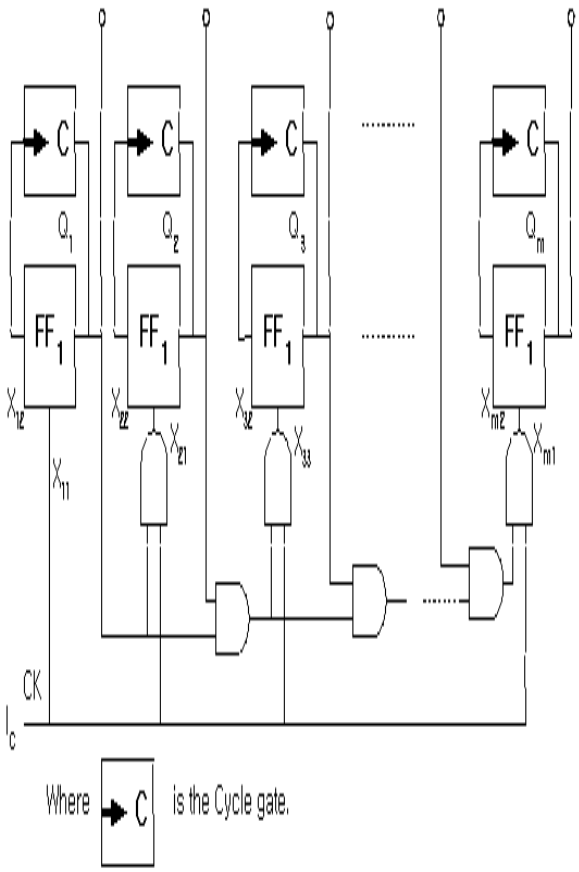

Fig. 4. The general logic design of the N^m counter.

Ⅵ. APPLICATIONS

In this section, we construct 3^3 counter in according to the algorithm of constructing the N^m counter.

[Step 1] In this example, H=3 and m=3

[Step 2] The next-state table for the flip-flop is depicted in table 3.

TABLE 3.
THE NEXT-STATE TABLE

X_1		0	0	0	1	1	1	2	2	2
X_2		0	1	2	0	1	2	0	1	2
Q(t)	0	0	0	0	0	0	0	1	2	
	1	1	1	1	1	1	0	1	2	
	2	2	2	2	2	2	0	1	2	
		Q(t+1)								

[Step 3] We obtain the excitation table 4 from the table 3. And the input equations are as following.

Input equation for $Q_1(t)$:

$X_{11}=2$

$X_{12}=Q_1^{\rightarrow 2}(t)$ (5)

Input equation for $Q_2(t)$:

$X_{21}=Q_1^{[2]}(t)$

$X_{22}=Q_2^{\rightarrow 1}(t)$ (6)

Input equation for $Q_3(t)$:

$X_{31}=Q_2^{[2]}(t)\cdot {}^1Q_1{}^2$

$X_{32}=Q_3^{\rightarrow 1}(t)$ (7)

[Step 4]: we obtain the state equation.

$Q_1(t+1)=X_{11}^{[2]}\cdot Q_1^{\rightarrow 2}(t) + [X_{11}^{[2]}]^C\cdot Q_1^{\rightarrow 2}(t)$ (8)

$Q_2(t+1)= ({}^1Q_1{}^2)^{[2]}(t)\cdot Q_2(t)+ [({}^1Q_1{}^2)^{[2]}]^C(t)\cdot Q_2(t)$ (9)

$Q_3(t+1)= (Q_2^{[2]\cdot 1}Q_1{}^2)^{[2]}(t)\cdot Q_3(t) + [(Q_2^{<2>\cdot 1}Q_1{}^2)^{[2]}]^C(t)\cdot Q_3(t)$ (10)

[Step 5] The logic design of 3^3 counter is depicted in figure 5.

Ⅶ. CONCLUSION

In this paper, we propose the counter design method using sequential systems based on the synchronous techniques.

First of all, we construct the higher valued logic flip-flop based on higher value sequential switching algebra and its switching functions.

Also, we derivate the next-state transition function using by the higher value sequential switching algebra, and obtain the next-state transition table and the excitation table which represent a characteristics of the sequential circuits. Then, we propose the algorithm of constructing the synchronous sequential circuits. And we derivate the algorithm of the H^m counter construction that is the proposed algorithm application. In the future research, we need the any other application in addition to the counter.

TABLE 4.
THE EXCITATION TABLE

$Q_3(t)Q_2(t)Q_3(t)$	Next-state $Q_3(t+1)Q_2(t+1)Q_3(t+1)$	$Q_1(t)$ X_1X_2	$Q_2(t)$ X_1 X_2	$Q_3(t)$ X_1 X_2
0 0 0	0 0 2	2 2	d d*	d d*
0 0 1	0 1 0	2 0	2 1	d d*
0 0 2	0 1 1	2 1	2 1	d d*
0 1 0	0 1 2	2 2	d d*	d d*
0 1 1	0 2 0	2 0	2 2	d d*
0 1 2	0 2 1	2 1	2 2	d d*
0 2 0	0 2 2	2 2	d d*	d d*
0 2 1	1 0 0	2 0	2 0	2 1
0 2 2	1 0 1	2 1	2 0	2 1
1 0 0	1 0 2	2 2	d d*	d d*
1 0 1	1 1 0	2 0	2 1	d d*
1 0 2	1 1 1	2 1	2 1	d d*
1 1 0	1 1 2	2 2	d d*	d d*
1 1 1	1 2 0	2 0	2 2	d d*
1 1 2	1 2 1	2 1	2 2	d d*
1 2 0	1 2 2	2 2	d d*	d d*
1 2 1	2 0 0	2 0	2 0	2 2
1 2 2	2 0 1	2 1	2 0	2 2
2 0 0	2 0 2	2 2	d d*	d d*
2 0 1	2 1 0	2 0	2 1	d d*
2 0 2	2 1 1	2 1	2 1	d d*
2 1 0	2 1 2	2 2	d d*	d d*
2 1 1	2 2 0	2 0	2 2	d d*
2 1 2	2 2 1	2 1	2 2	d d*
2 2 0	2 2 2	2 2	d d*	d d*
2 2 1	0 0 0	2 0	2 0	2 0
2 2 2	0 0 1	2 1	2 0	2 0

where, d=0, 1 d^*=0, 1, 2

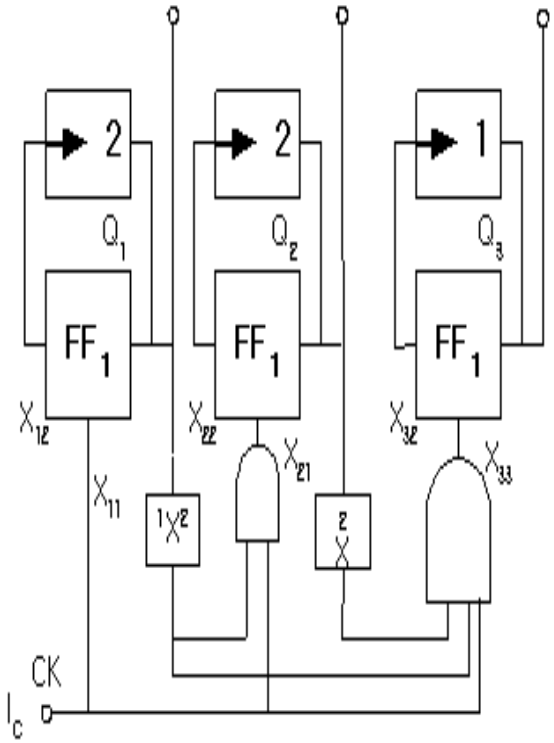

Fig. 5. The logic circuit realization of the counter 3^3.

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