Design of Broadband Impedance Matching Circuit for PLC Coupler using Butterworth Equalizer

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***Abstract*— This paper represents design broadband impedance matching circuit for Coupler to improve power transfer efficiency in the broadband power line communication (BPLC) systems. The Butterworth gain function equalizer is used to design broadband matching circuit. A practical PLC Coupler impedance matching circuit is designed, and the characteristics for S11 and S21 of PLC Coupler are enhanced comparing with unmatched one. This is done by maximizing the power transfer gain from modem to the load.**

***Index Terms*— BPLC (Broadband Power Line Communication), Butterworth Gain Function, Broadband Impedance Matching**

I. INTRODUCTION

Power Line communication (BPLC) are a new type of Power Line communication (PLC) system capable of providing significantly higher data rates than previous PLC systems. BPLC systems consist of terminal devices that are plugged into or attached to the electrical power supply network and allow data to be transmitted via the network to other terminal devices plugged into or attached to the network. The usage of the existing electrical power supply network wiring reduces costs and provides convenient access to broadband interconnection between devices.

In the areas where consumers already have cable modem or asymmetric digital subscriber line modem for internet access, BPLC could provide another broadband medium alternative. Due to the concern of radio frequency emission and interference, the permissible BPLC modem's power injection into power line networks is very limited. If the impedance of a BPLC modem mismatches the load impedance at a power line connection port, the BPLC modem signal power injection into the power line connection port will further be reduced. This will not only limit the BPLC modem signal delivery distance to next BPLC modem hence more repeaters needed, but also will cause the BPLC modem signal reflection (or radio frequency emission) from the power line connection port. The challenge of this research relies on finding a suitable Broadband Impedance Matching (BIM) circuit able to adapt the PLC physical layer to Modem.

An excellent set of explicit formulas for the design of optimum Chebyshev and Butterworth impedance filters based on Youla's theory [1] of broadband matching has been published by W. K. Chen [2].

In this paper, it is shown that the matching networks obtained from Butterworth gain functions for PLC networks. The BPLC signals are in the 0.1~30 MHz band and impedance matching is at the emission port only. The proposed algorithms can be applied to both medium voltage (MV) and low voltage (LV) networks. The aim of this paper is to propose some algorithms for broadband impedance matching for various types of load. Using Butterworth gain functions to design a broadband impedance matching circuit is a quite well known issue. However, adapting the existing algorithms to BPLC networks has never been done before due to a lack of knowledge of the distribution network, especially regarding the impedance of the emission port.

II. BROADBAND IMPEDANCE MATCHING THEORY

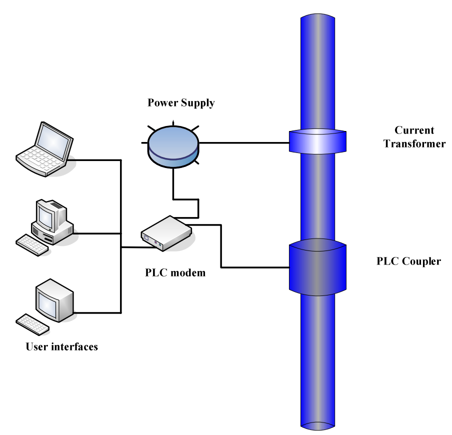

Fig. 1 BPLC communication system

In Fig. 1, the general configuration of PLC system is represented. BPLC modem is connected with standard data terminal such as PC, modulates and demodulates data signal from terminals. The modulated signals from

Manuscript received April 12, 2010; revised May 2, 2010; accepted May 14, 2010.

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modem will magnetically couple with power line through the Coupler, and it is sent to receiving terminal.

Let us consider the real condition of a PLC Coupler connected to the BPLC network according to Fig. 2. In most practical cases, BPLC modem can usually be represented as an ideal voltage source in series with a pure resistor, which may be the Thévenin equivalent of some other network. The load impedance is composed of the parallel combination of a resistor and a capacitor and the in series with an inductor, as shown in Fig. 2, which may include the parasitic effects of a practical device.

It is easy to see that the impedance matching circuit is a two port system to be inserted between the BPLC modem and the BPLC Coupler. The BIM circuit will be called equalizer in the following. We can see that the equalizer is a two port system to be inserted between the source and the load.

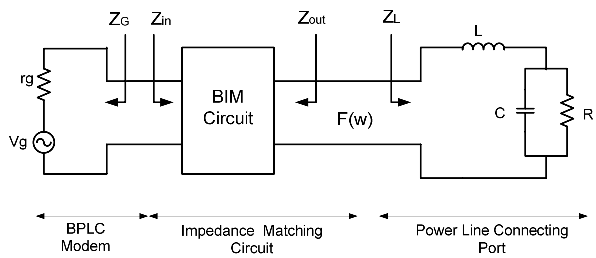


Fig. 2 Schematic of Impedance Matching

In this paper, we define Z_G the impedance of the source and Z_L the impedance of the load. Z_G is a pure resistive load whereas Z_L is a complex one including resistive, inductive and capacitive components. The total active power delivered by the source can be completely transmitted to the load if and only if Equation (1) is satisfied where ()* is for the complex conjugate.

$$Z_G = Z_L^* \tag{1}$$

Equation (1) shows definitively that if there is an impedance mismatch at the emission port, it means that the total active power P_L delivered by the PLC Coupler will be partly transmitted to the Modem P_t and partly reflected P_r, we have the power Equation (2).

$$P_g = P_t + P_r \tag{2}$$

We can get Z_G as normally a confirmed value given by the BPLC modem designer; Z_L can be achieved using network analyzer measure complex impedance in the [0.1~30MHz] band, though much more complicated.

Evaluating the transmitted power P_t is a crucial issue and in any case we cannot assume that the reflected power P_r is neglectable. The equalizer is necessary to minimize P_r and to maximize P_t, and perfect impedance matching will be reached if a total cancellation of P_r is achieved. In this paper, the goal of the equalizer since the design of this system has to be done in order to maximize P_t. A passive equalizer is built using passive components only like inductors and capacitors. In this paper, we focus on passive equalizer only.

It is convenient to use the gain function for the evaluation of the performance. The gain function is shown in Equation (3).

$$F\left(\omega^2\right) = 1 - |\rho|^2 \tag{3}$$

where $\rho = \dfrac{Z_G(j\omega) - Z_{in}(j\omega)}{Z_G(j\omega) + Z_{in}(j\omega)}$

The performances of the equalizer can therefore be evaluated using the gain function. Based on Equation (3), we can see that the second part of $F(\omega^2)$ is the square of the magnitude of the reflection coefficient calculated at the emission port. The values taken by $F(\omega^2)$ are between 0 and 1 thus corresponding to a very poor equalizer and a powerful one, respectively. Basically, the main goal of the equalizer is to maximize the transmitted power (or to minimize the reflected power) at the emission port. Considering $F(\omega^2)$ =1 in a chosen frequency band is equivalent to a total cancellation of the reflection located at the emission port. On the other hand, $F(\omega^2)$ =0 means that the designed equalizer is totally usefulness since there is a complete reflection at the emission port.

To properly design an equalizer, two technical constraints have to be satisfied. Let us define [F_1>0, F_2] the frequency band suitable for the wideband impedance matching. Achieving wideband impedance matching in the [F_1, F_2] band is possible if and only if $F(\omega^2)$ is maximized within the [F_1, F_2] band and minimize outside from this frequency band. Note that for the majority of BPLC systems, F_1 and F_2 can be around 0.1MHz and 30MHz. Knowing the characteristics of the impedance of the load and the source, the impedance matching algorithm has to optimize the gain function to satisfy the two previous constraints. Different shapes can be chosen for the gain functions. We choose Butterworth and Butterworth gain functions. We only focus in the following on Butterworth gain functions. We use Butterworth gain function in Equation (4).

$$F\left(\omega^2\right) = \frac{K}{1 + (\omega/\omega_c)^{2n}} \tag{4}$$

with maximum attainable DC gain K, where ω_c is the 3-dB bandwidth or the radian cutoff frequency.

Now we propose some algorithms to design the impedance matching circuit with references shown on the

PLC Coupler in order to calculate the components of the matching circuit [3-5].

We define some basic quantities used in the algorithms. r_g is the resistance of the BPLC modem and R is the resistance of PLC Coupler.

$$x = RC\omega_c \quad (5)$$

$$\gamma_m = m\pi/2n \qquad m = 1, 2, \cdots, \left[\frac{1}{2}(n-1)\right], n > 1 \quad (6)$$

$$r_g = R\frac{1-\delta^n}{1+\delta^n} \quad \Rightarrow \delta \quad (7)$$

when $x \ge 2\sin\gamma_1$, (8)

$$L_{\alpha 1} = \frac{xR\sin\gamma_3}{\sin\gamma_1\left[(x-\sin\gamma_1)^2 + \cos^2\gamma_1\omega_c\right]}$$

when $x < 2\sin\gamma_1$, (9)

$$L_{\alpha 2} = \frac{8R\sin^2\gamma_1\sin\gamma_3}{\left[(x-\sin\gamma_3)^2 + (1+4\sin^2\gamma_1)\sin\gamma_1\sin\gamma_3\right]\omega_c}$$

$$L_{\alpha 1}\left(\text{or } L_{\alpha 2}\right) = L_1 \quad (10)$$

$$C_{2m}L_{2m-1} = \frac{4\sin\gamma_{4m-1}\sin\gamma_{4m+1}}{\omega_c^2\left(1-2\delta\cos\gamma_{4m}+\delta^2\right)} \quad m \le \frac{1}{2}(n-1) \quad (11)$$

$$C_{2m}L_{2m+1} = \frac{4\sin\gamma_{4m-1}\sin\gamma_{4m+3}}{\omega_c^2\left(1-2\delta\cos\gamma_{4m+2}+\delta^2\right)} \quad m < \frac{1}{2}(n-1) \quad (12)$$

III. DESIGN OF IMPEDANCE MATCHING CIRCUIT

In this section, we design a BIM circuit for PLC Coupler using previous Butterworth gain functions. In Fig. 3, S11 characteristics of the unmatched Coupler developed PLC Coupler is represented on the Smith chart using the vector network analyzer in 0.1MHz to 30MHz frequencies, and impedance characteristics are represented in Fig. 5.

We propose to design a broadband equalizer for a cutoff frequency of 30MHz since many PLC modems use some carriers between 1MHz and 30MHz. We can take a load equivalent circuit from the tested results of Fig. 4 and 5 as series inductance is 637.8nH, shunt resistance 76.29 ohm, shunt capacitance 100pF and source impedance is 50 ohm as shown in Fig. 5.

Fig. 3 Test results of S-parameter (S11) of unmatched Coupler

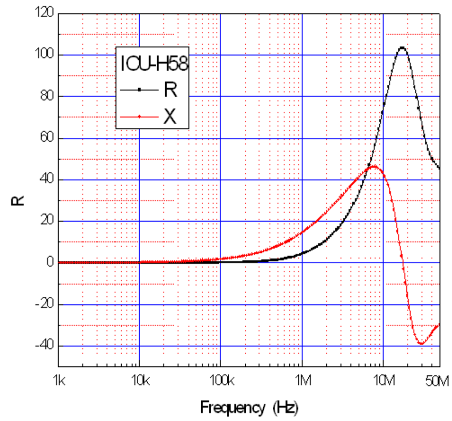
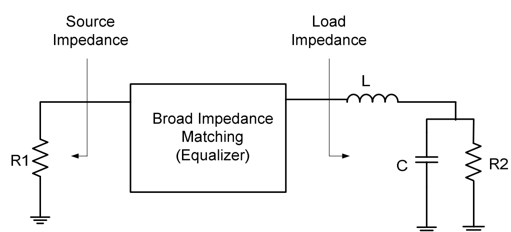


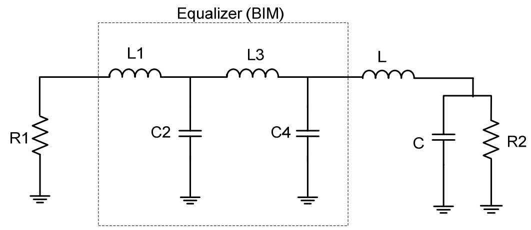
Fig. 4 Impedance(R+jX) of unmatched PLC Coupler

We choose the L-C low pass filter type as structure of equalizer, and applying to Weinberg relations of Equation (11) and (12), the elements values of equalizer are selected as L_1=61.424nH, C_2=27.187pF, L_3=381.16nH, and C_4=120.36nH. The Fig. 6 is the simulation result for S21 of equalizer using the Advanced Design System (ADS) of Agilent [6]. The simulation results show that the characteristic of filter with impedance matching circuit has more broadband comparing with without, and its cutoff frequency is about 30MHz.

We developed PLC Coupler including the broadband impedance matching circuit as following Fig. 7. PLC Coupler contains three main parts: noise filter, magnetic core and impedance matching circuit.



(a)



(b)

Fig. 5 (a) equivalent circuit (b) the circuit of Equalizer (BIM)

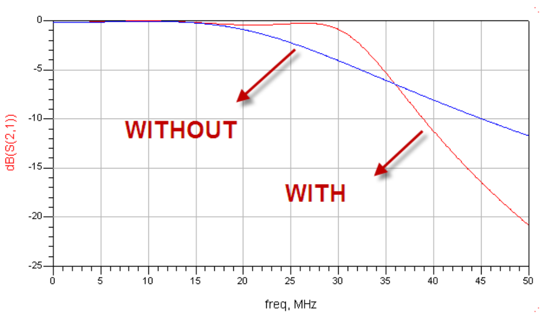
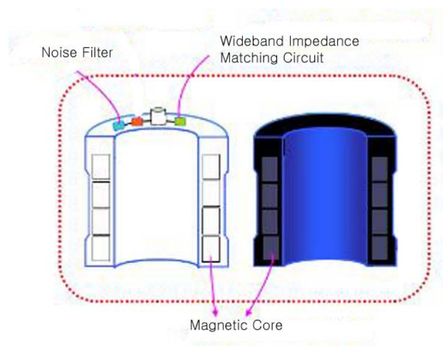


Fig. 6 S21 characteristics of the circuit with and without Equalizer (BIM)



(a) Configuration

(b) photo of developed coupler

Fig. 7 PLC Coupler with broadband impedance matching circuit

IV. RESULTS AND CONCLUSIONS

We tested to get the characteristics of broadband matching circuit of PLC Coupler using the vector network analyzer. Fig. 8 is shown S11 characteristic of developed Coupler with broadband impedance matching circuit comparing with characteristic of unmatched Coupler, and Fig. 9 is result for Smith chart of S11 characteristic for it. Fig. 10 is shown the comparing results for S21 characteristic with and without impedance matching circuit in PLC Coupler.

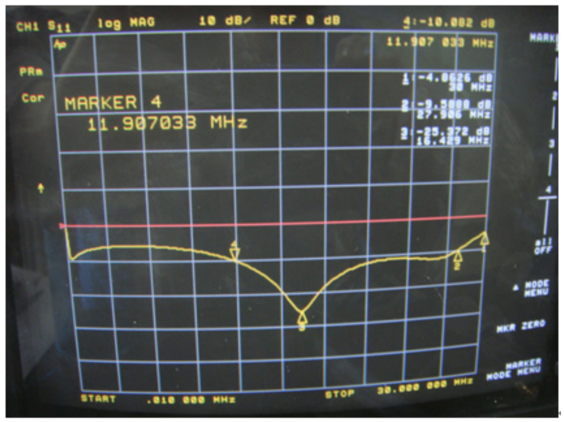


Fig. 8 S11 Characteristic of developed Coupler

Fig. 9 Smith chart for S11

In the broadband power line communication system, a lossless impedance matching circuit is a basic problem. The design of wideband impedance matching need more practice besides the theory.

In this paper, we have presented a general design for a wideband impedance matching in power line communication. We use the theory to analyze the coupling circuit we want to get. Then we make the circuit in practical. It is important to modify in practical conditions.

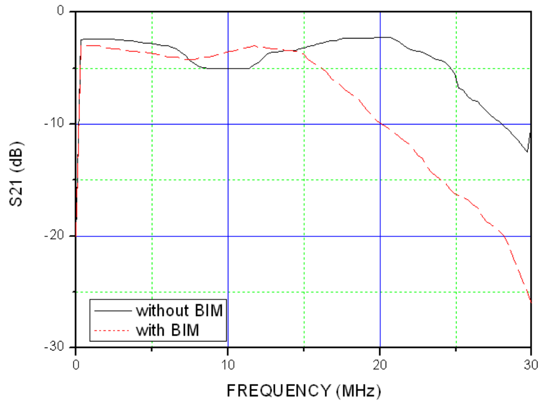


Fig. 10 S21 Characteristic of developed Coupler

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