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Reduction of Input Current Harmonics for Three Phase PWM Converter Systems under a Distorted Utility Voltage

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Abstract

This paper proposes a harmonics reduction technique for the input currents of three phase PWM converters. The quality of the phase angle information on the utility voltage connected to the PWM converters affects their control performance. Under a distorted utility voltage, the extracted phase angle based on the synchronous reference frame PLL method is distorted. This causes large harmonics in the input currents of a PWM converter. In this paper, a harmonics reduction method that makes the input currents in the PWM converter sinusoidal even under distorted utility conditions is proposed. By the proposed method, without additional hardware, the THD (Total Harmonic Distortion) of the input currents can be readily limited to below 5% which is the harmonic current requirements of IEEE std. 519. Its validity is verified by simulations and experimental results.

Key Words: Distorted utility voltage, Harmonics reduction method, PLL, PWM converter

I. INTRODUCTION

Phase angle information on utility voltage is essential to the operation of ac to dc conversion systems that are coupled with utility lines such as PWM converters and active power filters. This information has to be accurate because the control performance of the conversion systems such as power factor correction, active or reactive power control, and harmonic current compensation are highly dependent on its quality. The angle information is typically obtained by one of the forms of a phase locked loop (PLL)[1]. Among the different forms, the synchronous d, q reference frame PLL system is used the most because it is simple and works well under an ideal utility condition.

Recently, a growing part of the load is fed through power electronic equipment drawing a non-sinusoidal current. This results in undesirable harmonics in the utility voltage, whereby the voltage becomes a non-sinusoidal waveform containing distortions. Under such distorted utility conditions, the extracted phase angle based on the synchronous reference frame PLL also contains harmonics. This distorted phase angle causes harmonics in the current references for the control of a PWM converter. As a result, the real input currents in the PWM converter will become non-sinusoidal waveforms containing harmonics.

A few PLL systems that take into consideration distorted utility voltage conditions have been studied. These studies focused mainly on obtaining non-distorted phase angles. In order to do this, a low-pass filter (LPF) was used in a synchronous reference frame PLL system[1],[2]. Therefore, these methods have a disadvantage in that the bandwidth of their control system is limited to the cut-off frequency of the LPF.

When operating PWM converters under distorted utility voltage conditions, the fundamental problem is the distortion of the real input currents as a result of this distortion rather than the phase angle itself. Therefore, this paper proposes a harmonics reduction method which makes the input currents in a PWM converter almost sinusoidal even under a distorted utility voltage. The proposed method extracts the distorted component from the detected phase angle by a synchronous reference frame PLL system under a distorted utility voltage, and then corrects the d- and q- axis current references to obtain sinusoidal real input currents. Through simulations and experiments, it has been confirmed that the proposed method can readily limit the THD of input currents to below 5%, which is the harmonic current requirement of IEEE Std. 519, even under a source voltage with 12.6% THD.

II. SYNCHRONOUS REFERENCE FRAME PLL METHOD

The synchronous d, q reference frame PLL system works in a rotating frame of reference synchronized to the utility

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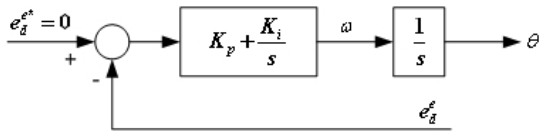
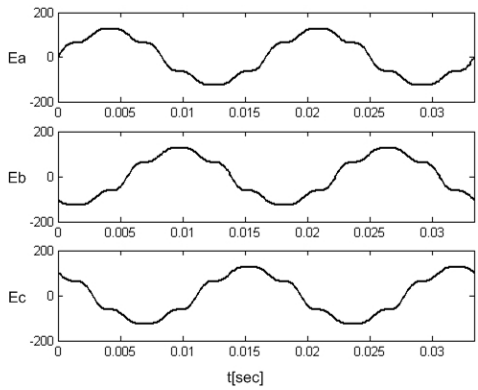
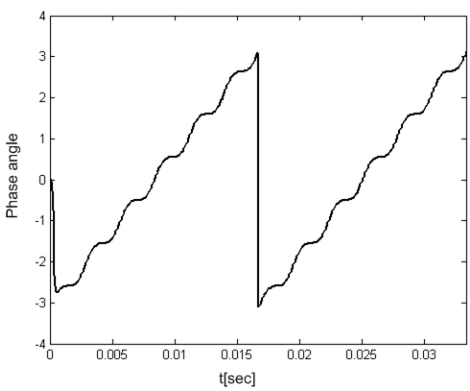


Fig. 1. Control diagram of synchronous reference frame PLL system.



(a) Distorted utility voltages.



(b) Phase angle.

Fig. 2. Phase angle in case of distorted utility voltage.

voltage frequency to detect the phase angle. In the synchronous reference frame, the d and q axis voltages appear as a dc quantity. Thus, the phase angle can be easily obtained by regulating the d-axis voltage e_d^e to zero using a PI regulator as shown in Fig. 1.

If the utility voltage has harmonics, the phase angle which is the output of the synchronous reference frame PLL will include similar harmonics. Fig. 2 shows that the utility voltage distortion produces a distortion on the phase angle extracted by the synchronous reference frame PLL system.

Such a distortion of the phase angle may deteriorate the control performance for systems. The distortion components in the phase angle bring about undesirable harmonics in the d and q axis current references for a PWM converter. As a result, the real input currents will not be sinusoidal. These distorted components can be eliminated by using a LPF with a low cutoff-frequency on the voltages[2]. However, using a LPF reduces the bandwidth to make the dynamic response of the PLL system sluggish.

To review the impact of the distorted phase angle θ' on the waveforms of the input currents, the d and q axis current

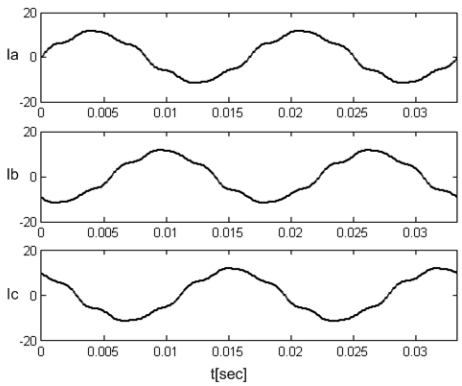


Fig. 3. Input currents in case of using the distorted phase angle.

references i_d^{e*}, i_q^{e*} in the synchronous frame are transformed into the current references i_d^{s*}, i_q^{s*} in the stationary frame as following

$$\begin{bmatrix} i_d^{s*} \\ i_q^{s*} \end{bmatrix} = \begin{bmatrix} \cos\theta' & -\sin\theta' \\ \sin\theta' & \cos\theta' \end{bmatrix} \begin{bmatrix} i_d^{e*} \\ i_q^{e*} \end{bmatrix} = \begin{bmatrix} \cos(\theta+\Delta\theta) & -\sin(\theta+\Delta\theta) \\ \sin(\theta+\Delta\theta) & \cos(\theta+\Delta\theta) \end{bmatrix} \begin{bmatrix} i_d^{e*} \\ i_q^{e*} \end{bmatrix} \quad (1)$$

where, $\Delta\theta$ is the error between the undistorted utility angle θ and the PLL output $\theta'(=\theta+\Delta\theta)$.

When a synchronous frame current regulator is used, the reference currents i_d^{e*}, i_q^{e*} are given as dc currents in the steady state. If these current references i_d^{e*}, i_q^{e*} are transformed into the references i_d^{s*}, i_q^{s*} in the stationary frame using the undistorted phase angle under ideal utility conditions, they will become pure sine waves without any distortion. In contrast, if i_d^{e*}, i_q^{e*} are transformed using a distorted phase angle, they will not become sinusoidal but will contain distortions. Therefore, the input currents will inevitably be distorted as shown in Fig. 3.

III. HARMONICS REDUCTION TECHNIQUE OF INPUT CURRENTS

To avoid distortion of the stationary frame current references due to a distorted phase angle, this paper proposes a current references correction method. In the proposed method, the current references in the synchronous frame are corrected so that the currents in the stationary frame can be sinusoidal even if they are transformed by a distorted phase angle.

If the phase angle is not distorted, the stationary reference frame current references i_d^{s*}, i_q^{s*} become sinusoidal and are given by:

$$\begin{bmatrix} i_d^{s*} \\ i_q^{s*} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_d^{e*} \\ i_q^{e*} \end{bmatrix}. \quad (2)$$

However, in the case of a distorted phase angle, these references may include distortion components as shown in (1).

The new corrected synchronous current references i_d^{e**}, i_q^{e**} can be found by solving (3) so that the stationary currents become sinusoidal currents as in (2) even if they are transformed by a distorted phase angle.

$$\begin{bmatrix} i_d^{s*} \\ i_q^{s*} \end{bmatrix} = \begin{bmatrix} \cos(\theta+\Delta\theta) & -\sin(\theta+\Delta\theta) \\ \sin(\theta+\Delta\theta) & \cos(\theta+\Delta\theta) \end{bmatrix} \begin{bmatrix} i_d^{e**} \\ i_q^{e**} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_d^{e*} \\ i_q^{e*} \end{bmatrix}. \quad (3)$$

By using the original current references i_d^{e*}, i_q^{e*} and the distortion components of the phase angle, the corrected current references i_d^{e**}, i_q^{e**} can be obtained by (4).

$$\begin{bmatrix} i_d^{e**} \\ i_q^{e**} \end{bmatrix} = \begin{bmatrix} \cos(\theta+\Delta\theta) & -\sin(\theta+\Delta\theta) \\ \sin(\theta+\Delta\theta) & \cos(\theta+\Delta\theta) \end{bmatrix}^{-1} \begin{bmatrix} i_d^{s*} \\ i_q^{s*} \end{bmatrix} = \begin{bmatrix} \cos(\theta+\Delta\theta) & \sin(\theta+\Delta\theta) \\ -\sin(\theta+\Delta\theta) & \cos(\theta+\Delta\theta) \end{bmatrix} \begin{bmatrix} i_d^{s*} \\ i_q^{s*} \end{bmatrix} = \begin{bmatrix} \cos(\theta+\Delta\theta) & \sin(\theta+\Delta\theta) \\ -\sin(\theta+\Delta\theta) & \cos(\theta+\Delta\theta) \end{bmatrix} \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_d^{e*} \\ i_q^{e*} \end{bmatrix} = \begin{bmatrix} \cos\Delta\theta & \sin\Delta\theta \\ -\sin\Delta\theta & \cos\Delta\theta \end{bmatrix} \begin{bmatrix} i_d^{e*} \\ i_q^{e*} \end{bmatrix}. \quad (4)$$

The distortion components $\sin\Delta\theta$ and $\cos\Delta\theta$ necessary for calculating (4) can be obtained by (5).

$$[R(\theta)] \begin{bmatrix} \cos(\theta+\Delta\theta) \\ \sin(\theta+\Delta\theta) \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \cos(\theta+\Delta\theta) \\ \sin(\theta+\Delta\theta) \end{bmatrix} = \begin{bmatrix} \cos\theta\cos(\theta+\Delta\theta)+\sin\theta\sin(\theta+\Delta\theta) \\ -\sin\theta\cos(\theta+\Delta\theta)+\cos\theta\sin(\theta+\Delta\theta) \end{bmatrix} = \begin{bmatrix} \cos\Delta\theta \\ \sin\Delta\theta \end{bmatrix}. \quad (5)$$

To extract such distortion components, the phase angles θ and $\theta+\Delta\theta$ should be known. In order to get these, two synchronous reference frame PLL systems are used in the proposed method. One is for the phase angle $\theta+\Delta\theta$ with distortion components and the other is for the phase angle without distortion components. When obtaining the phase angle θ, a LPF with a low cut-off frequency is used in the synchronous reference frame PLL system. However, in the proposed system, this phase angle θ is not used to control the system due to its low bandwidth, but to obtain the distortion components $\sin\Delta\theta$ and $\cos\Delta\theta$. The simulation results in Fig. 4 and 5 show that even if an undistorted utility angle can be obtained using a LPF with a low cut-off frequency like 5 Hz, the dynamic response becomes sluggish. Therefore, the phase angle θ is not used for system control, but exclusively for extracting the distortion components. It is the phase angle $\theta+\Delta\theta$ that is used to control the system.

Fig. 6 shows a block diagram of the proposed current correction method. The whole system consists of a current corrector and two PLL systems to detect the phase angles $\theta+\Delta\theta$ and θ. Details for the current corrector are shown in Fig 7.

Fig. 8 shows the current references before and after the correction. The output currents of a synchronous frame current regulator, i_d^{e*} and i_q^{e*} are naturally pure DC values as shown in Fig. 8(a). However, after the correction for obtaining the sinusoidal real input currents, the references become DC currents containing ripple components as shown in Fig. 8(b).

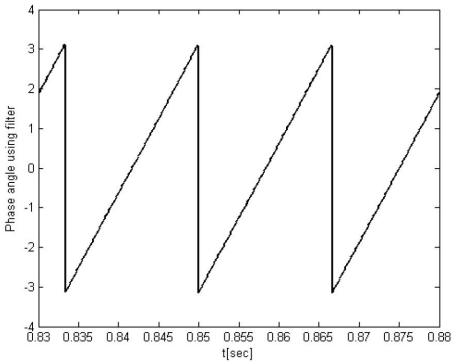


Fig. 4. Phase angle of Synchronous frame PLL using LPF.

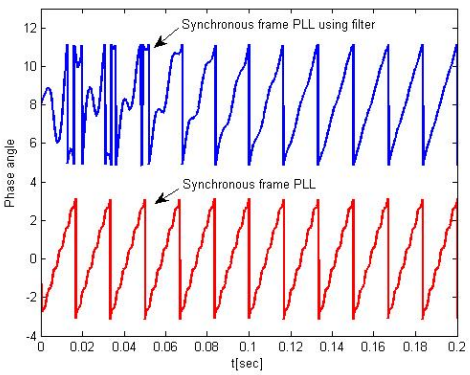


Fig. 5. Dynamic response characteristics of two PLLs.

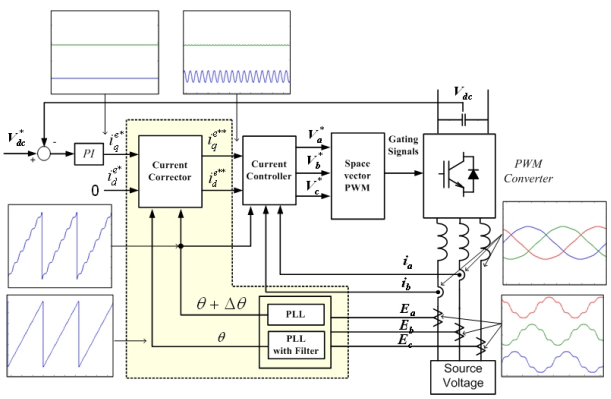


Fig. 6. Block diagram of proposed method.

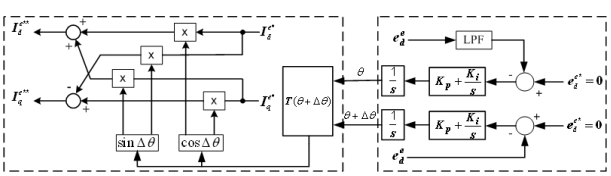
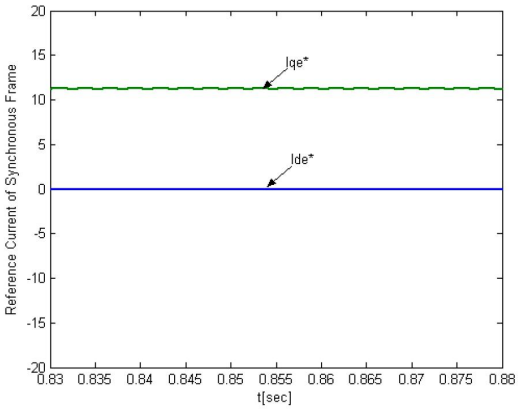


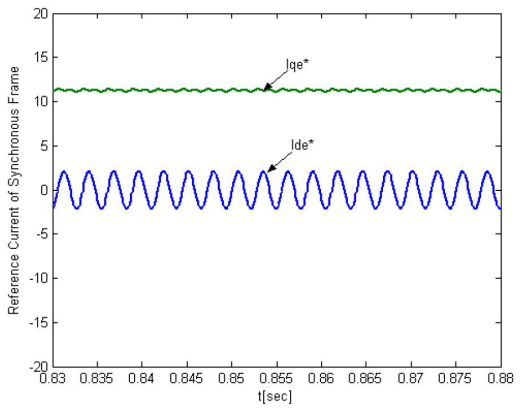
Fig. 7. Detail diagram of current corrector.

IV. SIMULATION RESULTS

To show the usefulness of the proposed method which eliminates the distortion of input currents, simulations were executed for a 3kW PWM converter system. Utility ac voltage of 120V (phase, rms) has 10% and 7% of 5th and 7th harmonics respectively, resulting in a 12.6% THD. The interface



(a) Before correction.



(b) After correction.

Fig. 8. Current references in the synchronous frame.

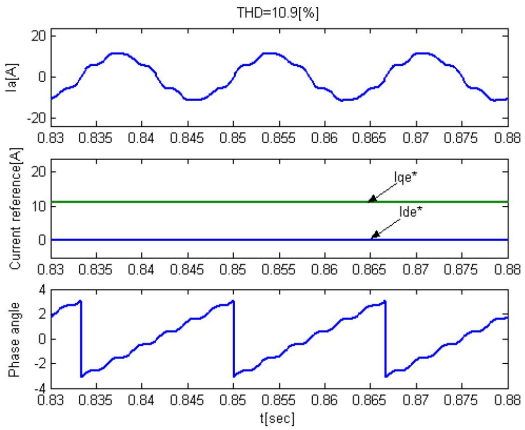
inductance at the input terminal is 0.8 mH and the DC link capacitor is 2700 uF. The DC link voltage is regulated at 250V with a load resistance of 30Ω.

Simulations were performed with three methods of synchronous reference frame PLL: the synchronous reference frame PLL method, the synchronous reference frame PLL method using a LPF with a 5 Hz cut-off frequency and the proposed method.

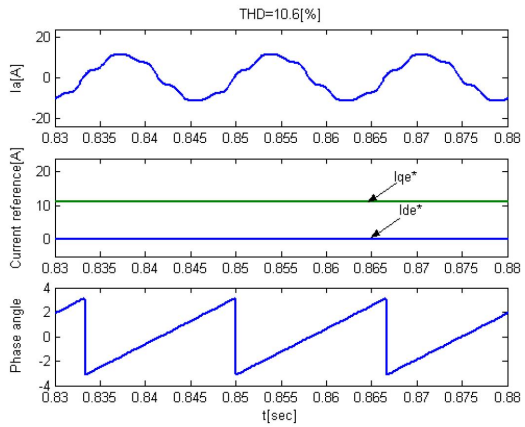
The simulation results in Fig. 9 show a-phase voltage and input current in the PWM converter.

When using the synchronous reference frame PLL method shown in Fig. 9(a), the harmonic components and the THD of the input current are almost the same as those of utility voltage. In this case, the THD of the current is 10.9%. In the case of the synchronous reference frame PLL method with a LPF shown in Fig. 9(b), the current has a 10.6% THD. Although the distortion of the phase angle can be eliminated by using a LPF, it can be seen that the THD is not improved. From the simulation results in Fig. 9(a) and 9(b), it can be concluded that in the two cases above, the harmonics of the input current can be directly influenced by the distortion of the utility voltage.

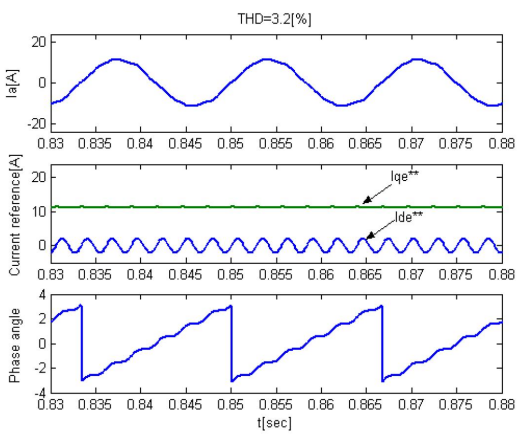
In the case of a synchronous reference frame PLL with the proposed correction method, even though the phase angle is distorted, the THD of the currents is reduced to 3.2% as shown in Fig. 9(c).



(a) Synchronous frame PLL.



(b) Synchronous frame PLL using LPF.



(c) Proposed method.

Fig. 9. A-phase voltage and input current in PWM rectifier.

V. EXPERIMENT RESULTS

To verify the validity of the proposed method, experiments were executed on a PWM IGBT converter system with a digital controller based on a TMS320VC33 DSP as shown in Fig. 10. The switching frequency is 10kHz and the control time interval of the PLL system is 50us. The experiments for the conventional and proposed methods were performed under the same conditions as the simulations. However, the input inductance was changed from 0.5 to 3.12mH in order to investigate its effect on the current THD.

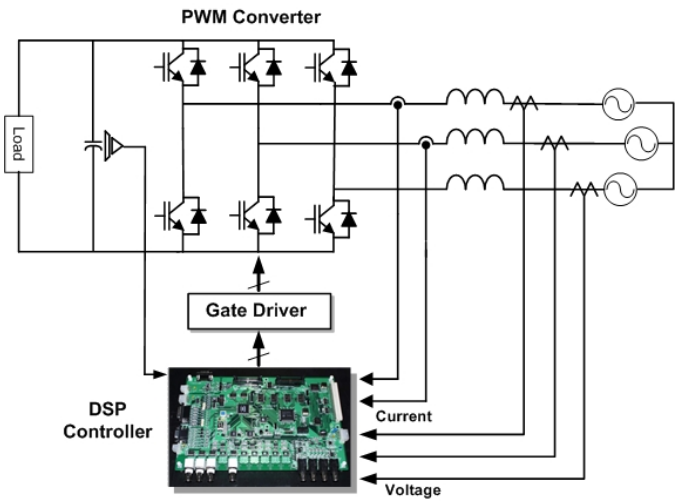


Fig. 10. Configuration of experimental sets.

Fig. 11 shows the phase voltage, the phase current and the THD for the three methods in the case of using a 0.8mH input inductance. It is confirmed that experiment results similar to the simulation results can be obtained.

Fig. 12 shows a comparison of the phase current THD using the three methods for several input inductances. It is natural that the more the input inductance increases, the more the THD reduces. In the case of the synchronous reference frame PLL method with a LPF, it can be seen that the interface inductance has a larger impact on the current THD than the other methods. It is clear that the proposed method needs a smaller inductance than the other methods to meet the THD requirements of the current: below 5% according to IEEE Std. 519. If the synchronous reference frame PLL method with a LPF has a large inductance, such as 3.12mH, a lower current THD can be achieved than with the proposed method. However, slow dynamics in this PLL system are inevitable due to the LPF with a low bandwidth.

VI. CONCLUSIONS

This paper proposed a new current harmonic reduction method which enables the input currents in PWM converters to be almost sinusoidal even under distorted utility conditions.

The proposed method, based on a synchronous reference frame PLL, does not deteriorate the system dynamics as the PLL method with a LPF does. Through simulations and experiments, it was verified that under a utility ac voltage with a 12.6% THD, the THD of the input currents of the proposed method can be readily limited below the 5% harmonic current requirements of IEEE std. 519. The proposed method is useful in ac to dc conversion systems connected to an ac utility line, such as a PWM converter and an active power filter, because the proposed algorithm can be simply implemented by software and requires a smaller interface inductance than the other PLL methods to achieve the same harmonic requirements.

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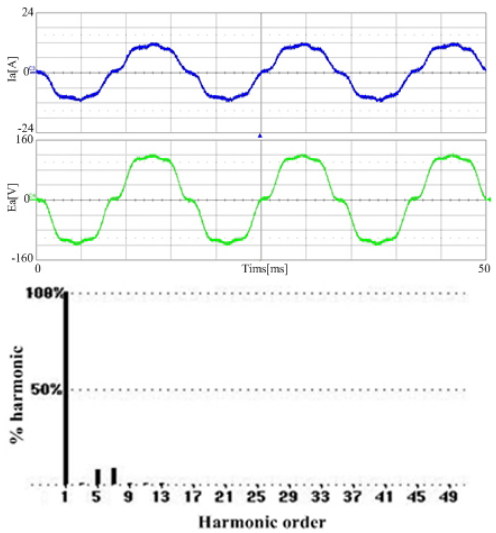
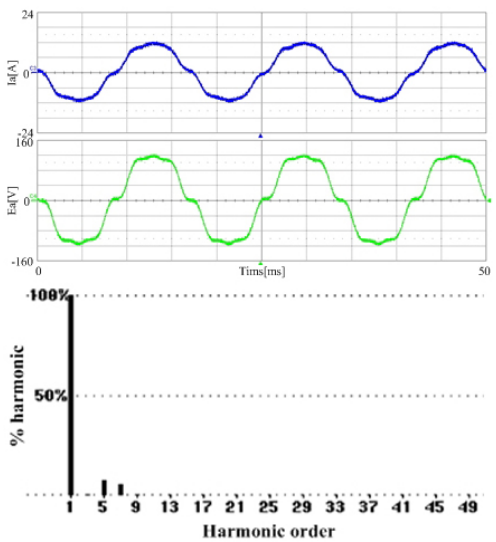
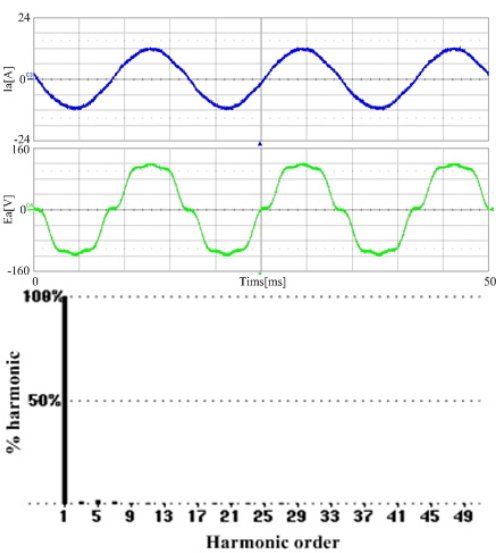


(a) Synchronous frame PLL (THD=11.8[%]).



(b) Synchronous frame PLL using LPF (THD=9.5[%]).



(c) Proposed method (THD=3.4[%]).

Fig. 11. A-phase voltage and current at input inductance 0.8mH.

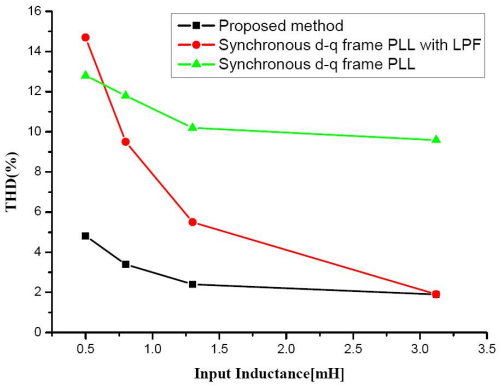


Fig. 12. Phase current THD as a function of a input inductance.

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