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Digital Control Strategy for Input-Series-Output-Parallel Modular DC/DC Converters

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Abstract

Input-series-output-parallel (ISOP) converters consisting of multiple modular DC/DC converters can enable low voltage rating switches to be used under high voltage input applications. This paper presents a digital control strategy, which can achieve equal sharing of input voltage for a modular ISOP system consisting of two-transistor forward DC/DC converters by forcing the input voltages of neighboring modules to be equal. The proposed scheme is analyzed using small signals analysis based on the state space average method. The performance of the proposed control strategy is verified with an experimental prototype of an ISOP converter made up of three two-switch forward converters.

Key Words: Digital control, Forward DC/DC, Input-series and output-parallel, Modular DC/DC converters, Voltage sharing

I. INTRODUCTION

Multilevel converters enable low-voltage rating switches to be used under high voltage applications. However, system reliability cannot be guaranteed for a large quantity of diodes or flying capacitors [1]. The input-series output-parallel (ISOP) configuration consists of several modular DC-DC converters connected in series at the input and in parallel at the output. This enables the use of high switching frequency metal oxide semiconductor field effect transistors (MOSFETs) with low voltage ratings, which leads to high power density and high conversion efficiency. However, control must be taken to ensure equal input voltage sharing among all of the modules for the ISOP DC/DC converters. Several control schemes have been proposed to achieve this purpose. Common duty ratio control results in stable operation for ISOP converters [2], but equal input voltage sharing (IVS) can not be achieved for parameter mismatches such as a turns ratio mismatch of transformers. A charge control scheme with input-voltage feed forward has been implemented for a two-converter system [3]. However, the input currents have to been sensed as well as the input voltages. A master/slave control schemes can only be used in small applications due to electrical isolation problems [4]. A three-loop control scheme [5], [6] and a decoupling IVS control scheme [7] can achieve input voltage equally for an ISOP system. However, all of the voltage references for the IVS control loops must vary with the total input voltage, thus complicating the design. Although interleaving control can minimize the output current ripples, in order to achieve satisfactory control, the integrated circuits need to be synchronized [4], [5], which complicates the design further. Most ISOP connected modules under research are full-bridge or single-ended forward DC-DC converters [2]–[10]. It is well known that neither of these are well suited because full-bridge converters work at the risk of shoot-through failures for switching devices connected directly across the source. Additional demagnetizing or snubber circuits have to be designed for single-ended forward converters. However, two-transistor forward (TTF) DC/DC converters are well suited for use under high input voltage and high power applications due to their inherent advantages. These advantages include automatic voltage spike clamping and demagnetization through diodes connected to the switching devices. Dual TTF DC/DC converters with all of the windings sharing one transformer can be fed from input DC voltage, but each of them are coupled through a magnetizing field and as a result they can not been called truly modular converters from an architecture point of view [11]. Control implementation for ISOP DC/DC converters using analogy circuits is time consuming and inflexible [2]–[11]. With the emergence of digital signal processors (DSP), digital control is becoming a potentially attractive alternative to the analogy option due to its inherent advantages [12], [13].

This paper proposes a very simple digital IVS control for ISOP systems, which does not require changing the voltage references for each module. Perfect voltage sharing can be achieved by forcing the input voltage between the neighbor modules equally, no matter what the total input voltage is. The proposed ISOP configuration consists of two-switch forward DC-DC converters, which have the advantages of no risks

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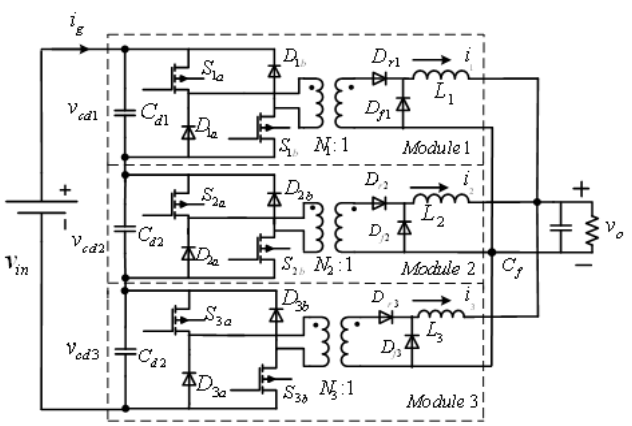

Fig. 1. ISOP connected modular two-switch forward converters.

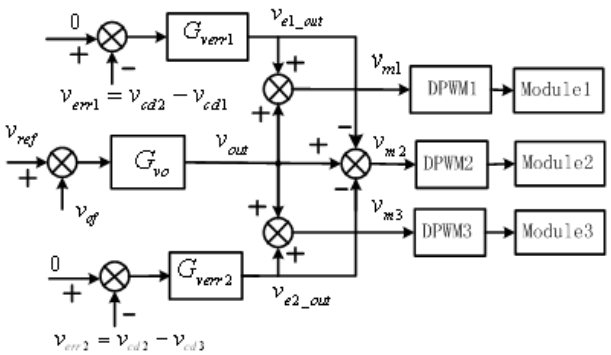

Fig. 2. Proposed control strategy.

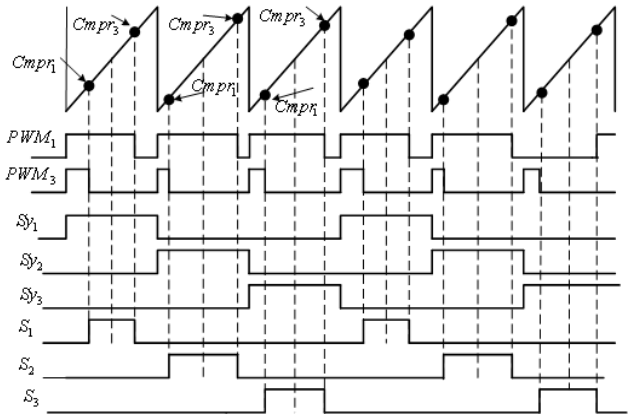

Fig. 3. Schematic of digital PWM generation.

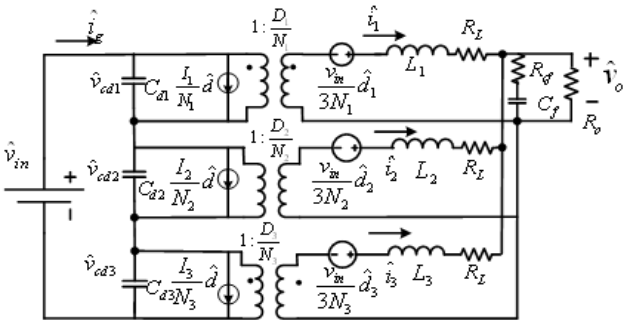

Fig. 4. Small-signal average model of the converter.

of shooting through, automatic voltage spike clamping and demagnetizing through diodes. Loop gain analysis is carried out on the proposed control strategy and a 100W prototype is fabricated and experimentally evaluated.

This paper is organized as follows. The proposed digital control strategy is presented and analyze in Section II. Small signal analysis and loop gain analysis are provided in Section III. Experimental results of the prototype are illustrated in Section IV. Conclusions are given in Section V.

II. Novel Input Voltage Sharing Control

A. Operation principles of the proposed control strategy

Fig. 1 shows the schematic of an ISOP converter made up of three TTF DC/DC converters. In this configuration, the total input voltage v_{in} is divided by the input capacitors C_{d1}, C_{d2} and C_{d3} thus we get the voltages v_{cd1}, v_{cd2} and v_{cd3} working as individual input voltages for each module respectively.

Equal sharing of the total input voltage v_{in} means that $v_{cd1} = v_{cd2} = v_{cd3}$ which can also be described by:

$$\begin{cases} v_{cd1} - v_{cd2} = 0 \\ v_{cd2} - v_{cd3} = 0. \end{cases} \tag{1}$$

However, satisfying (1) is only one of our control objectives. Another is that the output voltage should stay unchanged during load and under input voltage variations. Hence, the control strategy consists of one common output voltage regulation (OVR) loop and two IVS regulation loops. Fig. 2 shows a control block which can achieve equal sharing of the input voltage and a constant voltage output, where v_{ref} is the reference voltage for the voltage output; v_{of} is the feedback of the output voltage; G_{vo} is the compensation network of the output voltage control. To satisfy (1), both of the differences between the input voltages of neighboring modules must be equal to zero. This is why the references are zero for both of the input voltage sharing control loops. Input voltage differences are amplified by the compensation networks G_{verr1} and G_{verr2}. Then we can get c and v_{e2_out}, which work as offset voltages during duty ratio generation. v_{out} works as the output of OVR. Through linear combinations of OVR and IVS outputs, the values determining the duty ratios of individual modules can be derived as shown in (2).

$$\begin{cases} v_{m1} = v_{out} + v_{e1\_out} \\ v_{m2} = v_{out} - v_{m1} - v_{m3} \\ v_{m3} = v_{out} + v_{e2\_out}. \end{cases} \tag{2}$$

The balancing mechanism can be seen in Fig. 2 and can be explained as follows, if v_{cd2} is equal to v_{cd3} and both of them are higher than v_{cd1}, then v_{err1} is positive and the calculation of G_{verr1} causes v_{e1_out} to decrease. This results in a decrease in the duty ratio for module 1 and an increase in the duty ratio for module 2. Because v_{err2} is equal to zero in such case, v_{e2_out} remains unchanged. Therefore, capacitor C_{d1} is charged while capacitor C_{d2} is discharged, leading to an increase in v_{cd1} and a decrease in v_{cd2}. On the other hand, when v_{cd2} is equal to v_{cd1} and both of them are higher than v_{cd3}, through the calculation with the proposed control

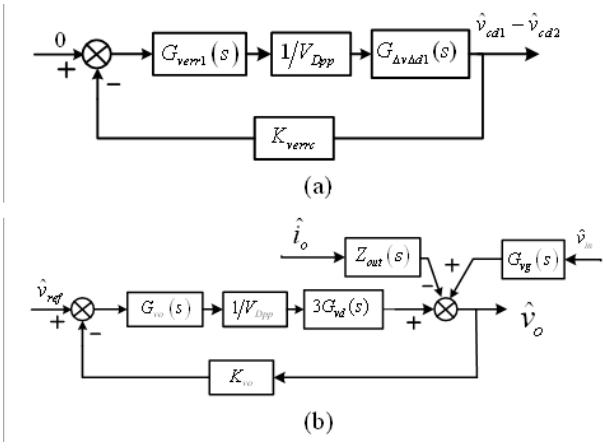

Fig. 5. System block diagram of ISOP converter (a) IVS control block diagram; (b) OVR control block diagram.

strategy, v_{cd3} will increase while v_{cd2} decreases. In this way, all of the individual input voltages become equal and power sharing balance among all of the modular DC/DC converters is accomplished.

B. Digital implementation of the control strategy

Note that the implementation of the proposed control strategy, shown in Fig. 2, is implemented by only one digital signal processor (DSP). Compensation networks including both OVR and IVS are based on digital proportion-integral types. The gate signals for the switches of each modular DC/DC converter are interleaved.

Fig. 3 shows the interleaved gate signal generation. Timer 1 is put in continuous mode and its period register is loaded with a value corresponding to the desired switching frequency and the number of modules. Because there are three modules, the frequency of Time 1 is three times that of the switching frequency for each module. Gate signals for every module are generated every three periods of Timer 1. Using module 1 as an example, the value of the compare register is constantly compared with the value of the time counter. When the values match, a transition from high to low takes place on the associated outputs form *PWM*1 and *PWM*3. The compared values can be seen from (3):

$$\begin{cases} Cmpr_1 = T_{P1}/2 - v_{m1}/2 \\ Cmpr_3 = T_{P1}/2 + v_{m1}/2 \end{cases} \tag{3}$$

where *Tp1* is the value of the period register. For module 2 and module 3, the signals *PWM1* and *PWM3* are generated in the same way except that v_{m2} and v_{m3} supersede v_{m1} respectively. Each period of Time 1 is marked subsequently by the synchronous signals Sy_1, Sy_2 and Sy_3 respectively. The logic expression of the gate signals for all of the switches in the ISOP configuration is shown in (4):

$$\begin{cases} S_1 = (PWM_1 \oplus PWM_3) \cdot Sy_1 \\ S_2 = (PWM_1 \oplus PWM_3) \cdot Sy_2 \\ S_3 = (PWM_1 \oplus PWM_3) \cdot Sy_3 \end{cases} \tag{4}$$

where S_1, S_2 and S_3 are the gate signals for the switches of module 1, module 2 and module 3 respectively.

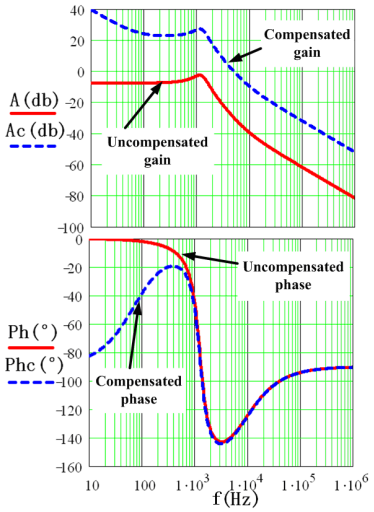

Fig. 6. Output voltage regulation (OVR) loop gains.

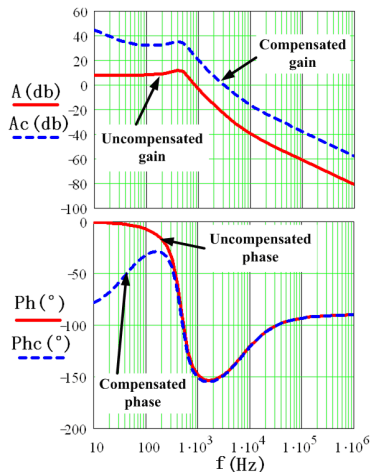

Fig. 7. Input voltage sharing (IVS) control loop gains.

III. Small Signal Analysis and Regular Loop Gain Design

A. Small signal modeling of the ISOP system

Based on a small signal model of isolated buck DC-DC converters, we can derive the small signal model of a ISOP connected three-converter system, as shown in Fig. 4, where $\hat{d}$ is the perturbation of the duty ratio, while $\hat{v}_{cdi}$ (*i*=1,2,3) and $\hat{i}_i$ (*i*=1,2,3) represent perturbations of the individual input voltages and output currents. Equivalent series resistors of the output inductors and output capacitors are denoted as R_L and R_{cf} respectively. For simplicity of the analysis, the three converters are assumed to have the same turns ratio *N* and same output inductance L, which can be revealed from (5):

$$\begin{cases} N_1 : 1 = N_2 : 1 = N_3 : 1 = N : 1 \\ L_1 = L_2 = L_3 = L \end{cases}. \tag{5}$$

Under the steady state, the three converters share the input voltage and load current equally. This can be seen as follows:

$$V_o = V_{cd1}\frac{D_1}{n} = V_{cd2}\frac{D_2}{n} = V_{cd3}\frac{D_3}{n}. \tag{6}$$

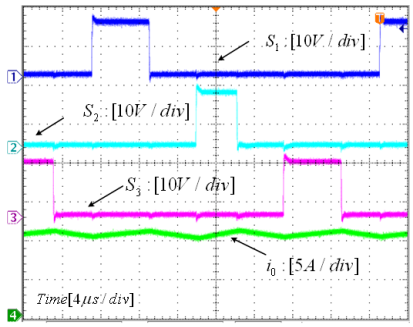

Fig. 8. Gate signals for each module switches.

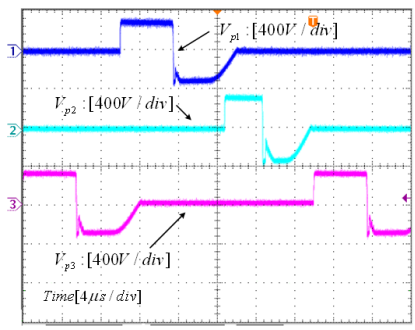

Fig. 9. Primary voltages over individual transformers.

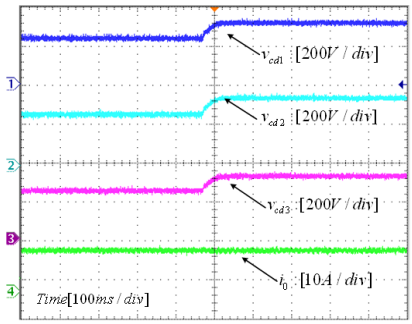

Fig. 10. Response to a step change of the input voltage V_{in}.

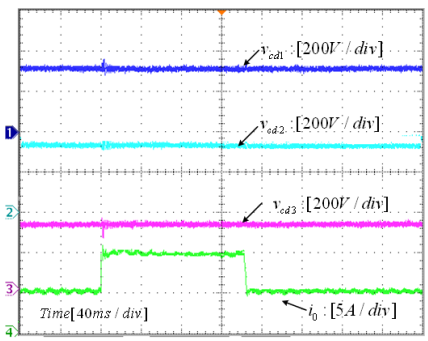

Fig. 11. Response to a step change of the load.

Because we assume the duty ratios of all the modules are the same:

$$D_1 = D_2 = D_3 = D. \tag{7}$$

Thus, we can get:

$$\begin{cases} I_1 = I_2 = I_3 = \dfrac{I_0}{3} = \dfrac{V_0}{3R_0} \\ V_{cd1} = V_{cd2} = V_{cd3} = \dfrac{V_{in}}{3} \end{cases} \tag{8}$$

where I_1, I_2 and I_3 are the individual steady-state output currents, R_0 is the rated load and V_{in} is the value of the total input voltage at the steady state. I_0 and V_0 are the load current and output voltage under the steady states. According to Fig. 4 and (5), the small model equations can be expressed as:

$$\begin{cases} \dfrac{D_1}{N}\hat{v}_{cd1} + \dfrac{v_{in}}{3N}\hat{d}_1 = (sL + R_L)\cdot\hat{i}_1 + \hat{v}_o \\ \dfrac{D_2}{N}\hat{v}_{cd2} + \dfrac{v_{in}}{3N}\hat{d}_2 = (sL + R_L)\cdot\hat{i}_2 + \hat{v}_o \\ \dfrac{D_3}{n}\hat{v}_{cd3} + \dfrac{v_{in}}{3N}\hat{d}_3 = (sL + R_L)\cdot\hat{i}_3 + \hat{v}_o \end{cases} \tag{9}$$

$$\begin{cases} \hat{i}_g - \hat{v}_{cd1}\cdot sC_d - \dfrac{i_1}{N}\hat{d}_1 = \dfrac{D_1}{N}\cdot\hat{i}_1 \\ \hat{i}_g - \hat{v}_{cd2}\cdot sC_d - \dfrac{i_2}{N}\hat{d}_2 = \dfrac{D_2}{N}\cdot\hat{i} \\ \hat{i}_g - \hat{v}_{cd3}\cdot sC_d - \dfrac{i_3}{N}\hat{d}_3 = \dfrac{D_3}{N}\cdot\hat{i} \end{cases} . \tag{10}$$

From Fig. 4 we can also get:

$$\begin{cases} \hat{v}_{in} = \hat{v}_{cd1} + \hat{v}_{cd2} + \hat{v}_{cd3} \\ \hat{i}_o = \hat{i}_1 + \hat{i}_2 + \hat{i}_3 = \hat{v}_o\left[R_o // \left(RC_f + \dfrac{1}{SC_f}\right)\right] \end{cases} . \tag{11}$$

Based on (9), (10) and (11), by setting $\hat{v}_{in}$=0 and $\hat{d}_k$=0, where $k \neq i$, the control-to-output transfer function of an arbitrary module i (i=1,2,3) can be written as:

$$\begin{aligned} G_{vdi} &= \left.\frac{\hat{v}_o}{\hat{d}_i}\right|_{\substack{\hat{v}_{in}=0 \\ \hat{d}k=0\ (k\neq i)}} \\ &= \frac{\dfrac{v_{in}}{3N}(sC_fR_o + 1)}{s^2LC_f\left(1+\dfrac{R_{cf}}{R_o}\right)+s\left[\dfrac{L}{R_o}+R_LC_f\left(1+\dfrac{R_{cf}}{R_o}\right)+3C_fR_{cf}\right]+\dfrac{R_L}{R_o}+3}. \end{aligned} \tag{12}$$

The control-to-module-input transfer function can be shown as follows:

$$\begin{aligned} G_{\Delta v\Delta d_i} &= \left.\frac{\hat{v}_{cd1} - \hat{v}_{cd(i+1)}}{\hat{d}_i - \hat{d}_{i+1}}\right|_{\substack{\hat{v}_{in}=0 \\ \hat{d}k=0\ (k\neq 1) \\ i=(1,2)}} \\ &= -\frac{s\dfrac{V_oL_f}{3nR_o} + \dfrac{V_oR_L}{3nR_o} + \dfrac{V_{in}D}{3n^2}}{s^2C_dL_f + sC_dR_L + \left(\dfrac{D}{n}\right)^2}. \end{aligned} \tag{13}$$

B. Regulator Loop Design

The specifications of the ISOP system are shown in Table I:

There is one OVR control loop and two IVS loops sharing the same structure and parameters with the proposed control scheme. Thus, we can take one IVS control loop gains as an example. Fig. 5 shows a system block diagram, where $G_{verr1}(s)$ and $G_{v0}(s)$ are the transfer functions of the compensators for one IVS and one OVR respectively. V_{Dpp} is the amplitude of a digital triangle waveform although it is a

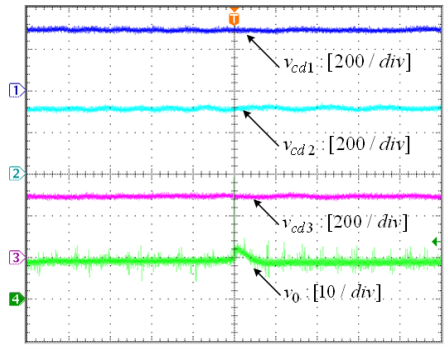

Fig. 12. Response to the load stepping down.

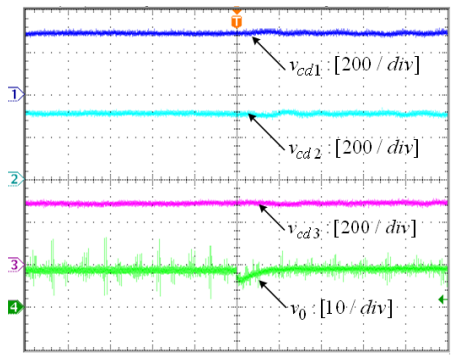

Fig. 13. Response to the load stepping up.

dummy, which can be calculated through the A/D sampling results and the values of the period registers. The transfer functions for the output impedance and the audio susceptibility are denoted as $Z_{out}(s)$ and $G_{vg}(s)$.

In Fig. 5, it is easy to get the loop gains of the OVR loop by:

$$T_{vo}(s) = 3K_{vo}G_{vd}(s)G_{vo}(s)/V_{Dpp}. \quad (14)$$

The IVS control loop gains can be expressed as:

$$T_{vo}(s) = K_{verrc}G_{verr1}(s)G_{\Delta v\Delta d1}(s)/V_{Dpp}. \quad (15)$$

Based on the parameters for the ISOP configuration, the voltage sensor gains for the OVR and IVS loops are 0.1 and 0.006 respectively. V_{Dpp} is 6V. Both proportional-integral (PI) type compensations for output voltage and input voltage sharing control are made. During the uncompensated condition, the transfer functions of compensator $G_{verr1}(s)$ and the compensator $G_{v0}(s)$ equal 1. The crossover frequency of the OVR loop is chosen to be 5kHz which is roughly one-seventh the switching frequency. In Fig. 6, the original loop gain of $G_{vd}(s)$ has a magnitude of -30dB at 5kHz, but after compensation, the compensated loop gain has a crossover frequency of 5kHz with a phase margin of $40°$. The bode diagram of the open loop transfer function $G_{\Delta v\Delta d}(s)$ is shown in Fig. 7, where the compensated loop gain has a crossover frequency of 3kHz with a phase margin of $30°$.

IV. Experimental Results

Experiments on a prototype with the same parameters as those shown in the loop gain analysis have been made. It should be pointed out that the turns ratios of each module is not the same in fact. The turns ratios of transformer T1 and transformer T3 are both 4:1, while the turns ratio of T2 is 3:1. The digital control strategy for the proposed ISOP converter has been implemented by a DSP (TMS320F2812).

TABLE I
System Specifications

Item	Value	Item	Value
Rated input voltage V_{in}	800V	Output capacitor C_f	1.0mF
Output voltage v_0	10V	ESR of output capacitor R_{cf}	50mΩ
Rated load R_0	1Ω	Output inductors L_f	0.1mH
Switching frequency f_s	33kHz	ESR of output inductors R_L	100mΩ

The TTF module contains the following power devices:

1) Switching devices: IXFH44N50P.
2) Diodes (clamping diodes, rectifier diodes and freewheeling diodes): DSEI30–06A.

Fig. 8 shows the gate signals for all of the modules with the proposed digital control strategy interleaved at full load, which can reduce the output current ripples. Because the turns ratio of T2 is less than those of the other two modules, the duty ratio for module 2 is smaller than those of module 1 and module 3 while the duty ratios of module 1 and module 3 are the same for identical turns ratios. Fig. 9 shows the primary voltages of the transformers in the system at full load under the steady state. Their amplitudes reveal that the corresponding individual input voltages are equal due to the excellent IVS control. Fig. 10 illustrates the individual converter input voltages corresponding to a step change in the input voltage from 660V to 960V. As can be seen, before and after the transient, the input voltage can be shared equally among the three modules. Fig. 11 shows the individual converter input voltages corresponding to a load stepping between half load (5A) and full load (10A). Despite the transients, the total input voltage can be shared well too. Fig. 12 and Fig. 13 show the response of the individual input voltages and the output voltage during a load transient between full load and half load. As can be seen from the figures, with the proposed control strategy, the individual input voltages are almost unaffected when facing a load transient.

V. Conclusions

This paper proposes a digital control strategy for an ISOP converter consisting of double-switch forward type DC/DC converters, which can be used in high voltage input applications with low voltage rating switches. It is simple to generate interleaving PWM gate signals for the switches of each module, reducing the output current ripples as well as the size of output inductors. Small signal analysis of the ISOP converter has be made with the proposed digital control strategy. A 100W three module prototype has been built to verify the effectiveness of the digital control strategy. Both under steady states and transients, the input voltage can be shared equally among all the modules despite turns ratios mismatches.

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