Design of Temperature Stable FLL Circuit

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Abstract— **The FLL(frequency locked loop) circuit is used to generate an output signal that tracks an input reference signal. The locking time of FLL is short compared to PLL(phase locked loop) circuit because the output signal of FLL is synchronized only in frequency. Also the FLL is designed to allow the circuit to be fully integrated. In this paper, the temperature stable FLL circuit is designed by using full CMOS transistors. When the temperature is varied from -20 °C to 70 °C, the variation of output frequency is about from -2% to 1.6% from HSPICE simulation results.**

Index Terms— **temperature stable characteristics, voltage reference, frequency locked loop, frequency-to-voltage converter, voltage controlled oscillator,.**

I. INTRODUCTION

A PLL is a frequency-selective feedback system which can synchronize with a selected input signal and track the frequency change. The PLL is a very versatile circuit block suitable for a variety of frequency selective signal demodulation, signal conditioning, synchronization and frequency synthesis applications[1,2,3]. The PLL is a feedback loop comprised of a phase detector, low pass filter and VCO(voltage controlled oscillator)[2]. The output voltage of the phase detector is the phase difference between the input signal and the VCO output signal and produces an output voltage that is related to this phase angle difference. In PLL the high frequency components are removed by the low pass filter. And then the output of the low pass filter is amplified and applied as the control voltage of the VCO[2]. However the PLL can't be fully integrated because the low pass filter has to be implemented externally with discrete components[4].

A FLL is similar to a PLL in the way that it generates an output signal which tracks an input reference frequency. But the FLL circuit has a simple structure compared to PLL which contains a FVC(frequency-to-voltage converter), a VCO and an opamp(operational amplifier)[4,5]. The operation of FLL circuit is based on frequency comparison by the two FVC circuit blocks. It generates an output signal which tracks an input reference frequency. The designed FLL circuit is based on frequency comparison by the FVC which does not required the charge pump and the low pass filter[4,5]. Therefore the designed FLL can be integrated on the one chip. The architecture of FVC circuit is built on the charge redistribution principle based on switching capacitor[6].

In this paper, the temperature stable FLL circuit is designed. In Section II the output characteristics of FLL circuit are described with temperature. In Section III the simulation results of the temperature stable FLL circuit will be shown with temperature. Finally, the conclusions show in Section IV.

II. FLL CIRCUIT IMPLEMENTATION

Fig. 1 shows the block diagram of the FLL circuit[5]. The FLL circuit is composed of two FVCs, two buffers, a VCO, and two frequency dividers.

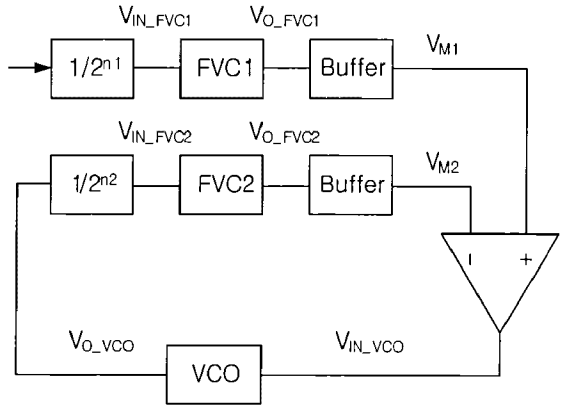

Fig. 1 Block diagram of the FLL circuit

First, the frequency of the input signal is divided by 2^{n1} and the output of the VCO is divided by 2^{n2} in the same way. The signals are converted to a voltage by the FVC1 and FVC2[7]. The circuits of FVC1 and FVC2 are the same structure. The output voltages, V_{O_FVC1} and V_{O_FVC2}, are linearly dependent on the frequency of the input signal. The frequency information is converted to the voltage signal by the FVC circuit. The buffer is used for driving which is implemented an opamp. The voltage difference between V_{M1} and V_{M2} is then amplified by the opamp and the output voltage of the opamp, V_{IN_VCO}, is employed to control the output frequency of the VCO. The voltage V_{M2}

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will increase or decrease until V_{O_FVC2} becomes equal to V_{O_FVC1}.

The temperature characteristics of FLL circuit were presented[7]. From the results, the change of output characteristics with temperature is nearly cancelled in frequency divider, FVC and buffer. Because the circuit blocks of frequency divider, FVC and buffer are the same structure the change of output signal is the same with temperature. And the change of VM1 with temperature contains the change of FVC1 and buffer1 and the change of VM2 with temperature contains the change of FVC2 and buffer2. And the VCO circuit input voltage, V_{IN_VCO}, is obtained by subtracting V_{M1} from V_{M2}. Thus the output change of frequency divider, FVC and buffer with temperature can be cancelled.

Fig. 2 shows the change rate of the buffer output voltage difference with temperature. The change rate is calculated by using eq.(4), eq.(5) and eq.(6).

$$F1 = \frac{V_{M1}(temp.) - V_{M1}(room\_temp.)}{V_{M1}(roomtemp.)} \times 100(\%) \quad (4)$$

$$F2 = \frac{V_{M2}(temp.) - V_{M2}(room\_temp.)}{V_{M2}(room\_temp.)} \times 100(\%) \quad (5)$$

$$F = F2 - F1(\%) \quad (6)$$

From Fig. 2, the temperature independent characteristics of FLL circuit can be obtained from the temperature stable VCO.

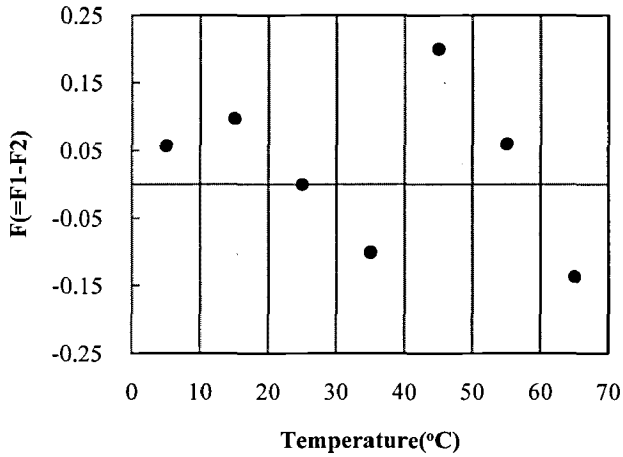

Fig.2 Change rate of buffer output voltage difference with temperature

A conventional VCO circuit consists of PMOS (MP15~MP29), NMOS (MN10~MN19), resistor (R3 and R4) and C as shown in Fig. 3. And PMOS (MP1~MP14), NMOS (MN1~MN9), resistor (R1, R2) are added to obtain the temperature stable VCO characteristics.

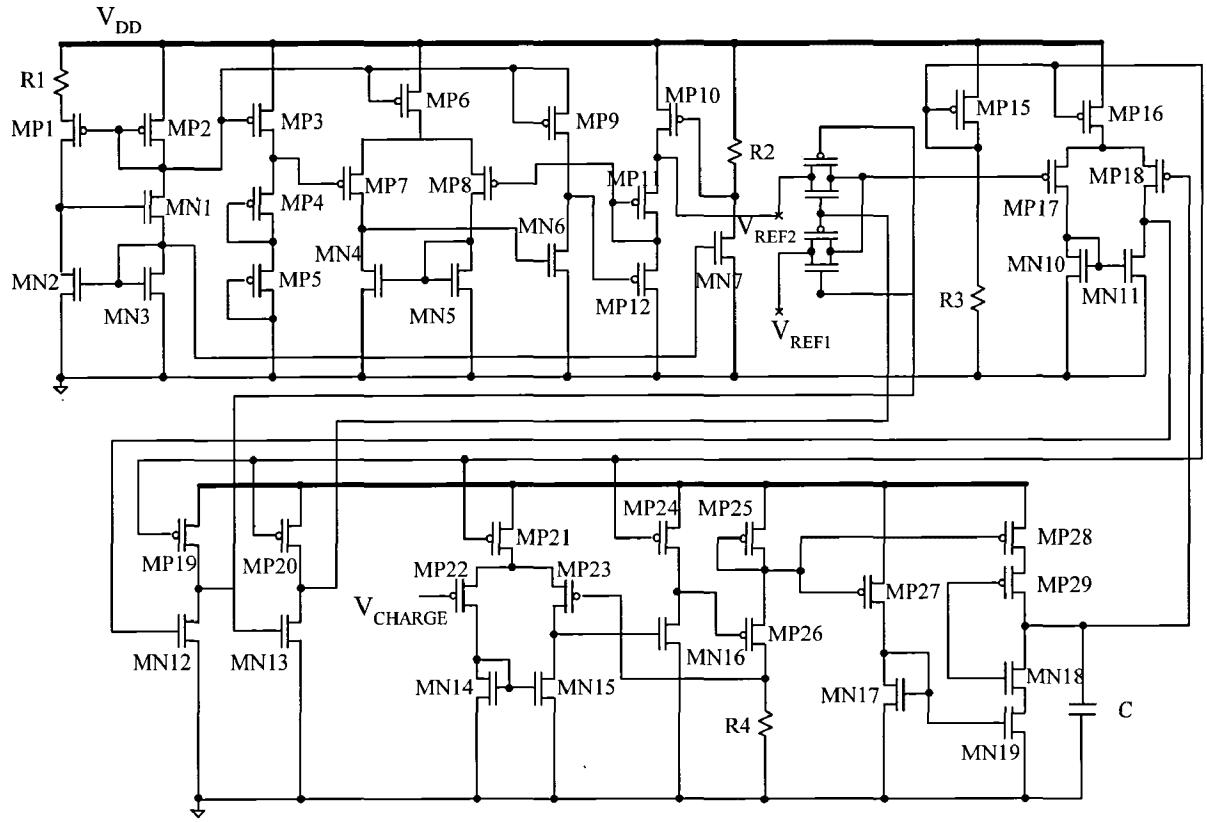

Fig. 3 Temperature stable VCO circuit

Fig. 4 shows the output frequency of the VCO with temperature. The output frequency decreases with increasing temperature because of electrical characteristics degradation. Fig. 5 shows the change rate of frequency compared to frequency in room temperature with the temperature. The error is calculated as follows:

$$Error = \frac{f(temp) - f(room\_temp.)}{f(room\_temp)} \times 100(\%) \quad (7)$$

When the temperature is varied from -20 °C to 70 °C, the change of output frequency is about from 4.1% to -6.2%.

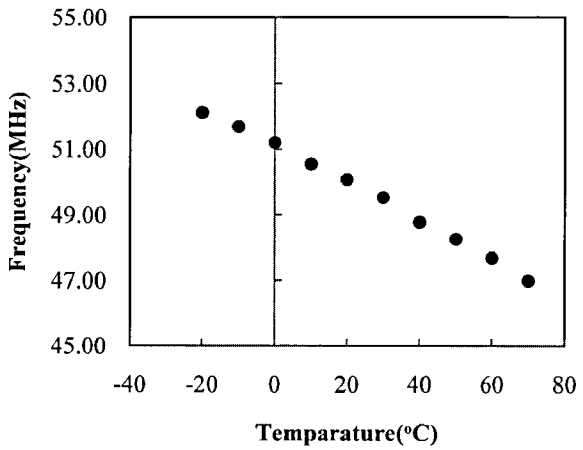

Fig. 4 Output frequency with temperature

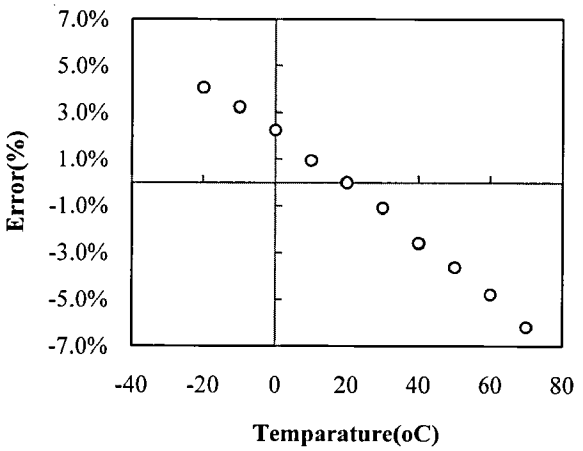

Fig. 5 Error with temperature

III. TEMPERATURE STABLE FLL CIRCUIT

In order to obtain temperature stable characteristics of FLL circuit the VCO circuit has to operate temperature independently. From Fig. 3 the output frequency of the VCO is calculated as follows:

$$f_O = \frac{V_{CHARGE} / R4}{C \times (V_{REF2} - V_{REF1})} \propto \frac{1}{R4C \times \Delta V} \quad (8)$$

V_{REF1} and V_{REF2} are the oscillation peak voltage of the VCO. If the multiplication of R4, C and the difference of V_{REF1} and V_{REF2} is constant in eq. (8) with temperature the temperature stable characteristics can be obtained.

In this paper, to obtain constant R4CΔV with temperature the VREF2 is controlled with temperature. The temperature dependent voltage reference is achieved by the bias circuit and comparator. In Fig. 3 the bias circuit is consists of R1, MP1, MP2, MN1, MN2 and MN3 and the comparator is consists of MP3 to MP12 and MN4 to MN6. Fig. 6 shows the VREF2 voltage with temperature, the VREF2 voltage decreases with temperature. The peak-to-peak voltage decreases to charge and discharge with temperature by decreasing the VREF2

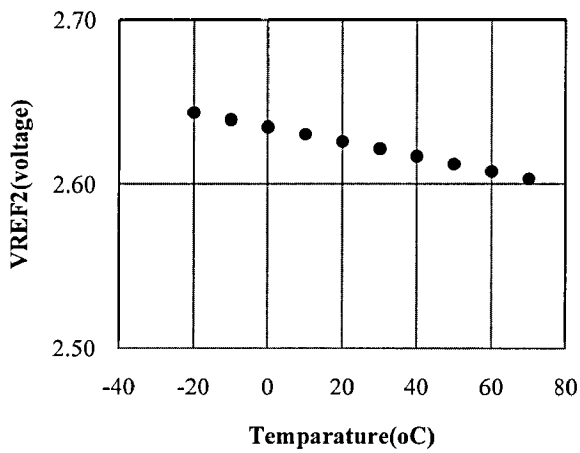

Fig. 6 VREF2 voltage with temperature

Fig. 7 shows the output frequency with temperature and Fig. 8 shows the error of the output frequency with temperature the error is calculated by using eq.(7).

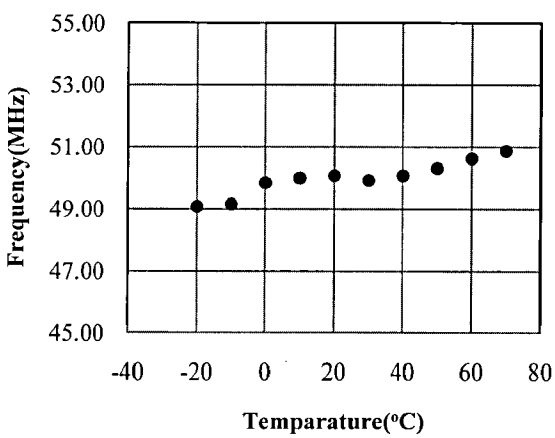

Fig. 7 Output frequency with temperature

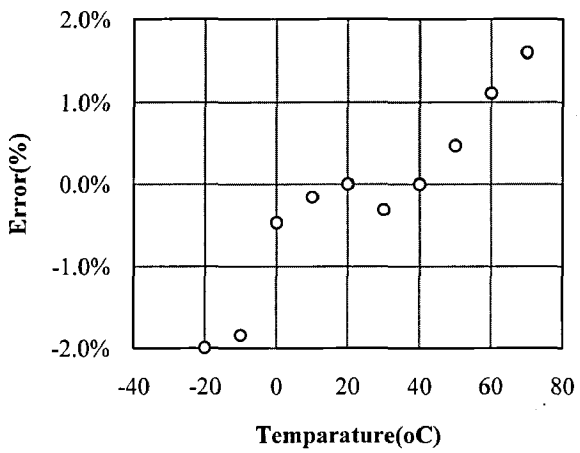

Fig. 8 Error with temperature

When the temperature is varied from -20 °C to 70 °C, the change of output frequency is about from -2% to 1.6%.

IV. CONCLUSIONS

The temperature stable FLL circuit is designed and the simulation carried out with HSPICE. The temperature variation of frequency divider, FVC and buffer was cancelled because the circuit structure is the same and the change of electrical characteristics with temperature is cancelled by the comparator. Therefore the temperature stable FLL can be obtained by temperature stable VCO. From simulation result, the operating characteristic of FLL with temperature shows enough good compared to conventional FLL.

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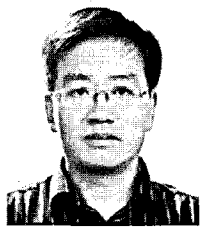

Jin-Ho Choi (M'85–SM'87–F'92) received the B.S. degree in electronics from Busan University in 1985, and the M.S. degree in electronics from KAIST in 1987. He received the Ph. D. degree in electronics from KAIST in 1992. From 1992 to 1996, he was a researcher at Hynix Semiconductor Inc.. Since 1996, he has been a professor in Dept. of Computer Engineering, Pusan University of Foreign Studies. His research interest includes VLSI design.