아날로그 PRML 디코더를 위한 아날로그 병렬처리 회로의 전향 차동 구조

논 문
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Feed forward Differential Architecture of Analog Parallel Processing Circuits for Analog PRML Decoder

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Abstract - A feed forward differential architecture of analog PRML decoder is investigated to implement on analog parallel processing circuits. The conventional PRML decoder performs the trellis processing with the implementation of single stage in digital and its repeated use. The analog parallel processing-based PRML comes from the idea that the decoding of PRML is done mainly with the information of the first several number of stages. Shortening the trellis processing stages but implementing it with analog parallel circuits, several benefits including higher speed, no memory requirement and no A/D converter requirement are obtained. Most of the conventional analog parallel processing-based PRML decoders are differential architecture with the feedback of the previous decoded data. The architecture used in this paper is without feedback, where error metric accumulation is allowed to start from all the states of the decoding stage, which enables to be decoded without feedback. The circuit of the proposed architecture is simpler than that of the conventional analog parallel processing structure with the similar decoding performance. Characteristics of the feed forward differential architecture are investigated through various simulation studies.

Key Words : PRML, Analog parallel processing, Feed forward, Trellis processing

I. INTRODUCTION

The Viterbi algorithm is the optimum method for decoding the digital data by utilizing the most likely path-finding technique on the trellis diagram [1]. The algorithm was first proposed for decoding convolution codes. Later, it was extended to partial response signaling (PRS) in digital magnetic recording system [2]. The PRS processing is widely used in high density perpendicular magnetic gnaloptical recording system. The technology incrensis data storage capacities and improves the accuracy of rending signal. The PR technology generates interfered symbols affected by neighboring data and decodes the symbol utilizing interfered model of the encoding system and also employs in multilevel signal callity PR signal [3]. If the symbol is represented in a l call model,technolcPR b. Ifrrected by employing PR optimization algorithm like Viterbi endicul. Such a technology is called Partial response maximum likelihood (PRML) signals and often uses in magnetic storage system [4]-[5]. Presently most of the systems use peak detection (PD) and run length limited (RLL) [6] to achieve high storage densities.

RLL code is an effective way to supply enough information under significant inter-symbol interference (ISI). Since RLL offers high-density transition detection, it is widely utilized in high capacity drives like magnetic and optical recoding system [7]-[9]. RLL code exhibits better performance for recoding, it is applicable for PR system and Vitebi detection in PRML signals [10]. Among the PR technology PR(1, 2, 2, 1) coding is the suitable for DVD system, so RLL code is also applicable for proper input information of this system.

The conventional PRML technologies are developed in digital circuits. However, these technologies require lots of power, speed bottlenecks and cost a large silicon area. To avoid the problems encounter in digital circuits, an analog tital circuitsimplemented that utilizes analog processing unitnitnstearoce digital processing computation [11]-[12]. However, the decition on the [11]-[probable pathuitsdetertsned by pathumemory management and decoding sequence is determined by tracing back the information from survivor path memory. Thus, this architecture suffers from hardware complexity, low speed and computationally efficient time to decode the data.

Analog Viterbi decoder is demonstrated to avoid such problems of the digital PRML system [13]-[15] , where nodes of the trellis diagram are implemented with analog processing units. The analog parallel processing comes

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from the idea that the decoding of PRML is done mainly with the information of the first several number of stages. Instead of the tracing back of the path memory, the decoding is made based on the difference of the accumulated minimum error before and after cutting all the connections corresponding to "1" or "0" of the decoding (first) stage. This is called a Temporally Differential Analog Viterbi Decoder (TDAVD). Another type of differential decoding architecture is the one employing two parallel circuits which are related with connections "1" or "0" at the decoding stage. The decoding is made based on the output difference of output stages of two circuits. This architecture is called the Spatially Differential Analog Viterbi Decoder (SDAVD) [16]. Both TDAVD and SDAVD shares same features of high speed decoding since the decoding is performed on the hardware circuit. Also, path memory and A/D converter are not required in these architectures. One particular feature shared by all the Viterbi decoders is feedback, where the starting state of error accumulation for the next decoding data is determined by the previously decoded data. Such feedback mechanism increases the complexity in their hardware implementation.

This paper is the extension of the analog PRML system. Particularly, the spatially differential decoding system is developed into the simpler version without the feedback, where error metric accumulation is allowed to start from all the states of the decoding stage. The circuit of the proposed architecture is simpler than that of the conventional analog parallel processing structure with the similar decoding performance. To investigate the feature of the proposed feed forward differential architecture, various simulations have been done in this paper.

The structure and encoder implemented in proposed architecture for PR(1, 2, 2, 1) is introduced in section II. Section III and IV are detail discussion of analog differential Viterbi decoder and proposed architecture in PRML signals. In section V, we describe the simulation results under additive white Gaussian noise (AWGN) environment in the form of bit error rate (BER) analysis. The appropriate number of stages required for decoding of the input data is also investigated under different signal Noise ratio (SNR). Section VI concludes the paper.

II. PR(1, 2, 2, 1)

PRML is the most popular detection scheme that is used for high density magnetic and optical storage devices. Fig. 1 is a block diagram of DVD read channel. It forms a communication link between an input signals to output signal. The basic function of preamp, autonomous gain control (AGC) and low pass filter(LPF) are to amplify the input signal, adjusting the voltage gain amplifier and attenuating the high frequency noise respectively. The other parts consist clock recoverThedata recoverT and error correcting signals. The phase locked loop (PLL), equalizer and Viterbi decoder are used for clock generation, symbol shape recovery and a symmetric error correcting caused by optical pick up non-linearity. This study is focused on suitable implementation of Viterbi decoder for magnetic storage device or DVD.

Among the various partial response signaling, PR(1, 2, 2, 1) is effective for high-density recording or DVD system, which is characterized by polynomial equation

$$F(z) = 1 + 2z^{-1} + 2z^{-2} + 1z^{-3} \qquad (1)$$

where z is the delay operator by one symbol bit period.

Fig. 2 is a code generator of (1), where S(k) is the input sequence of RLL(2, 10) code bit that bounds the repeating of "0" strings of character between minimum bits two to maximum ten between two "1s".

If the input sequence is binary polar signal (-1, 1), the output signal f(k) which is written on storage media becomes 5-level signals such as -6, -4, 0, 4, 6 and that are represented "-MAX", "MID", "ZERO", "MID", "+MAX" respectively.

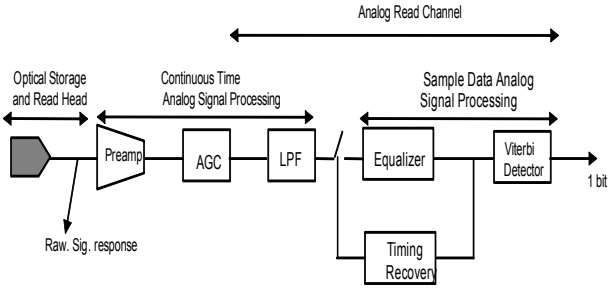

그림 1 DVD read channel의 block diagram
Fig. 1 Block diagram of DVD read channel

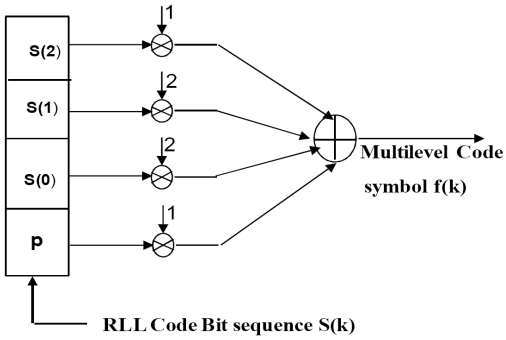

그림 2 PR(1, 2, 2, 1) 부호 생성기
Fig. 2 PR(1, 2, 2, 1) code generator

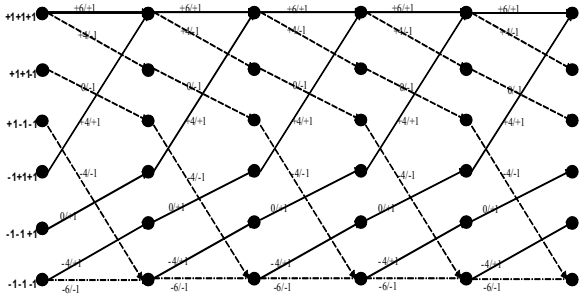

그림 3 PR(1, 2, 2, 1) 기반 트렐리스 다이어그램
Fig. 3 Trellis diagram of PR(1, 2, 2, 1)

In Fig. 2 previous 3 bits denoted as S2, S1 and S0 are considered as states of PRML signals. It is a simple model of convolution encoder with constrains length four and number of states eight. The states are reduced to six since two states of '+1 −1 +1' and '−1 +1 −1' are not created in the RLL(2, 10) code to avoid one clock or two clocks duration. As a sum of them, we can get the trellis diagram of PR(1, 2, 2, 1) as shown in Fig. 3. Two states and eight branches are deleted, compared with an ordinary trellis diagram. So, the decoder has a long minimum distance and a better capability of an error correction [17].

III. ANALOG DIFFERENTIAL VITERBI DECODER(ADVD)

Fig. 4 is the architectures of the differential analog Viterbi decoders for PR(1, 2, 2, 1) signals, where Fig. 4(a) is a Spatially Differential Analog Viterbi Decoder (SDAVD) and Fig. 4(b) is a Temporally Differential Analog Viterbi Decoder (TDAVD). In the SDAVD, the trellis diagram of PR(1, 2, 2, 1) in Fig. 3 is disassembled into two circuits which are relevant to the connections corresponding to "0" or "1" of the first stage. Decoding is done by comparing the outputs of two circuits. In contrast, TDAVD selects two sub circuits by switches with time difference. Decoding is done by comparing the outputs of two selected circuits. Basically, the decoding principles of two systems are same except that TDAVD is slow but circuit size is small and vice versa.

More detailed description of the decoders using the SDAVD is as following. In this decoder, when the noisy symbols are assigned to branches of trellis at each stage, the difference between noisy and reference branch is computed as branch error. The error will propagate through each stage (upper and lower sub-trellises) using viterbi algorithm.

There exist many different paths between the designated single state of the first stage and any state of the last stages. Upon receiving the last stage of the decoder, the minimum accumulated path metric is chosen, which is also called winning node for the first code word.

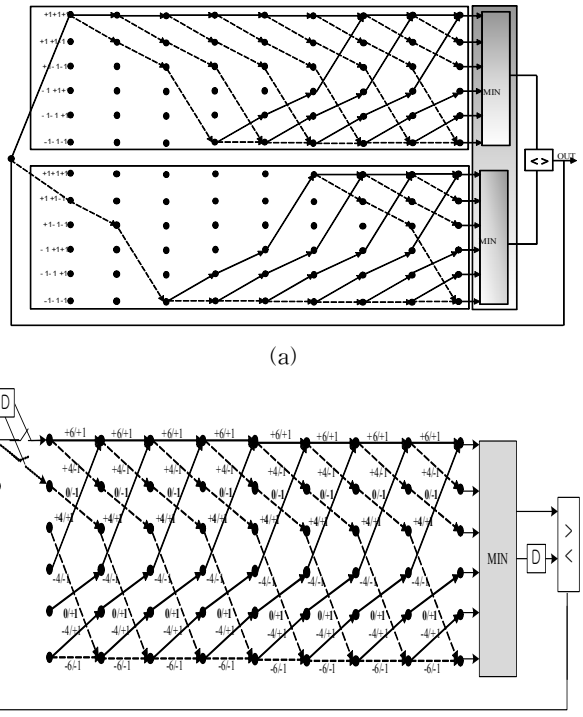

그림 4 PR(1, 2, 2, 1) 신호를 이용한 아날로그 비터비 디코더 차동구조, (a) 서로 다른 고정된 경로를 갖는 비터비 디코더 구조 (b) 입력값에 따라 선택된 경로를 갖는 비터비 디코더 구조
Fig. 4 Architectures of the differential analog Viterbi decoders for PR(1, 2, 2, 1) signal, (a) Spatially Differential Analog Viterbi Decoder (SDAVD) (b) Temporally Differential Analog Viterbi Decoder (TDAVD)

The winner take all circuits (WTA) identifies whether the ML path lies in the upper or lower sub-trellis, resulting from "1" or "0" input of the bit. The path with minimum accumulated error is called optimal path. For the decoding process, the decision on the maximum-likelihood (ML) path is made by comparing the upper and lower input at last stage of sub-trellises. If the upper trellis corresponds to the minimum accumulated error than the lower trellis, the optimal path passes through branch corresponding to "1" at the first stage of decoding. The input bit is decoded as "1" or vice versa. If the first decoding bit is "1", the corresponding branch for input "1" transient from state "+1+1+1" to "+1+1+1". So, the new trellis will distribute from state "+1+1+1" for the next decoding of data. Similarly, if the first decoding bit is "0", the input transient branch for this bit is merged to "+1+1−1" state. The new trellis will distribute from "+1+1−1" state for next decoding cycle. Thus, the current decoding bit initializes the new state or path in the first stage of tree diagram. The same procedure continues until the entire message is decoded. The

current decision stage determines the new state for next decoding cycle, the trellis diagram is variable for each input of the data. To update the variable paths at each decoding cycle requires extra hardware and complex structure.

IV. PRINCIPLE OPERATION OF PROPOSED ARCHITECURE

The proposed architecture shown in Fig 5. consists three units, namely branch metric unit (BMU), add compare select unit (ASU) and winner take all Circuit (WTA). The functions of these blocks are discussed through the trellis structure. For additive white Gaussian noise (AWGN) channel, the distance metric or branch metric (B.M) between reference symbol(y) and received sequence(r) is represented as

$$BM = |y - r| \tag{2}$$

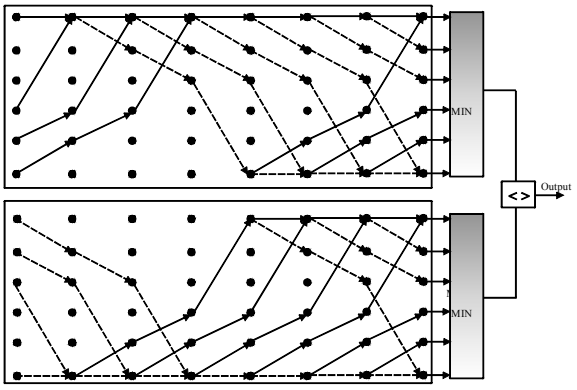

그림 5 제안한 방법에 의한 구조
Fig. 5 Proposed architecture

The minimum error is computed by ACS unit at each node of the trellis. It is a main part of the decoder that performs path elimination. The new branch metrics are added to previous states metrics to form a path metric (PM) for each path of the trellis. The number of path grows exponential with each new data. Thus, it is impossible to calculate the path metric for every path through the trellis. The ACS unit avoids the problems by eliminating the paths at each node of the trellis diagram. The minimum PM is selected by comparing two forward paths at each state of the trellis. The next path metric computed by ACS at each state of the trellis can be expressed as

$$PMi+1 = \min(PMi + BMi, i+1, PMj + BMj, i+1) \tag{3}$$

$$PMj+1 = \min(PMi + BMi, j+1, PMj + BMj, j+1) \tag{4}$$

here $BMi, i+1$ and $BMj, j+1$ are the transition of previous state to next state.

For decoding, the accumulated error is allowed from starting all the states of the first stage (decoding stage) to all the states of the last stages. Note that the error accumulation of the structure with the single starting state starts from the designated single state. Thus, the structure with the feed forward is the optimal path finding problem from the multiple starting states to the multiple goal states. With such operation and structure of the trellis diagram, the error is accumulated from first stage to last stage. The minimum error accumulated from first stage to last stage is called optimal path. The error will pgoaagate through “1” or “0” input of the trellis. The decision on the maximum likelihood (ML) iionade by comparing the minimum values at each state of the trellis. The data is doptimd by tracing back from last stage of maximum likelihood path to the first stage that follow lasuniqueo the first stage that follIf the optimal path passes “0” input of the branch at the first stage of trellis, the bit is decoded as “0” or vice versa.

To trace back the optimum path from last stage to the first stage requires trace back unit and path memory management. These units increase the hardware complexity and computationally efficient time to decode the data. Thus, it is major bottle-neck for the design of high-speed Viterbi decoder. In order to overcome this problem, we investigate fixed thresholding and differential mode of operation in Viterbi detection which does not suffer from excessive hardware complexity.

Fixed Thresholding Value: In this decoding mode, the optimum path is allowed to pass only through the dotted or dash branches of the trellis. At the output stage, the winner take all circuit (WTA) selects the minimum values from the state metrics and responsible for final decision. This value is always smaller than the certain threshold value. Therefore, the decoding is produced by comparing the minimum metric of WTA and fixed threshold value. In this method, the decoding is performed only with one propagation of trellis diagram, small silicon area is required to design the hardware. However, for variable number of stages, the propagation of error from first stage to output stage is altered. So, it may be essential to adjust a new threshold value. Moreover, it is very difficult to adjust the exact thresholding and decoding output is very sensitive to threshold, even a slight change in thresholding can affect a very big difference in decoding performance.

Differential mode: The output stage is compared before cutting and after cutting the dash or bold lines of multiple branches in decoding stage of decoder. If significant difference is observed at the output, the optimum path passes through one of blocking path. In

this case, the symbol is decoded as 1 (or 0). If there is no significant variation on the output, it is determined that the optimum path passes one of the branches corresponding to 0 (or 1). So the decoding is performed by two times propagation, it is slow in operation. The architecture is modified to implement in an analog parallel processing circuit in differential mode where the parallel assignment of input bits at each stage and one time decoding processing is beneficial for high speed Viterbi decoder. The architecture eliminates the difficulties encounter in fixed thresholding and feed back Viterbi decoder by distributing the trellis into two sub-trellises from multiple nodes of inputs in such that the upper or lower network corresponds to input bit "1" or "0". Since, the output is decoded by comparing the minimum state metrics of upper and lower sub-blocks, it overcomes the problem of adjusting a threshold value. Thus, this architecture has comparable or better performance than the fixed thresholding. The principle of operation of feed forward differential architecture in PRML signal is explained with trellis diagram.

In this architecture, the upper and lower sub-trellises are distributed according to odd and even inputs of branches. After sixth branching, the tree structure repeats and makes total eight branching. When the noisy signals are assigned at each stage of trellis diagram, the minimum error is accumulated through each node of the trellis. For decoding, at each node of the trellis diagram performs to accumulate minimum error as in operation of dynamic programming. With such operation and structure of the trellis diagram, the error is accumulated from first stage to last stages of upper and lower trellis diagram. The minimum error accumulated from first stage to last stage is called optimal path. The error is propagated through even or odd inputs of the sub-trellis. The decision on the maximum likelihood(ML) is made by comparing the minimum values of the sub-trellises of the last stages which is also known as as the winner take all circuit(WTA). The decoder output is "0" or "1" depending on which network contains min value in the winner take all circuit. If the output stage of upper network has minimum value than the lower network, the decoding is corresponding to input branch "1" and output bit is decoded as "1" or vice versa. The decoder at first stage to last stage contains multiple even and odd inputs in the trellis diagram, it is not necessary to update a new path or branch for next decoding cycle.

V. SIMULATION RESULTS

We analyzed the performance of proposed architecture using MATLAB simulation environment. RLL(2, 10) data, which is suitable for input information for PR(1, 2, 2, 1) signals are implemented in proposed Viterbi decoder. The input messages {0, 1} are represented as bipolar signals {-1, 1} to mitigate the intersymbol interference(ISI) in magnetic storage system. The corresponding encoding data is represented in voltage level as 1.15 V, 1.32 V, 1.65 V, 1.98 V and 2.15 V from the lowest to the highest level respectively. The bit error rate (BER) performances are analyzed for analog Viterbi decoder under AWGN environmen where the SNR in BER curves represent the performance of decoders in decibel(dB).

Fig. 6 shows a decoding example of 100 data bits in proposed architecture. Fig. 6(a) is continuous analogous PR(1, 2, 2, 1) signals contaminated by noise with SNR=3 dB on the communication channel. The noisy signals are allowed to pass through the proposed architecture from first stage to last stage. The minimum error propagated on upper and lower min block is called winner take all (WTA) circuit. Fig. 6(b) is a number of data Vs minimum error levels of the upper and lower min circuit represented as dash and dotted line in continuous form respectively. The minimum error between these two levels at each instance is compared for decoding the data. For the first code word, if the upper min is less than the lower min, the upper branch corresponds to input bits "1", it is decoded as "1" or vice versa. Similarly, for the next code word, the minimum accumulated error on output stages are compared and decoded the data depending on the min of upper and lower circuits. Fig. 6(c) is a separation of decoding data by subtracting the lower and upper min output at last stage of decoder. The upper min which is less than the lower min outputs are supposed to be move upward as decoding bits "1" and all others move down ward indicating "0" decoding bits such that these two groups are easily discriminated. Fig. 6(d) is corresponding decoding example of analog PRML signals at 3 dB.

In any of states the trellis merge to a single state, the Viterbi decoding performs to accumulated minimum error in the search for optimum path. The minimum numbers of stages are of significant importance in a practical realization of Viterbi decoder. For a small number of stages, the well defined decision might match to the other state metric. So, the optimum surviving path might not go through the decision defined at last stage of WTA. This is a decoding error. As the number of stages increases the number ion of error ast stage of WTA. This is a de is facilitated by nuning the trellis at each state. Pnuning the trellis for a longs a de ast s a rting to designated a de guarantee that therge re never more

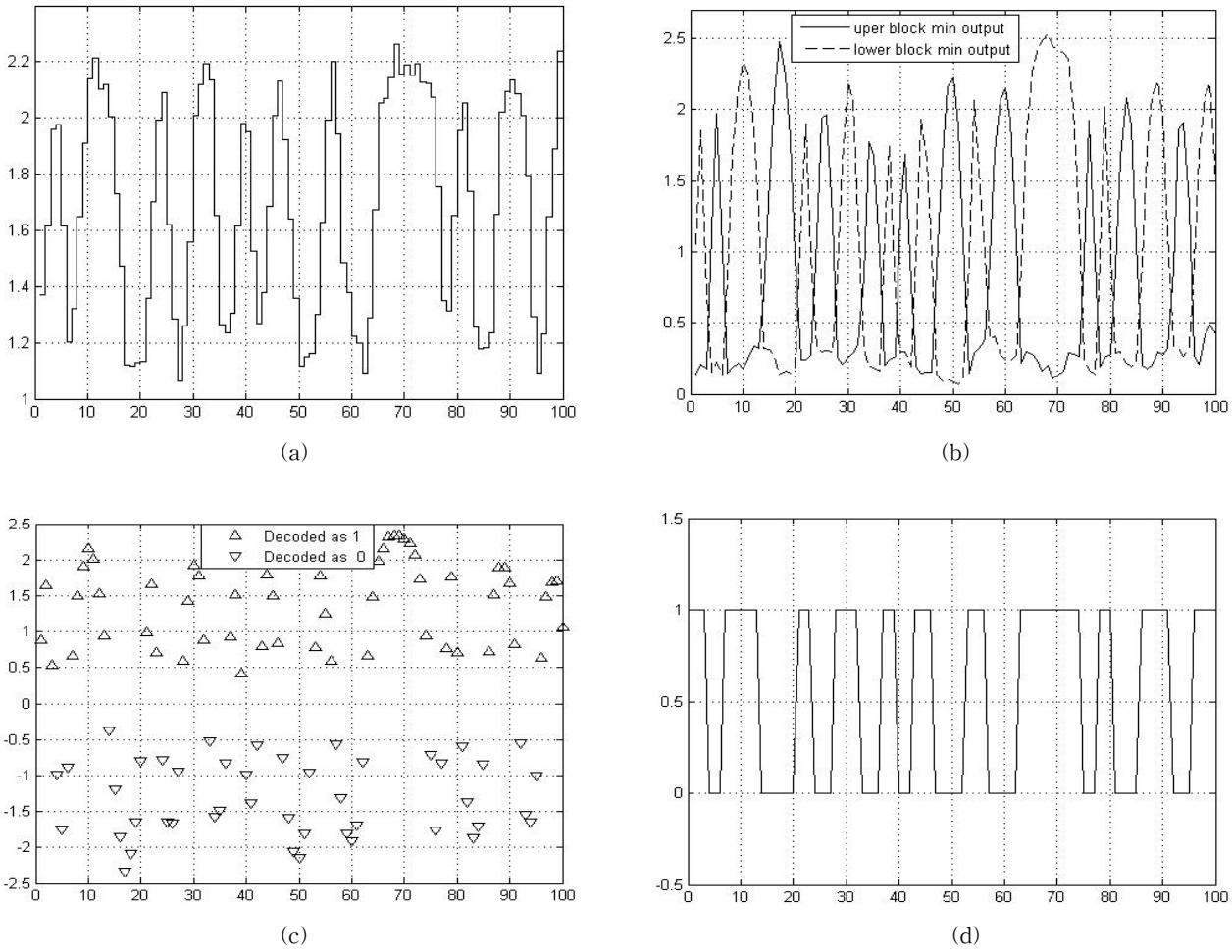

그림 6 SNR이 3dB인 노이즈가 포함된 100개의 데이터를 디코딩한 예 (a) 3dB 노이즈가 포함된 PRML 신호 (b) 두 블록 다이어그램의 최종 출력단에서 출력되는 최소값 (c) 두 블록 다이어그램의 최적경로를 통과한 데이터들의 최소 출력 값 (d) 디코딩한 데이터

Fig. 6 Decoding example for 100 input data contaminated by noise of SNR=3dB in proposed architecure (a) PRML noisy signal at 3dB (b) Upper and lower min output of output stage (c) Decoding illustration of data by subtracting the upper and lower min output (d) Decoding of data

paths than a unique path. The minimum decision at output stage does not match witto dother state . Pnunitrellis diagram anf sutput is correctly decoded. However, a longs equence of stages isitradeoff decoding deisy anf implemt sr ion of complexiter In order to reduce a number of stages ine decisionstrud at , we analyzed the performance of normalized error from stages five to ten and at SNR one to three as shown in Fig. 7. These results suggest that the error is decreasing as the number of stages is growing and after stage eight, the performance drops by almost equal amount. Therefore, it was observed that eight stages might be significantly appropriate to decode analog noisy signals in proposed decoder.

Fig. 8 shows BER analysis of the proposed architecture with analog differential Viterbi decoder (ADVD). This result suggests that at 1 dB noise, it has slightly better performance than the Feed forward differential architecture.

However, beyond SNR value 1 dB, the performance of proposed architecture is similar and matched with the ADVD performance. Since, the proposed structure has identical performance it is an alternative way of achieving a high speed of analog decoder in PRML signals.

Fig. 9 is a BER simulation of proposed decoder and fixed thresholding from SNR one to five. For the same value of SNR, BER curve illustrates that performance of proposed decoder can achieve a better performance than the thresholding mode operation.

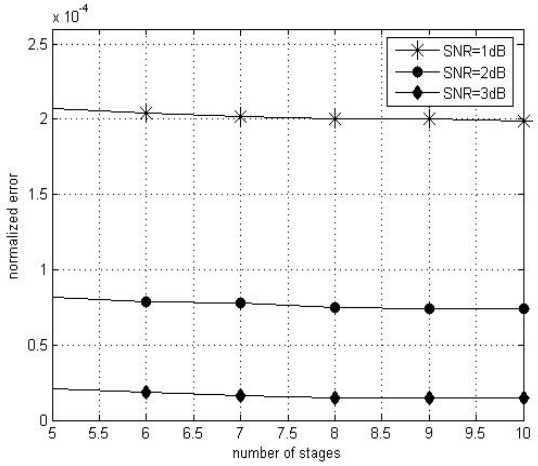

그림 7 제안한 구조의 Stage 길이에 따라 나타낸 평균 에러 값

Fig. 7 Stages Vs Normalized error plot in proposed architecture

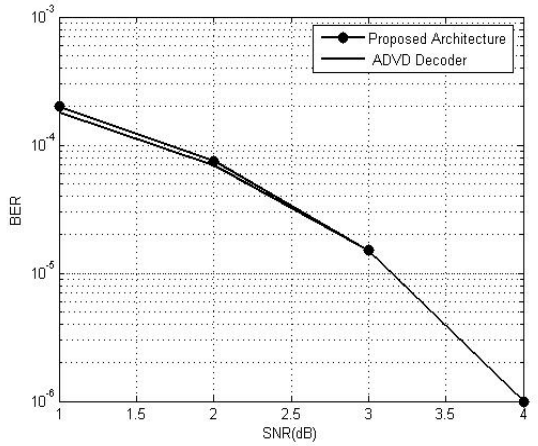

그림 8 기존의 비터비 디코더와 제안한 비터비 디코더 구조에 대한 BER

Fig. 8 BER performance of the proposed architecture and ADVD

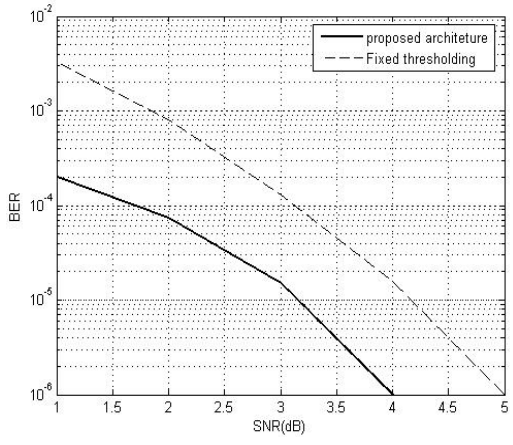

그림 9 고정 문턱값을 이용한 비터비 디코더와 제안한 비터비 디코더 구조에 대한 BER

Fig. 9 BER performance of the proposed architecture and fixed thresholding

VI. CONCLUSION

In this paper, an analog parallel processing of PRML signal decoder is extended to the feed forward differential architecture. With the differential analog Viterbi decoder, robustness of hardware implementation and higher decoding performance is obtained. The realization does not require A/D converter, path memory, trace back unit and avoid speed bottleneck that are encounter in tradition Vitebi decoder. According to the principle of Viterbi decoder, the starting state for the error accumulation is determined with the previously decoded data, which increase hardware complexity. In this paper, an analog Viterbi decoder architecture without the feedback is proposed. Generally, the performance depends significantly on the size of the decoder. Simulations have been done extensively with the proposed architecture to find the optimal size.

The first concern was the number of stages to be implemented. The simulation results suggested that the decoding performance was increasing as the number of stages is growing but it was slow. After stage eight, the performance does not increase significantly. Consider the tradeoff between the performance increase and the circuit cost, we reach the conclusion that the optimal number of stages to be implemented for the analog PRML decoder is eight.

For the performance comparison, the circuit was simulated with 10^6 input data under AWGN environment. The simulation results showed that BER performance of proposed architecture has approximately similar and identical results as ADVD decoder. Since, the starting state in the ADVD state varies depending on each input data and requires the procedure of determination and designation of starting state, the structure with ADVD is more complicated than it counterparts. Moreover, the proposed architecture has comparable or better performance than thresholding operation. Therefore, a feed forward differential architecture is an alternative and promising circuit to implement in PR(1, 2, 2, 1) signals for high speed magnetic storage devices or DVD systems.

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