Delay Time Reliability of Analog and Digital Delay Elements for Time-to-Digital Converter

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Abstract— **In this paper, the delay times were evaluated to develop highly reliable time-to-digital converter(TDC) in analog and digital delay element structures. The delay element can be designed by using current source or inverter. In case of using inverter, the number of inverter has to be controlled to adjust the delay time. And in case of using current source, the current for charging and discharging is controlled. When the current source is used the delay time of the delay element is not sensitive with varying the channel width of CMOS. However, when the inverter is used the delay time is directly related to the channel width of CMOS. Therefore to obtain good reliability in TDC circuit the delay element using current source is more stable compared to inverter in the viewpoint of the variation of fabrication process.**

Index Terms— **delay element, time-to-digital converter, current source delay element, inverter.**

I. INTRODUCTION

TIME information can be converted to digital value by using TDC circuit. It has been widely used in many applications such as laser range finder, frequency analysis or phase analysis[1]-[4]. For many years the main methods used to achieve the hundreds of pico-seconds resolution have been based on time-stretching and tapped delay line. These technique can be implemented both in analog and digital devices. This work describes characteristics comparison of the analog and digital delay elements in the viewpoint of the channel width variation. In Section II the operation of TDC circuit is described. In Section III and Section IV the characteristics of the digital delay element and the analog element are described, respectively. Finally, the conclusions show in Section V.

II. OPERATION OF TDC CIRCUIT

Fig. 1 shows the block diagram of the conventional TDC circuit[4]. The TDC circuit is composed of a delay element, flip flop and logic circuit. The input signal, start signal, is delayed by the delay element as shown in Fig. 2.

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After t1 sec. the output signal of D_1 element is high if the delay time of D_1 element is t1 sec.. And after (n-1)t1 sec. the output signals of from D_1 to D_{N-1} elements are high. When the stop signal is high the output signal of delay elements is memorized in flip flops.

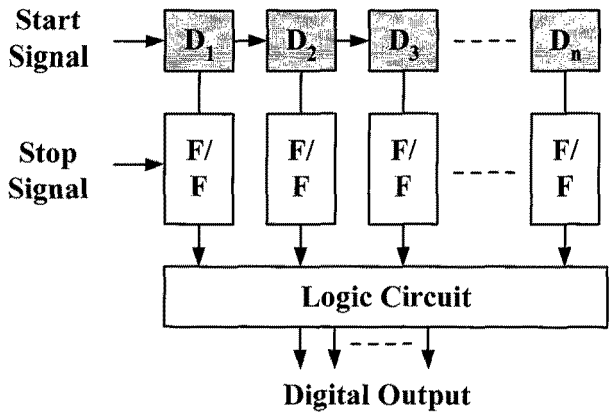


Fig. 1. Block diagram of the TDC circuit.

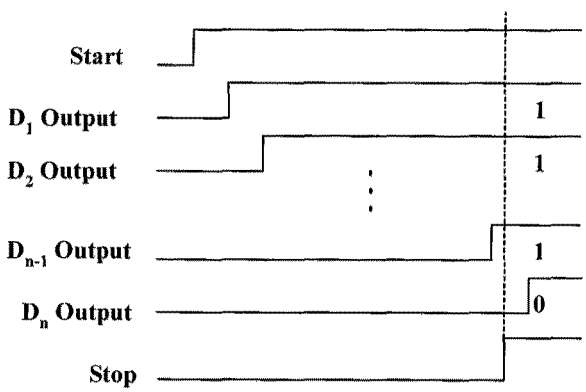


Fig. 2. Output signals of the delay element.

II. CHARACTERISTICS OF DIGITAL DELAY ELEMENT

The delay element can be designed by using the analog and digital devices. In case of using digital devices, the delay element is realized by even number of NOT gates as shown in Fig. 3. The delay time is controlled by controlling the number of NOT gates.

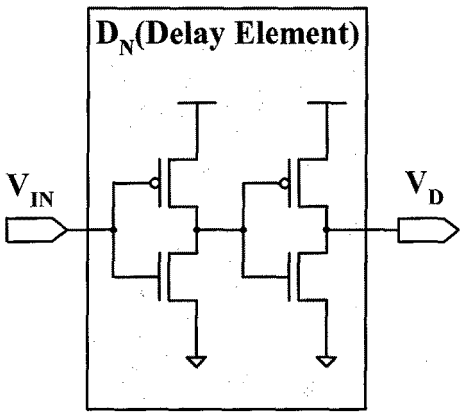


Fig. 3. Digital delay element using NOT gates.

The delay time of NOT gate is limited by the time taken to charge and discharge the load capacitance. The rising time is the time to rise from 10% to 90% of its steady-state value and the falling time is the time to fall from 90% to 10% of its steady-state value. The rising time and falling time are expressed as follows[5]:

$$t_f = 2\frac{C_L}{\beta_n(V_{DD}-V_{TN})}[\frac{V_{TN}-0.1V_{DD}}{V_{DD}-V_{TN}} + \frac{1}{2}\ln(\frac{19V_{DD}-20V_{TN}}{V_{DD}})] \quad (1)$$

$$t_r = 2\frac{C_L}{\beta_p(V_{DD}-|V_{TP}|)}[\frac{|V_{TP}|-0.1V_{DD}}{V_{DD}-|V_{TP}|} + \frac{1}{2}\ln(\frac{19V_{DD}-20|V_{TP}|}{V_{DD}})] \quad (2)$$

where β_n is $\mu_n C_{OX} Wn/Ln$, β_p is $\mu_p C_{OX} Wp/Lp$, V_{TN} is the threshold voltage of NMOS and V_{TP} is the threshold voltage of PMOS. From eq. (1) and eq. (2) the rising time and the falling time are related to the channel width and the channel length.

During the fabrication of the TDC circuit the channel width and the length can be changed compared to the layout of the channel width and length. Fig. 4 shows the change of the rising time and falling time in the digital delay element, NOT gates, when the channel width is varied from -10% to +10% during the fabrication process.

Fig, 5 shows the delay time with the width change and Fig. 6 shows the error rate with the channel width change. The delay time is calculated from the rising time and the falling time. When the channel width is varied from -10% to +10%, the error of the delay time is about from -3.5% to +2.9%.

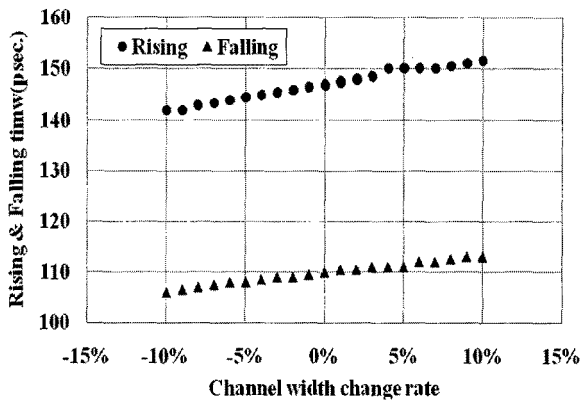


Fig. 4. Rise time and fall time with the channel width change.

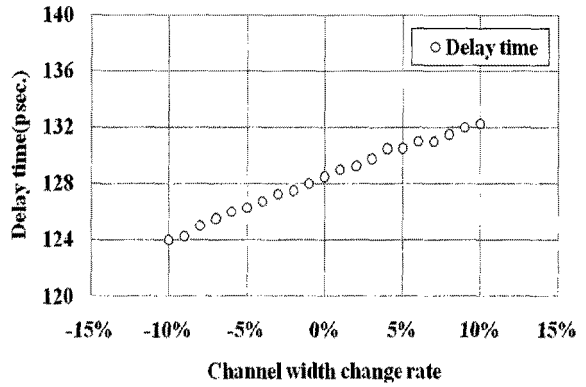


Fig. 5. Delay time with the width change.

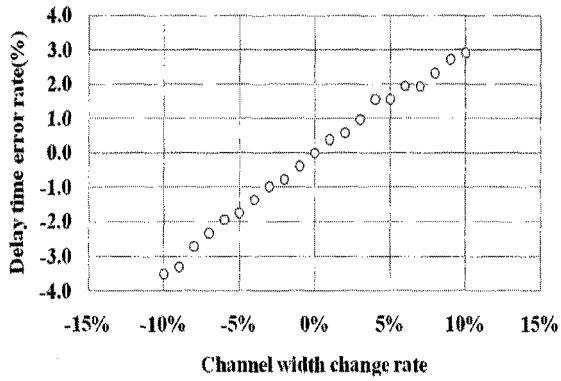


Fig. 6. Delay time error rate with the width change rate.

III. CHARACTERISTICS OF ANALOG DELAY ELEMENT

Fig. 7 shows the analog delay element circuit. In the analog delay element the delay time can be controlled by adjusting the reference current, I_{REF}.

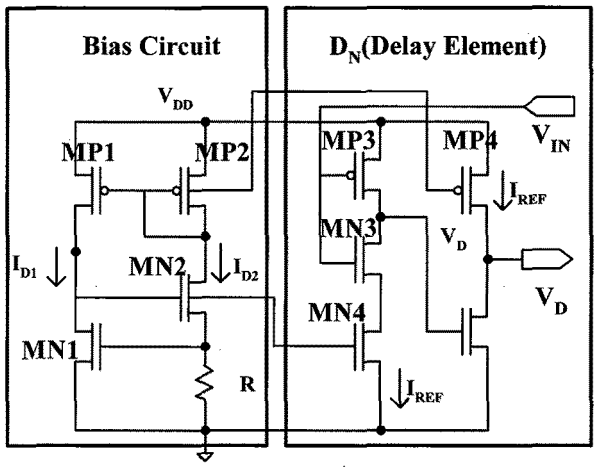


Fig. 7. Analog delay element.

In Fig. 7, the current I_{D1} and I_{D2} are expressed as follows:

$$I_{D1} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS1} - V_{TN})^2 \quad (3)$$

$$I_{D2} = \frac{V_{GS1}}{R} \quad (4)$$

where μ is the effective mobility, C_{OX} is the gate capacitance, V_{GS} is the gate-source voltage and V_{TN} is the threshold voltage of NMOS. When the channel width of MN1 is larger than the channel length of MN1 eq. (1) and eq. (2) can be re-expressed as follows:

$$I_{D1} = I_{D2} = \frac{V_{TN}}{R} + \frac{1}{R}\frac{1}{\mu C_{OX}}\frac{L}{W}(2I_{D1}) \cong \frac{V_{TN}}{R} \quad (5)$$

From eq. (5) the bias currents I_{D1} and I_{D2} are approximately dependent on only the threshold voltage of NMOS. The reference current, I_{REF}, is linearly dependent I_{D1} and I_{D2} and the delay time can be controlled by adjusting the reference current.

Fig. 8 shows the block diagram of the TDC circuit using the analog delay element. The bias circuit of Fig. 7 is added to control the delay time.

Fig. 9 shows the change of the rising time and falling time in the analog delay element when the channel width is varied from -10% to +10% compared to the channel width in layout condition. Fig. 10 shows the delay time and Fig. 11 shows the error rate with the channel width change. When the channel width is varied from -10% to +10%, the error of the delay time is about from -0.2% to +1.8%. When the analog delay element is used the error can be reduced compared to the digital delay element.

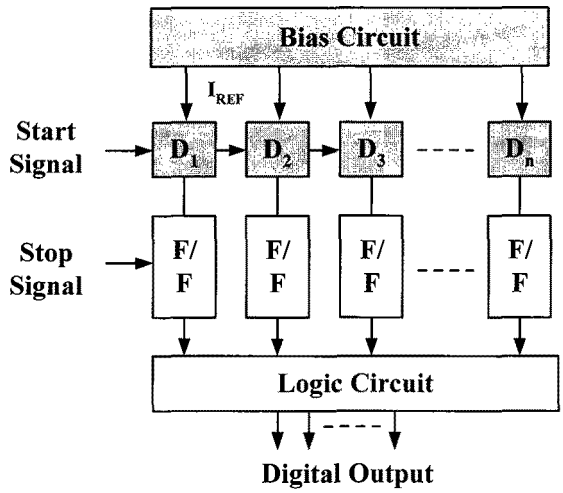


Fig. 8. Block diagram of the TDC circuit using the current source.

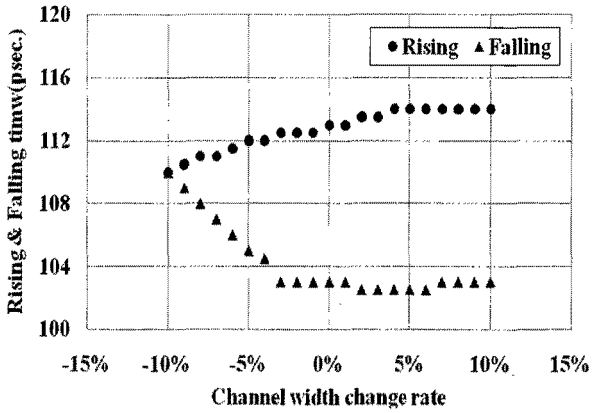


Fig. 9. Rise time and fall time with the width change.

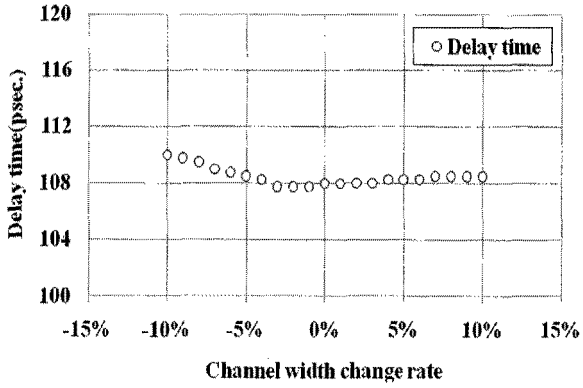


Fig. 10. Delay time with the width change rate.

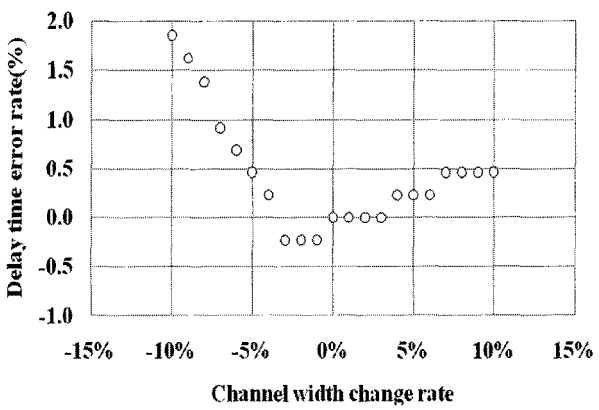


Fig. 11. Delay time error rate with the width change.

IV. CONCLUSIONS

The characteristics of the analog and digital delay elements are analyzed with the channel width variation. The delay elements were designed by 0.5μm CMOS process and simulation carried out with HSPICE. When the channel width is varied from -10% to +10%, the change of the delay time is about from -3.5% to 2.9% in digital delay element. However, in case of using the analog delay element the change of the delay time is about from -0.2% to +1.8%. The analog delay element shows smaller delay time fluctuation when the channel width of CMOS FET is varied between +10% and -10% than the digital delay element in the circuit simulation result. This small delay time fluctuation in TDC increases the process reliability of the converter.

REFERENCES

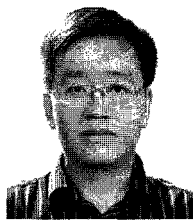
[1] R. cicalese, A. Alosio, P. Branchini, R. Giordano, V. Izzo and S. Loffredo, "Implementation of High-Resolution Time-to-Digital Converters on two different FPGA devices," WSPC-Proceedings, pp. 1-5, 2007.

[2] Jian Song, Qi An and Shubin Liu, "A high-resolution Time-to-Digital Converter Implemented in field programmable gate array," IEEE Trans. Instrum. Meas., vol. 53, no. 1, Feb. 2006.

[3] Volodymyr Kratyuk, Pavan Kumar Hanumolu, Keren Ok, Kartikeya Mayaram and Un-Ku Moon, "A Digital PLL with a Stochastic Time-to-Digital Converter," 2006 Symposium on VLSI Circuits and Design of Technical Papers, IEEE Symposium on VLSI Circuits and Design, 2006.

[4] Poki Chen and Shen-Iuan Liu, "A Cyclic Time-to-Digital Converter With Deep Sub-nanosecond Resolution," IEEE 1999 Custom Integrated Circuits Conference pp. 605-608, 1999.

[5] Neil Weste and Kamran Eshraghian, "*Principles of CMOS VLSI Design-A Systems Perspective*," Weste Eshraghian, 1985.



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