Low-temperature polycrystalline silicon level shifter using capacitive coupling for low-power operation

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Abstract

A new level shifter using low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs) for low-power applications is proposed. The proposed level shifter uses a capacitive-coupling effect and can reduce the power consumption owing to its no-short-circuit current. Its power saving over the conventional level shifter is 72% for a 3.3 V input and a 10 V output.

Keywords: low power, level shifter, capacitive coupling

1. Introduction

The markets for liquid crystal display (LCD) panels using the low-temperature polycrystalline silicon (LTPS) technology are increasing, and the LTPS technology is expected to become a dominant display technology in the small-medium display market this year [1]. The development of a system-on-panel (SOP) display with monolithically integrated driving circuits has been advancing in recent years in small displays because it has several advantages, such as high resolution, high luminance images, narrow picture frames, low power consumption, and an extremely reliable electrical connection [2]. The most important feature of SOP displays, however, is their low power consumption for mobile applications. The most effective way to reduce the power consumption is to run the integrated circuits on the panel at a low voltage range. LCD displays, however, require a relatively high voltage to drive liquid crystal. Thus, a level shifter that converts a low-voltage signal to a high-voltage one is essentially necessary, and it should exhibit low-power operation for mobile applications. The level shifters that have been integrated on the panel have been reported to be utilizing the LTPS technology [3-5], but such level shifters use a 0~5 V input signal or a redundant voltage source on the panel.

In this paper, a new low-power level shifter with a 0~3.3 V input signal and without a redundant voltage source on the panel for mobile applications, employing the capacitive-coupling effect, is presented.

2. Proposed Level Shifter

Fig. 1 shows a conventional level shifter consisting of a differential amplifier and buffers. The differential amplifier has complementary low-voltage inputs (CLK and CLKB) and a high-voltage output (Q2). It exhibits a classic complementary output stage with independent control of the gate voltages of the n- and p-channel thin-film transistor (TFT) devices N2 and P2 [6]. As both the gate and drain of P1 are connected, this forces P1 to operate in either the saturation or cut-off region. When CLK assumes a high state, such as 3.3 V, N1 is turned on, and the voltage of

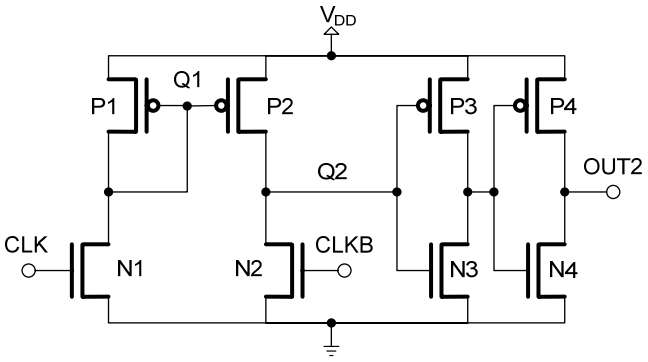

Fig. 1. Conventional level shifter.

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node Q1 is pulled down to GND. Then P1 operates at the saturation region and static current flows from VDD to ground through P1 and N1, which increases the power consumption of the level shifter. Thus, it is necessary to reduce the dissipated power of the level shifter for battery-powered applications.

Fig. 2 shows the proposed level shifter circuit, which can solve the power consumption problem of the conventional one. The proposed level shifter is composed of two coupling capacitors, three diode-connected transistors, two switches, and buffers. Transistor N4 pulls down the voltage of CLK whereas P1 pulls up the voltage of node Q3 to the voltage of node Q1. N4 has low-voltage logic inputs (CLK and CLKB) whereas P1 has high-voltage nodes (Q1 and Q2). Nodes Q1 and Q2 are driven by low-voltage logic inputs through two coupling capacitors. Initially, when CLK is low (0 V) and hence CLKB is high (3.3 V), the voltage of node Q1 becomes VDD- V_{TN} due to a diode-connected transistor (N1), where V_{TN} is the threshold voltage of the n-channel TFT and is generally smaller than 3.3 V. When CLK is high (3.3 V) and CLKB is low (0 V), node Q2 is charged to VDD-2 V_{TN} by diode-connected transistors (N2 and N3). When CLK changes from high (3.3 V) to low (0 V), node Q2 is pushed up to VDD-2 V_{TN} +3.3V by the capacitor C2, and node Q1 becomes VDD- V_{TN}. Then N4 is turned on and P1 is turned off because the voltage of node Q2 is higher than the voltage of node Q1. Thus, the voltage of node Q3 is pulled down to 0 V. There is no short-circuit current during the level-shifting operation because all the TFTs are connected to coupling capacitors. When CLK changes from low (0 V) to high (3.3 V), node Q1 is pushed up to VDD- V_{TN} +3.3V by the capacitor C1, and node Q2 becomes VDD-2 V_{TN}. Then N4 is turned off and P1 is turned on because the voltage of node Q1 is higher than the voltage of node Q2. Thus, the voltage of node Q3 goes to VDD- V_{TN} +3.3V, and the proposed level shifter successfully generates a level-up shifter signal because VDD- V_{TN} +3.3V is higher than VDD. Fig. 3 shows the simulation results of the conventional and proposed level shifters with an operation frequency of 50 kHz. The simulation conditions are as follows: CLK and CLKB have a low-voltage swing (0~3.3 V), and the threshold voltages of the n- and p-channel TFTs, V_{TN} and V_{TP}, were 1.5 and -1.5 V, respectively. The mobilities of the n- and p-channel TFTs were 60 and 50 cm^2/Vs, respectively. It was confirmed that the proposed level shifter successfully shifts up the signal level, and that the delay time of the proposed level shifter is comparable to that of the conventional level shifter, as shown in Fig. 3, which shows the simulated currents of the conventional and proposed level shifters. A stationary current flows from VDD to ground through both P1 and N1 when CLK is high in the conventional circuit, but there is no stationary current between VDD and GND in the proposed level shifter. In the simulation results, the power consumptions of the proposed and conventional level shifters are 29 and 86 μW, respectively. The power consumption of the proposed level shifter can be reduced by about 66%.

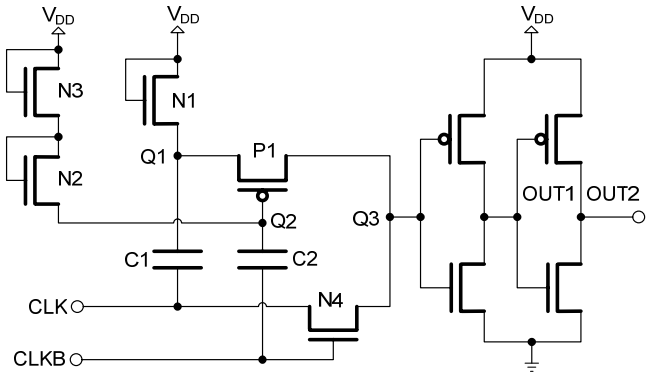

Fig. 2. Proposed level shifter.

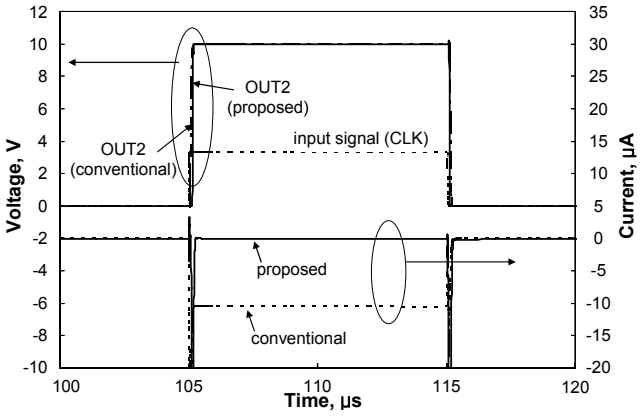

Fig. 3. Simulated waveforms of the level shifters.

3. Experiment Results

The conventional and proposed level shifters with the LTPS process were fabricated using the excimer laser-annealing method. V_{TN} and V_{TP} were 1.2 and -2.9 V, respectively. The mobilities of the fabricated n- and p-channel TFTs were 50.6 and 47.6 cm^2/Vs, respectively. The target

V_{TN} and V_{TP} were 1.5 and -1.5 V, respectively. V_{TP}, however, largely deviated from the target voltage due to the grain boundaries of the poly-Si film and the process variations. Fig. 4 shows the measured output waveforms of the conventional and proposed level shifters. Both level shifters successfully converted the 3.3 V input to a 10 V output. Fig. 4 shows that the delay time from the rising edge of the CLK input to the rising edge of node OUT2 of the proposed level shifter was about 10 μs. The proposed level shifter was simulated using the measured device parameters. Table 1 shows how the delay time increased in accordance with V_{TP}. The long delay time of the proposed level shifter was caused by the high absolute value of V_{TP}. The delay time of the proposed level shifter can be decreased by tuning V_{TP}. The power consumption of the conventional and proposed level shifters are summarized in Table 2, which shows that the power consumption of the proposed level shifter can be reduced by 72% compared with that of the conventional one, for a 3.3 V input and a 10 V output.

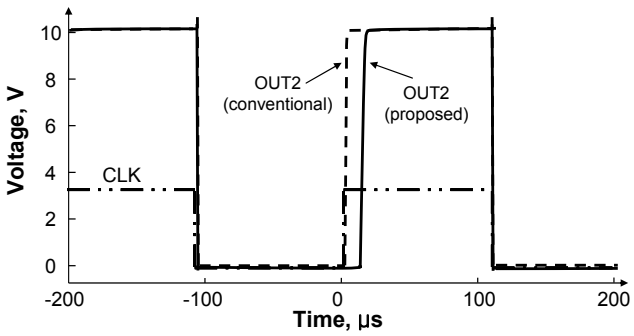

Fig. 4. Measured output waveforms of the level shifters.

Table 1. Simulation results of the delay time with varying V_{TP}.

V_{TP}	−1.0 V	−1.5 V	−2.0 V	−2.5 V	−3.0 V
Delay time	0.4 μs	0.8 μs	1.3 μs	2.6 μs	9.0 μs

Table 2. Power consumptions of the conventional and proposed level shifters.

	Conventional	Proposed
Simulation	86 μW	29 μW
Measurement	97 μW	27 μW

4. Conclusions

A new low-power LTPS level shifter using the capacitive-coupling technique is proposed. The low-power consumption of the proposed level shifter was verified by the fabrication results. It is believed that the proposed level shifter can be applied to mobile applications and to an SOP display with low-power operation.

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