

Current-Type Nine-Switch Inverters

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Abstract

In this paper two dual output current-type inverters are proposed. These inverters have been called a current source nine-switch inverter and a current-type z-source nine-switch inverter by the authors. The proposed inverters have two independent current source outputs. Compared to two independent current source inverters, the proposed converters are implemented with fewer semiconductor switches. Space vector modulation (SVM) is proposed for these converters. Simulation results show the validity and performance of the proposed inverters.

Key Words: Current Source Inverter, Nine-Switch Inverter, Multi-output inverter, Space vector modulation, Z-Source Inverter

I. INTRODUCTION

Current source inverters (CSIs) are used in many high and medium power industrial applications [1], [2]. An AC/AC conversion system based on a CSI is shown in Fig. 1. The CSI has the advantage of indirect output short-circuit protection. In addition, it has a low output harmonic because of its output capacitors.

In many industrial applications, there is a need to power two AC loads at the same time. The conventional method of controlling two AC loads is to use two separate inverters. This method increases both the cost and volume. In [3], a nine-switch inverter (NSI) was presented for this purpose (Fig. 2). This inverter was used as an AC/AC converter in [4], [5] where two back to back inverters were used conventionally. The nine-switch inverter has three less switches than dual inverters. While the inverter in [3] is a voltage source inverter (VSI), this paper presents a current source inverter with two AC outputs (Fig. 3). The proposed inverter is based on a voltage source nine-switch inverter (VS-NSI). In addition, a space vector modulation (SVM) algorithm has been presented for the proposed inverter. The SVM is based on conventional CSI [6], [7] and nine-switch voltage-source inverter [8] space vector modulations.

The input DC current of the proposed inverter is shared between two outputs. Consequently the maximum output currents for the proposed inverter are less than the single output of a conventional CSI. To remedy this limitation, a current-type z-source nine-switch inverter (CTZS-NSI) is also proposed in this paper (Fig. 4). This converter is composed of a current-source nine-switch inverter and a current-type z-source network. The current-type z-source network acts as a current DC/DC boost converter. The z-source network was

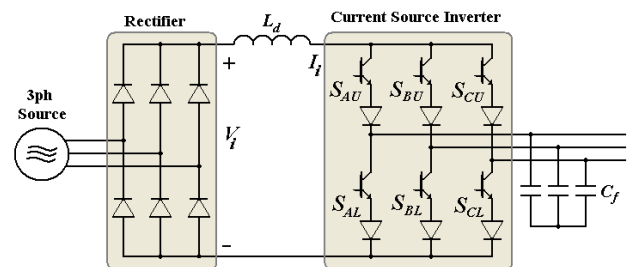


Fig. 1. AC/AC conversion system based on CSI.

proposed as a voltage boost converter in [9], for the first time. Then a current-type z-source network was proposed in [10], as the front stage of a single output CSI. Single output z-source CSIs are developed and analyzed in [11] and [12]. A modified SVM has been proposed for the nine-switch z-source current-type inverter in this paper.

Section II of this paper introduces a current source nine-switch inverter. A SVM method for the CS-NSI is proposed in section III. Section IV presents a current-type z-source nine-switch inverter. In section V, the proposed converters with front-end rectifiers are discussed. Finally, simulation results are presented, to verify the performance of the proposed converter.

II. CURRENT SOURCE NINE-SWITCH INVERTER

A conventional CSI (Fig. 1) has nine switching vectors. Six active vectors and three zero vectors. Table I shows the ON switches in each vector. In all of the vectors an upper switch and a lower switch are ON. In this manner, there is always a path for the input DC current. In the active vectors, the ON switches are from different legs. Thus the input DC current passes through the load. However in the zero vectors, both of the ON switches are from the same leg. It is obvious that the input DC current does not pass across the load in the zero

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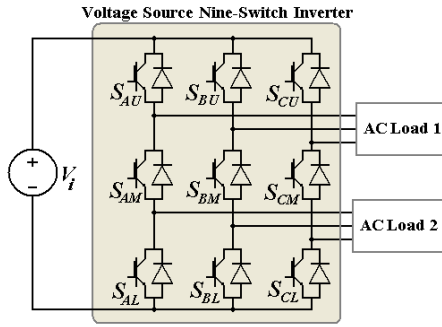


Fig. 2. Voltage source nine-switch inverter (VS-NSI) [3].

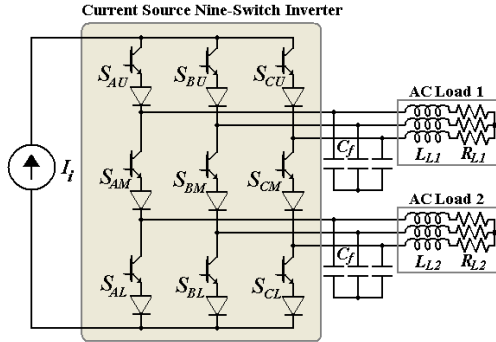


Fig. 3. Proposed current source nine-switch inverter (CS-NSI).

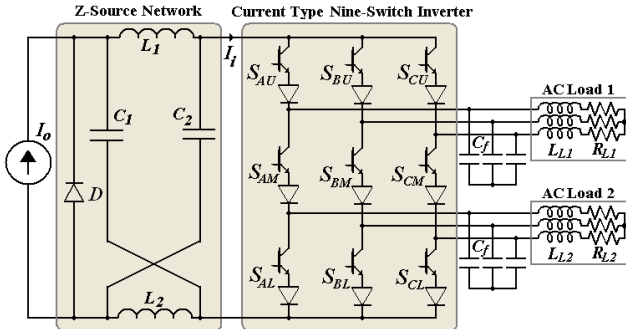


Fig. 4. Proposed current-type z-source nine-switch inverter (CTZS-NSI).

vectors. Thus this current can be used for another load. This is the main idea for the CS-NSI (Fig. 3). The CS-NSI can be considered as two separate conventional CSIs with three common switches. When an inverter is in an active vector, another inverter must be in a zero vector.

For implementation of the above idea, a list of vectors has been created for the CS-NSI, as shown in Table II. The numbers 0 to 5 indicate the state of the switches in each leg. Table III explains the switch states 0 to 5, where, J is A, B or C and U, M and L are the upper, mid and lower switches. The switching vectors are divided into four groups: upper active vectors, lower active vectors, zero vectors and an open-circuit vector. In the upper active vectors (I_1 - I_6), the upper output (the upper inverter) is in the active state, and the lower output is in the zero state. There is an inverse logic in the lower active vectors (I_7 - I_{12}). In the zero vectors (I_{13} - I_{15}), both outputs are in the zero state. The open-circuit vector (I_{16}) is not used for the CS-NSI. Vector I_{16} is used in the CTZS-NSI as described

in section IV.

TABLE I
THE SWITCHING VECTOR OF THE CONVENTIONAL CSI (FIG. 1)

Vector	ON Switches	Type
1	S_{AU}, S_{CL}	Active
2	S_{BU}, S_{CL}	
3	S_{AL}, S_{BU}	
4	S_{AL}, S_{CU}	
5	S_{BL}, S_{CU}	Zero
6	S_{AU}, S_{BL}	
7	S_{AU}, S_{AL}	
8	S_{BU}, S_{BL}	Zero
9	S_{CU}, S_{CL}	

TABLE II
THE SWITCHING VECTORS OF THE CURRENT-TYPE NINE-SWITCH INVERTERS (FIG. 3)

Vector	Leg A	Leg B	Leg C	Type
1	2	0	1	Upper Active
2	0	2	1	
3	1	2	0	
4	1	0	2	
5	0	1	2	
6	2	1	0	
7	4	0	3	Lower Active
8	0	4	3	
9	3	4	0	
10	3	0	4	
11	0	3	4	
12	4	3	0	
13	5	0	0	Zero
14	0	5	0	
15	0	0	5	
16	0	0	0	Open-Circuit

TABLE III
VECTOR SWITCH STATE IN CURRENT-TYPE NINE-SWITCH INVERTERS (TABLE II)

	S_{JU}	S_{JM}	S_{JL}
0	OFF	OFF	OFF
1	OFF	ON	ON
2	ON	OFF	OFF
3	OFF	OFF	ON
4	ON	ON	OFF
5	ON	ON	ON

III. SVM METHOD FOR A CURRENT-SOURCE NINE-SWITCH INVERTER

Fig. 5 shows a proposed sequence of switching vectors for implementing the SVM method for a current source nine-switch inverter. The sequence includes the upper active vectors, the lower active vectors and the zero vectors in each switching cycle.

I_Z	I_{AU}	I_{AU}	I_Z	I_{AL}	I_{AL}	I_Z	I_{AU}	I_{AU}	I_Z	I_{AL}	I_{AL}	I_Z
$\frac{T_o}{4}$	T_1	T_2	$\frac{T_o}{2}$	T_3	T_4	$\frac{T_o}{2}$	T_2	T_1	$\frac{T_o}{2}$	T_4	T_3	$\frac{T_o}{4}$

Fig. 5. The switching vector sequence of SVM for CS-NSI.

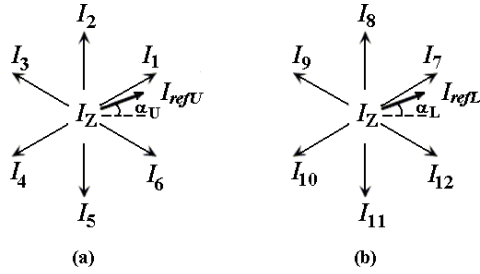


Fig. 6. Space vector diagrams for CS-NSI: a) Upper output, b) Lower output.

To determine the correct active vectors, two space vector diagrams are proposed as shown in Fig. 6. Diagrams (a) and (b) are used to determine the upper and lower active vectors respectively. The SVM active vectors are determined with regard to the location of the upper reference signal (\bar{I}_{refU}) in diagram (a) and the lower reference signal (\bar{I}_{refL}) in diagram (b). The reference signals for the upper and lower outputs are defined as:

$$\bar{I}_{refU} = I_{refU} \angle \alpha_U \quad (1)$$

$$\bar{I}_{refL} = I_{refL} \angle \alpha_L \quad (2)$$

where

$$\alpha_U = 2\pi f_U t + \phi_U \quad (3)$$

$$\alpha_L = 2\pi f_L t + \phi_L \quad (4)$$

where, f_U and f_L are the frequencies, and ϕ_U and ϕ_L are the phases. All of the zero vectors I_{13} , I_{14} and I_{15} can be used for the zero states. The switching time intervals of the vectors are calculated as:

$$T_1 = \frac{\sqrt{3}}{2} m_U T \sin\left(\frac{\pi}{3} - \alpha_U\right) \quad (5)$$

$$T_2 = \frac{\sqrt{3}}{2} m_U T \sin(\alpha_U) \quad (6)$$

$$T_3 = \frac{\sqrt{3}}{2} m_L T \sin\left(\frac{\pi}{3} - \alpha_L\right) \quad (7)$$

$$T_4 = \frac{\sqrt{3}}{2} m_L T \sin(\alpha_L) \quad (8)$$

$$T_o = T - T_1 - T_2 - T_3 - T_4 \quad (9)$$

where, T_1 and T_2 are the time intervals of the upper active vectors, T_3 and T_4 are the time intervals of the lower active vectors, T_o is the time interval of the zero vectors and T is the switching period. m_U and m_L are the upper and lower modulation indices respectively and they are defined by:

$$m_U = \frac{2\sqrt{2} I_{refU}}{\sqrt{3} I_i} \quad (10)$$

$$m_L = \frac{2\sqrt{2} I_{refL}}{\sqrt{3} I_i} \quad (11)$$

I_Z	I_{OC}	I_{AU}	I_{AU}	I_{AL}	I_{AL}	I_{OC}	I_Z	I_{OC}	I_{AU}	I_{AU}	I_{AL}	I_{AL}	I_{OC}	I_Z
$\frac{T_o}{2}$	T_2	T_1	T_4	T_3	$\frac{T_o}{2}$	T_3	$\frac{T_o}{2}$	T_1	T_2	T_3	T_4	$\frac{T_o}{2}$	$\frac{T_o}{2}$	$\frac{T_o}{2}$

Fig. 7. Space vector modulation (SVM) of CTZS-NSI.

The sum of the active vector time intervals must be less than or equal to T . Thus the following constraint must be satisfied:

$$(m_U + m_L) \leq \frac{1}{\sqrt{3}} \quad (12)$$

IV. CURRENT-TYPE Z-SOURCE NINE-SWITCH INVERTER

Considering (12), it is obvious that the output currents from a nine-switch inverter are lower than those from a conventional CSI of the same power. As a solution, a current-type z-source nine-switch inverter (CTZS-NSI) is proposed. A current-type z-source inverter was presented in [10] and [11], previously. However, we have modified the current type ZSI to accommodate two loads at the same time by using a nine-switch topology.

Fig. 4 shows the proposed CTZS-NSI. This converter is composed of a current-type z-source network and a CS-NSI. The current-type z-source network includes two inductors (L_1 & L_2), two capacitors (C_1 & C_2) and one diode (D), as shown in Fig. 4. If a bidirectional power flow is required, diode D can be replaced by a voltage-bidirectional two-quadrant switch (such as an IGBT in series with a diode).

The current-type z-source network causes the input DC current of a CS-NSI (I_i), to be larger than the DC terminal current (I_o). Therefore the z-source network operates as a current boost converter. This DC/DC converter has two operation modes. In the first mode, the output of the converter should be open-circuit. Consequently the diode D turns ON (If a switch is used instead of a diode D , it should be forced ON). This mode is known as the open-circuit mode. The open-circuit mode can be implemented by turning OFF all the switches in the CS-NSI. Vector I_{16} from Table II can create an open-circuit mode. The second mode is known as the non-open-circuit mode. In this mode, there is a path for the output current of the z-source converter and the diode D turns OFF. This mode occurs if the CS-NSI is in one of the vector I_1 - I_{15} states. As described in [10], the relationship between the output current of the z-source network (I_i) and the input DC current (I_o) is defined by:

$$I_i = B I_o \quad (13)$$

where, B is known as the boost factor and is given by following equation:

$$B = \frac{1}{1 - 2 \left(T_{OC}/T \right)} \quad (14)$$

where T_{OC} is time interval of the open-circuit vector (I_{16}).

The proposed SVM for a CS-NSI can be modified for a CTZS-NSI (Fig. 7). As shown in Fig. 7, the two open-circuit vectors (I_{OC}) are inserted at both sides of the zero vectors (I_Z). The active vectors are determined via the diagrams in Fig. 6. T_1 , T_2 , T_3 , T_4 and T_o are calculated by (5-9) and T_{OC} is determined by (14).

V. CURRENT-TYPE NINE-SWITCH INVERTERS WITH A FRONT-END RECTIFIER

A voltage source such as a front end rectifier (Fig. 1) in series with an inductance is used as a current source. In this case, the CSI acts as a voltage boost converter [10]:

$$v_{ac} = \frac{4}{3\sqrt{3}} \frac{V_i}{m \cos \varphi} \quad (15)$$

where V_i is the DC source voltage, v_{ac} is the output peak phase voltage and $\cos \varphi$ is the power factor of the load. According to the above equation, there is a voltage limitation for the output such that:

$$v_{ac-\min} = \frac{2}{3} \frac{V_i}{\cos \varphi}. \quad (16)$$

To remedy this problem a variable voltage source such as a controlled rectifier is used for a low voltage application.

Now, we discuss the proposed converter with a front-end rectifier. In the case of the proposed CS-NSI, we have:

$$i_{acU} = \frac{\sqrt{3}}{2} m_U I_i \quad (17)$$

$$i_{acL} = \frac{\sqrt{3}}{2} m_L I_i \quad (18)$$

where i_{acU} and i_{acL} are the peak current of the upper and lower outputs, respectively. Since the input and output powers of the converter are equal, it can be written:

$$P_{in} = P_{out} \quad (19)$$

$$V_i I_i = \frac{3}{2} (i_{acU} v_{acU} \cos \varphi_U + i_{acL} v_{acL} \cos \varphi_L) \quad (20)$$

$$V_i = \frac{3\sqrt{3}}{4} (m_U v_{acU} \cos \varphi_U + m_L v_{acL} \cos \varphi_L). \quad (21)$$

On other hand:

$$v_{acU} = z_{LoadU} i_{acU} \quad (22)$$

$$v_{acL} = z_{LoadL} i_{acL}. \quad (23)$$

Considering (17), (18), (22) and (23), we have:

$$\frac{v_{acU}}{v_{acL}} = \frac{m_U z_{LoadU}}{m_L z_{LoadL}}. \quad (24)$$

According to (21) and (24), the peak phase voltage of the outputs can be calculated by:

$$v_{acU} = \frac{4}{3\sqrt{3}} \frac{m_U z_{LoadU}}{m_U^2 z_{LoadU} \cos \varphi_U + m_L^2 z_{LoadL} \cos \varphi_L} V_i \quad (25)$$

$$v_{acL} = \frac{4}{3\sqrt{3}} \frac{m_L z_{LoadL}}{m_U^2 z_{LoadU} \cos \varphi_U + m_L^2 z_{LoadL} \cos \varphi_L} V_i. \quad (26)$$

As can be seen from the above equations, the output voltage outputs are not independent. However modulation indices can be calculated for desirable output voltages by:

$$m_U = \frac{4}{3\sqrt{3}} \frac{1}{\cos \varphi_U + \left(\frac{v_{acL}}{v_{acU}}\right)^2 \left(\frac{z_{LoadU}}{z_{LoadL}}\right) \cos \varphi_L} \frac{V_i}{v_{acU}} \quad (27)$$

$$m_L = \frac{4}{3\sqrt{3}} \frac{1}{\left(\frac{v_{acU}}{v_{acL}}\right)^2 \left(\frac{z_{LoadL}}{z_{LoadU}}\right) \cos \varphi_U + \cos \varphi_L} \frac{V_i}{v_{acL}}. \quad (28)$$

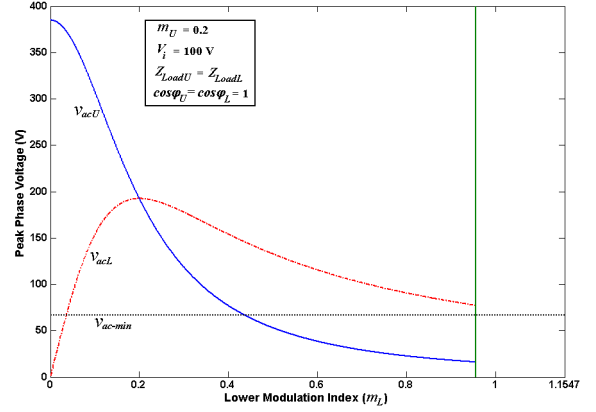


Fig. 8. Typical curve of CS-NSI output voltages for various modulation indices.

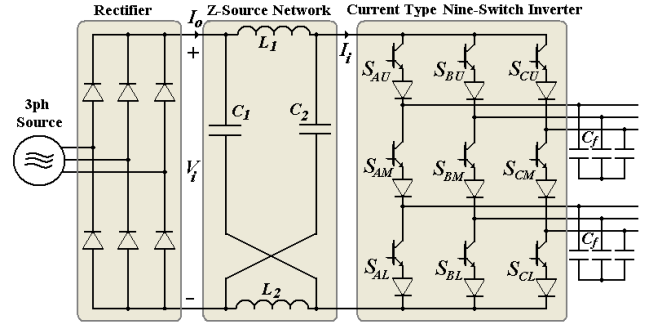


Fig. 9. CTZS-NSI with front-end rectifier.

Unlike a conventional CSI, the proposed CS-NSI can function as a voltage buck-boost converter. Both outputs of the CS-NSI can be used as a voltage boost converter or one of them can be used as a boost converter while the other is used as a buck converter. However both can not be used as buck converters at the same time. Fig. 8 shows a typical curve for CS-NSI output voltages for various modulation indices. The dotted line is related to the minimum voltage for a conventional CSI in similar conditions.

In the case of a CTZS-NSI, the inductor and diode D (in Fig. 4) can be removed when a front-end rectifier is used (Fig. 9). Equations (20) and (21) can be rewritten for the CTZS-NSI as:

$$\frac{V_i I_i}{B} = \frac{3}{2} (i_{acU} v_{acU} \cos \varphi_U + i_{acL} v_{acL} \cos \varphi_L) \quad (29)$$

$$\frac{V_i}{B} = \frac{3\sqrt{3}}{4} (m_U v_{acU} \cos \varphi_U + m_L v_{acL} \cos \varphi_L). \quad (30)$$

Therefore we have,

$$v_{acU} = \frac{4}{3\sqrt{3}} \frac{m_U z_{LoadU}}{m_U^2 z_{LoadU} \cos \varphi_U + m_L^2 z_{LoadL} \cos \varphi_L} \frac{V_i}{B} \quad (31)$$

$$v_{acL} = \frac{4}{3\sqrt{3}} \frac{m_L z_{LoadL}}{m_U^2 z_{LoadU} \cos \varphi_U + m_L^2 z_{LoadL} \cos \varphi_L} \frac{V_i}{B}. \quad (32)$$

In a CTZS-NSI, the low output voltage for both outputs can be generated using B . B can also be used for constant current control of the dc link current. Consequently the output voltages can be controlled independently.

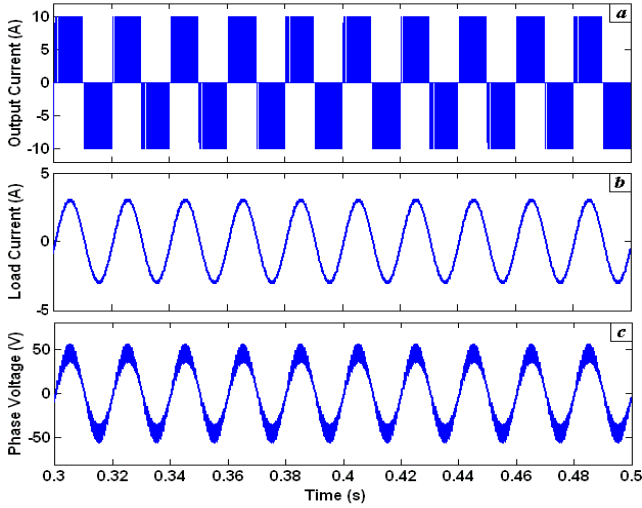


Fig. 10. Upper output of CS-NSI based on ideal source: a) Output current before filter capacitor C_f . b) Load current. c) Phase voltage.

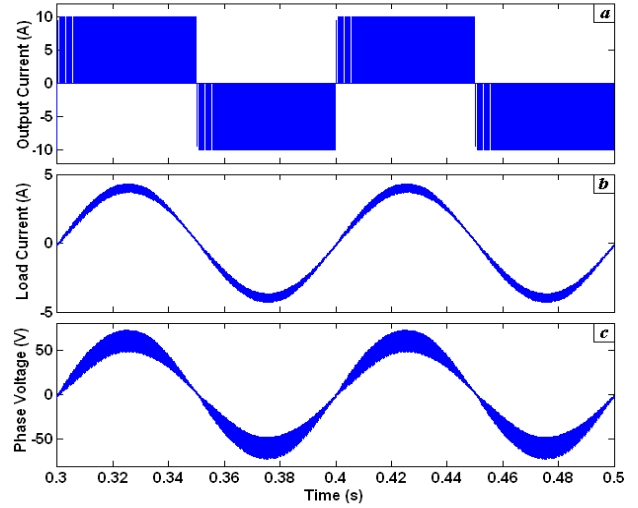


Fig. 11. Lower output of CS-NSI based on ideal source: a) Output current before filter capacitor C_f . b) Load current. c) Phase voltage.

VI. SIMULATION VERIFICATION

The simulation results of proposed converters are discussed in this section. This section has three parts: A) a simulation based on an ideal input current source B) a simulation based on a front-end rectifier C) Calculation and comparison of the efficiency and the total harmonic distortion (THD). Similar RL loads are connected to the outputs of the inverters. Table IV shows the simulation parameters.

TABLE IV
PARAMETERS OF SIMULATION

Parameter	Sim. A	Sim. B
Switching Frequency (f_S)	2 kHz	6.3 kHz
Reference Upper Output	$I_{refU}=2$ A	$v_{acU}=400$ V
Reference Lower Output	$I_{refL}=3$ A	$v_{acL}=300$ V
Upper Load Frequency (f_U)	50 Hz	25 Hz
Lower Load Frequency (f_L)	10 Hz	50 Hz
Filter Capacitor (C_f)	45 μ F	45 μ F
R_{L1} & R_{L2} (Loads)	15 Ω	50 Ω
L_{L1} & L_{L2} (Loads)	2 mH	50 mH
$C1$ & $C2$ (Z-Source Net.)	150 μ F	2 μ F
$L1$ & $L2$ (Z-Source Net.)	40 mH	15 mH
Resistance of $L1$ & $L2$	-	0.1 Ω
DC Link Filter (L_d)(Fig. 1)	-	30 mH
Resistance of L_d	-	0.2 Ω

A. Ideal input current source

First, the CS-NSI was simulated with an input ideal DC current source of 10A. The output currents (before the filter capacitor C_f), load currents and phase voltages are shown in Fig. 10 and Fig. 11 for the upper and lower outputs, respectively. It can be seen that load currents are equal to the reference values in Table IV (2A and 3A). In addition, the signals have the expected frequencies of 50 and 10 Hz.

In the second simulation, a current-type z-source network was added to the CS-NSI. The magnitude of the DC current source is 7A. Considering (14), to boost the input current to

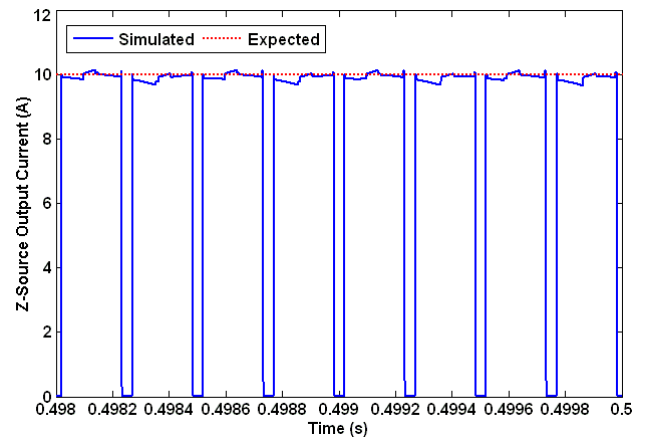


Fig. 12. Z-source output current in CTZS-NSI based on ideal source (I_i in Fig. 4).

10A, T_{OC}/T was set to 0.15. The output current of the z-source network (I_i) is shown in Fig. 12. As expected, the I_i magnitude changes between 0A and 10A. Fig. 13 shows the z-source network inductor current. The current is equal to the expected value of 8.5A. The inductor current is $0.5(I_o + I_i)$, as described in [10]. Fig. 14 and Fig. 15 show the output current, load current and phase voltage of the two outputs.

B. Front-end rectifier

Now, the ideal input current source is replaced with a front-end rectifier connected to the grid (380V-60Hz). The peak phase voltage is used as the reference value (400V and 300V for the upper and lower outputs, respectively).

For the CS-NSI, according to these reference values, the modulation indices were calculated by (27) and (28). The grid voltage, V_i is considered to be 512V in these equations. Fig. 16 and Fig. 17 show the output currents, load currents and phase voltages. It can be seen from the phase voltages that the reference values are generated. Some ripple can be seen in the output currents. This is due to non-ideal current source ripple, as shown in Fig. 18.

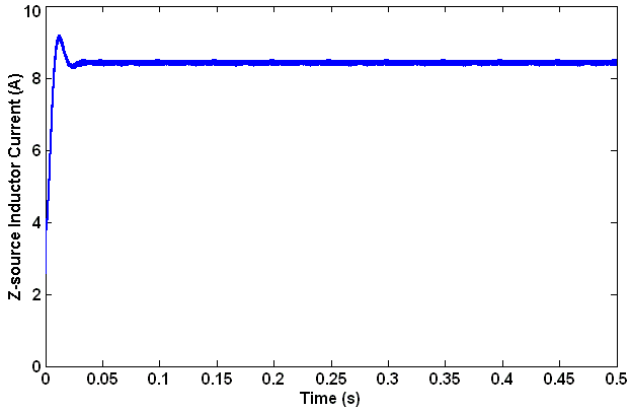


Fig. 13. Z-source inductor current of CTZS-NSI based on ideal source (L_1 current in Fig. 4).

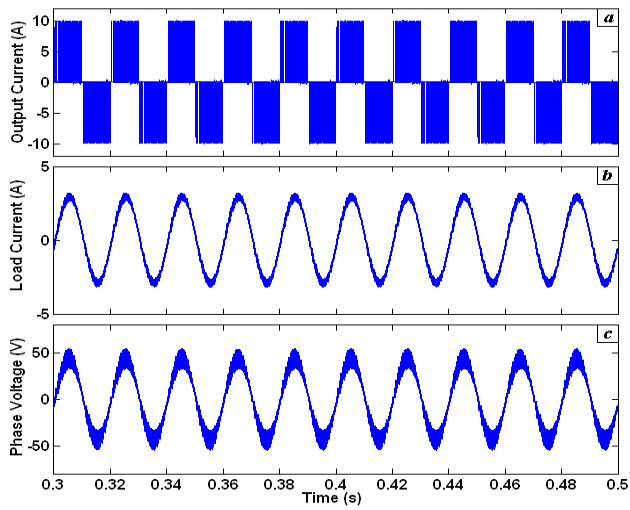


Fig. 14. Upper output of CTZS-NSI based on ideal source: a) Output current before filter capacitor C_f . b) Load current. c) Phase voltage.

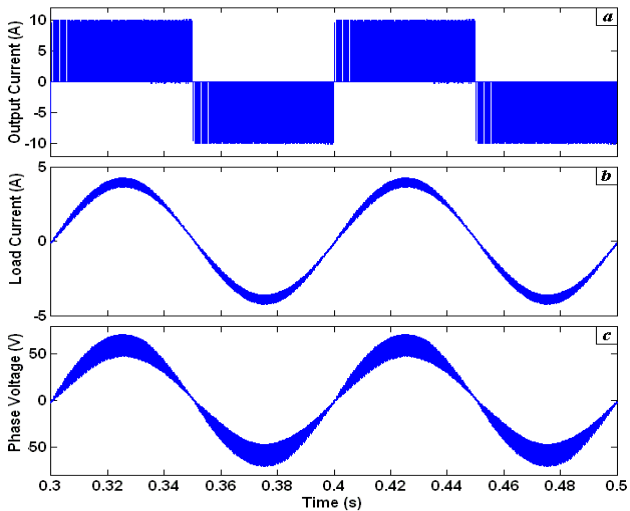


Fig. 15. Lower output of CTZS-NSI based on ideal source: a) Output current before filter capacitor C_f . b) Load current. c) Phase voltage.

For the CTZS-NSI, the topology shown in Fig. 9 has been simulated. The boost factor (B) was selected as 1.43. The modulation indices calculated by (27) and (28) were divided

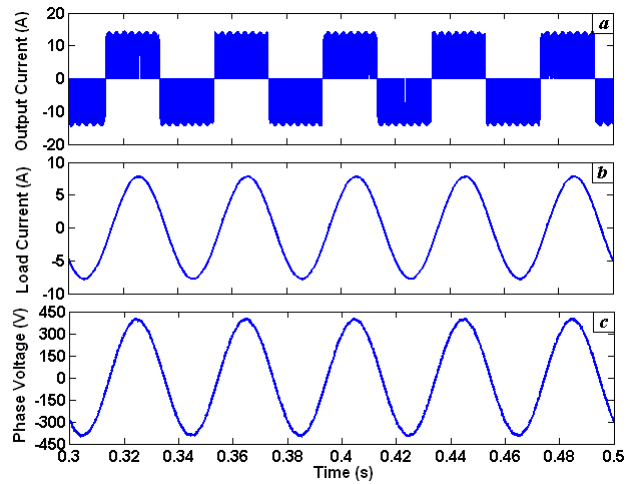


Fig. 16. Upper output of CS-NSI based on front-end rectifier: a) Output current before filter capacitor C_f . b) Load current. c) Phase voltage.

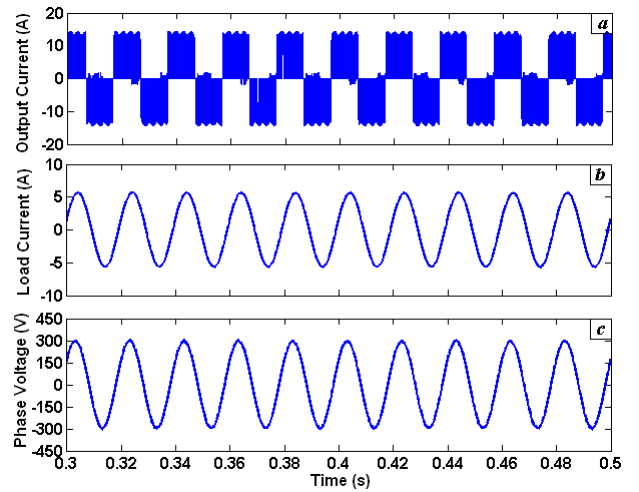


Fig. 17. Lower output of CS-NSI based on front-end rectifier: a) Output current before filter capacitor C_f . b) Load current. c) Phase voltage.

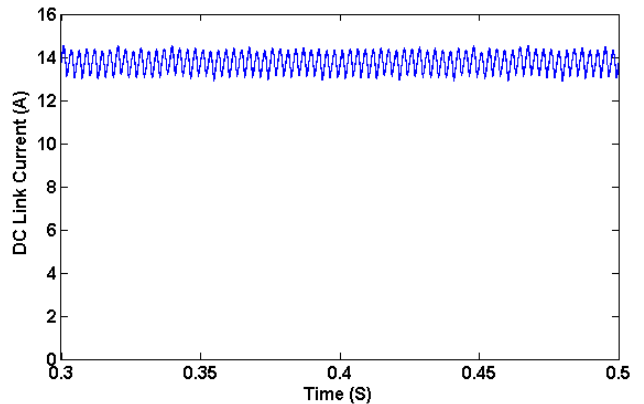


Fig. 18. DC link current of CS-NSI based on front-end rectifier.

by B . The output currents, load currents and phase voltages are shown in Fig. 19 and Fig. 20. The output and input currents of the z-source network are shown in Fig. 21. The magnitude of the z-source output current (I_i) changes between 0A and 20A. The magnitude of the z-source output current

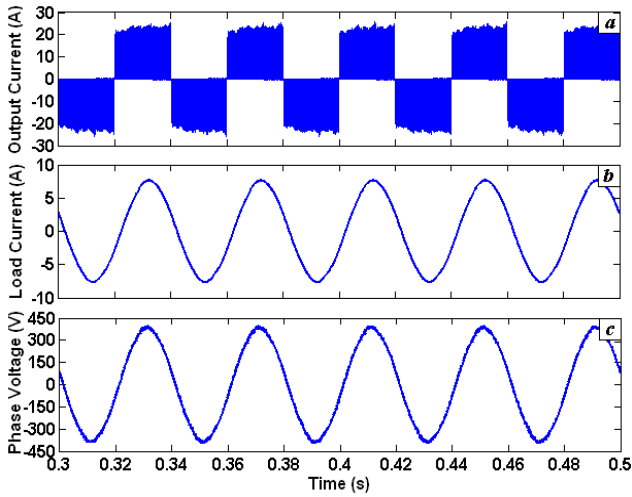


Fig. 19. Upper output of CTZS-NSI based on front-end rectifier: a) Output current before filter capacitor C_f . b) Load current. c) Phase voltage.

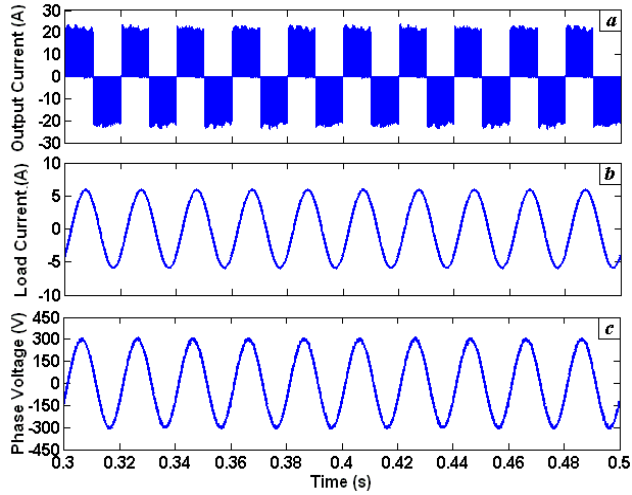


Fig. 20. Lower output of CTZS-NSI based on front-end rectifier: a) Output current before filter capacitor C_f . b) Load current. c) Phase voltage.

(I_o) changes between 14A and 34A. 14A happens during the non-open circuit vectors and is equal to the DC link current in the previous simulation (because the consumed power is the same in both simulations). Consequently a value of 20A in I_i is expectable according to (14). The value of I_o as 34A is related to the open-circuit vectors and is equal to sum of the z-source inductor currents. The z-source inductor current is shown in Fig. 22 which is equal to the expected value of 17A ($0.5I_o + 0.5I_i$).

C. Efficiency

For an efficiency comparison, a CS-NSI with a front-end rectifier is compared with two parallel conventional CSIs with a common front-end rectifier (Fig. 23). The total power loss includes the power losses related to the rectifier, inductor and current source inverters. By using a bridge rectifier module, the dissipation can be calculated versus current from the datasheet. The power loss of the inductor is composed of the core loss and resistive loss. We used Micrometal design software to design the inductor and calculate the power loss [13].

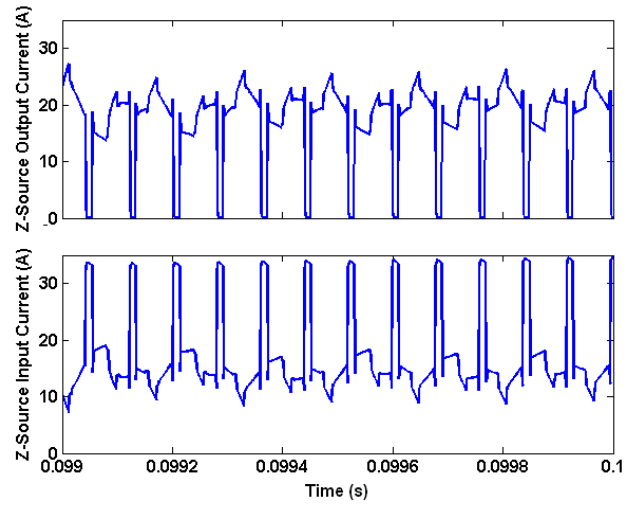


Fig. 21. Output and input currents of z-source network in CTZS-NSI based on front-end rectifier (I_i and I_o in Fig. 9).

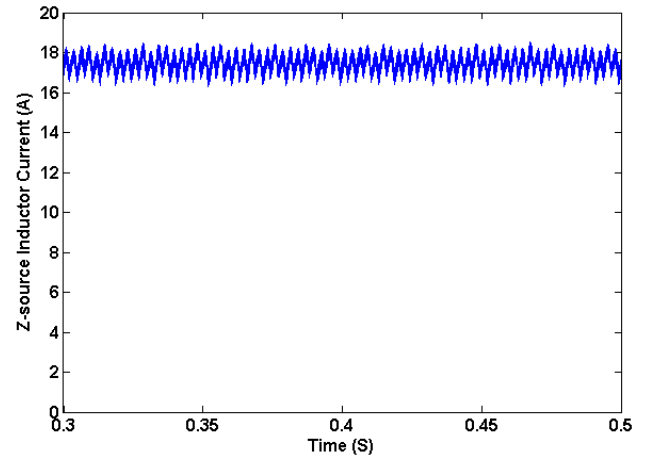


Fig. 22. Z-source inductor current of CTZS-NSI based on front-end rectifier (L_1 current in Fig. 9).

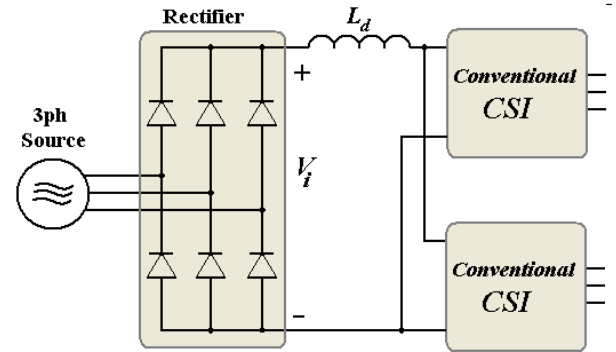


Fig. 23. Conventional CSIs to control two loads.

Semiconductor losses of the inverter include the switching loss and conduction loss. The conduction loss of a conventional CSI can be expressed by [14]:

$$L_{Loss-Con} = 2(V_{ce}I_i + r_{CE}I_i^2 + V_fI_i + r_fI_i^2). \quad (33)$$

In the case of a CS-NSI, since three switches are always

ON, the conduction loss of can be expressed by:

$$P_{Loss-Con} = 3(V_{ce}I_i + r_{CE}I_i^2 + V_fI_i + r_fI_i^2). \quad (34)$$

The switching loss of a conventional CSI can be expressed by [14]:

$$P_{Loss-SW} = f_s \frac{3}{\pi} (E_{ON} + E_{OFF} + E_{rr}) \frac{I_i v_{line}}{I_n V_n} \quad (35)$$

where, f_s is the switching frequency, I_i is the current of the DC link and v_{line} is the peak line voltage of the output. E_{ON} , E_{OFF} and E_{rr} are the wasted energies for turning a switch ON, turning a switch OFF and turning a diode OFF in the current I_n and the voltage V_n that can be obtained from the datasheet.

The switching loss of the CS-NSI depends on the frequency and phase of the outputs because the voltage stress of the middle switches is related to the difference between the line voltages of the two outputs. Minimum loss occurs when both outputs have the same frequency, phase and amplitude (in this case the voltage stress of the middles switches is zero):

$$P_{Loss-SW} = f_s \frac{6}{\pi} (E_{ON} + E_{OFF} + E_{rr}) \frac{I_i v_{line}}{I_n V_n}. \quad (36)$$

Maximum loss occurs when both outputs have the same frequency and amplitude but with a phase difference of 180 degrees:

$$P_{Loss-SW} = f_s \frac{12}{\pi} (E_{ON} + E_{OFF} + E_{rr}) \frac{I_i v_{line}}{I_n V_n}. \quad (37)$$

As an example, two conventional systems and the proposed system have been designed for two 6kW loads with a peak line voltage of 1000V. Table V shows the designed systems. It can be seen that the efficiency is reduced in the proposed system by between 0.9 and 1.6 percent.

TABLE V
PROPOSED AND CONVENTIONAL SYSTEM DESIGNED FOR EFFICIENCY
COMPARISON

Parameter	Conventional System	Proposed System
$v_{line-grid}$	380 V (RMS)	380 V (RMS)
$v_{line-output}$	1000 V (peak)	1000 V (peak)
Load	2*6kW	2*6kW
f_s	6.3 kHz	6.3 kHz
Rectifier	Semikron-SK55D08 800V-45A	Semikron-SK55D08 800V-45A
	$P_{loss} = 60 W$	$P_{loss} = 60W$
L_d	20 mH	20 mH
	$P_{loss} = 120W$	$P_{loss} = 120W$
IGBT	IXYS-IXRH 15N120 1200V-15A	IXYS-IXRH 40N120 1200V-35A
	$P_{loss} = 2 * 84 W$	$P_{loss} = 275-370$
Efficiency	97.1%	95.42%-96.21%

VII. CONCLUSIONS

This paper has presented two dual-output current source inverters, called a current source nine-switch inverter (CS-NSI) and a current-type z-source nine-switch inverter (CTZS-NSI). These inverters are composed of only nine semiconductor

switches. Both inverters can control two ac loads independently. The current-type z-source nine-switch inverter can also boost the input DC current. While a conventional CSI with a diode front-end rectifier acts as a voltage boost converter, one of the outputs of the CS-NSI and both outputs of the CTZS-NSI can act as voltage buck converter in addition to their voltage boost capacity. A SVM method was presented for the proposed inverters. Simulation results show the validity and performance of the proposed inverters and also the proposed space vector modulation methods.

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