# Adaptive Carrier-based PWM for a Four-Switch Three-Phase Inverter under DC-link Voltage Ripple Conditions

**Tuyen D. Nguyen*, Hong-Hee Lee† and Hoang M. Nguyen***

**Abstract –** This paper proposes an adaptive carrier-based pulse width modulation (PWM) method for a four-switch three-phase (4S3P) inverter under dc-link voltage ripple conditions. The proposed method guarantees balanced output currents despite of the existence of the voltage oscillations across two dc-link capacitors. And also, this new approach achieves a linear over-modulation with calculation time reduction. Simulation and experimental results are given to validate the feasibility of the proposed method.

**Keywords:** Adaptive carrier-based PWM, Four-switch inverter, Low cost inverter, Over-modulation

## 1. Introduction

In industrial applications, low cost motor drives are very important and necessary. Power switch reductions in inverters are one of the main investments. The 4S3P inverter, which uses only four switches to produce three phase output voltages, is the suggested topology with a low cost. Besides its low cost advantage, some drawbacks in this topology do exist: output voltages decrements and unbalanced output currents due to variations of voltages across two dc-link capacitors. The modulation techniques for 4S3P inverters have received much consideration from researchers to remove these drawbacks. In [1], a simple method based on the sinusoidal reference signals was proposed. This method did not consider the ripple of two dc-link voltages. The authors of [2] also used the sinusoidal pulse width modulation (SPWM) method by generating two sinusoidal reference signals with a 60 degree phase-shift to control a 4S3P inverter.

Recently, modulation strategies have been developed based on space vectors [3]. Compared with the SPWM method, the space vector PWM (SVPWM) method has been shown to generate less total harmonic distortion in output voltages and currents, less switching loss and a wide linear modulation region. The authors in [4] presented a new space vector modulation strategy based on flux trajectory with minimum motor torque ripple. However, the effects of two unbalanced dc-link voltages to output currents were not considered in [1]-[4]. Some adaptive SVPWM techniques were proposed in [5], [6], and balanced output currents were obtained despite dc-link voltage ripples. With these SVPWM methods, the maximum obtainable output voltage is limited in the linear modulation region. To overcome this problem, we proposed the use of carrier-based PWM for a 4S3P inverter in [7].

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In this paper, the adaptive carrier-based PWM method is developed for a 4S3P inverter control. The proposed method provides a very simple way to generate the desired output voltage from the intersection of reference signals and a triangle signal. It is simply implemented with either an analog or a digital solution. And, with this proposed carrier-based PWM method, the calculation time is significantly reduced and the linear modulation region for output voltages can be extended.

Firstly, a review of 4S3P inverter topology and SVPWM analysis is presented in section 2. The conventional method and proposed method are then analyzed in section 3. The modulation technique in the over-modulation region is presented in section 4. Finally, simulation and experimental results are provided in section 5 to verify the effectiveness of the proposed adaptive carrier-based PWM method.

## 2. Four–Switch Three–Phase Inverter Topology and Space Vector Analysis

Fig. 1 presents the circuit diagram of a 4S3P inverter fed by a three-phase diode rectifier. The 4S3P inverter topology consists of four switches that provide two inverter output phases: B and C. The third output phase, phase A, is connected to the midpoint of the two split capacitors.

The zero potential point is defined as point 0 in Fig. 1. The phase-to-zero voltages VA0, VB0 and VC0 depend on the switching states of S1, S2, S3 and S4, and two dc-link

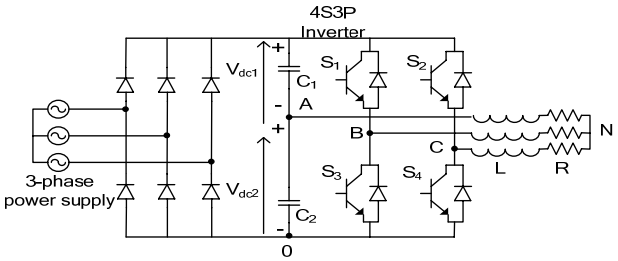


**Fig. 1.** 4S3P inverter topology.

voltages (Vdc1, Vdc2). The phase-to-zero voltages are determined as follows:

$$V_{A0}=V_{dc2} \quad (1)$$

$$V_{B0}=S_1(V_{dc1}+V_{dc2}) \quad (2)$$

$$V_{C0}=S_2(V_{dc1}+V_{dc2}) \quad (3)$$

where $V_{dc}$ is the total dc-link voltage. $V_{dc1}$, $V_{dc2}$ are voltages across two capacitors $C_1$ and $C_2$, respectively.

Switching state $S_x = 0$ when the switch $S_x$ is off and $S_x = 1$ when the switch $S_x$ is on (x=1,2).

The following equations are obtained under balanced load conditions:

$$V_{AN}+V_{BN}+V_{CN}=0 \quad (4)$$

$$V_{A0}+V_{B0}+V_{C0}-3V_{N0}=0 \quad (5)$$

$$V_{N0}=\frac{V_{A0}+V_{B0}+V_{C0}}{3} \quad (6)$$

From (4)-(6), the phase-to-neutral voltages $V_{AN}$, $V_{BN}$ and $V_{CN}$ are derived:

$$V_{AN}=\frac{2}{3}V_{A0}-\frac{1}{3}(V_{B0}+V_{C0}) \quad (7)$$

$$V_{BN}=\frac{2}{3}V_{B0}-\frac{1}{3}(V_{A0}+V_{C0}) \quad (8)$$

$$V_{CN}=\frac{2}{3}V_{C0}-\frac{1}{3}(V_{A0}+V_{B0}) \quad (9)$$

Table 1 shows the phase-to-zero and phase-to-neutral output voltages corresponding to all possible switching states of the 4S3P inverter.

The phase-to-neutral output voltages can be transformed into space vector form with real and imaginary axes by the following expression:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix}=\frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} V_{A0} \\ V_{B0} \\ V_{C0} \end{bmatrix} \quad (10)$$

Using all possible switching combinations of $S_1$ and $S_2$, the 4S3P inverter can only generate four output voltage vectors, which are all active vectors. The output voltage space vectors obtained are summarized in Table 2.

**Table 1.** Phase-to-zero and phase-to-neutral output voltages

| $S_1$ | $S_2$ | $V_{A0}$ | $V_{B0}$ | $V_{C0}$ | $V_{AN}$ | $V_{BN}$ | $V_{CN}$ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | $V_{dc2}$ | 0 | 0 | $2V_{dc2}/3$ | $-V_{dc2}/3$ | $-V_{dc2}/3$ |
| 1 | 0 | $V_{dc2}$ | $V_{dc1}+V_{dc2}$ | 0 | $V_{dc2}/3-V_{dc1}/3$ | $2V_{dc1}/3+V_{dc2}/3$ | $-V_{dc1}/3-2V_{dc2}/3$ |
| 1 | 1 | $V_{dc2}$ | $V_{dc1}+V_{dc2}$ | $V_{dc1}+V_{dc2}$ | $-2V_{dc1}/3$ | $V_{dc1}/3$ | $V_{dc1}/3$ |
| 0 | 1 | $V_{dc2}$ | 0 | $V_{dc1}+V_{dc2}$ | $V_{dc2}/3-V_{dc1}/3$ | $-V_{dc1}/3-2V_{dc2}/3$ | $2V_{dc1}/3+V_{dc2}/3$ |

**Table 2.** Voltage vectors in αβ plane

| $S_1$ | $S_2$ | Vector | $V_\alpha$ | $V_\beta$ |
|---|---|---|---|---|
| 0 | 0 | $V_1$ | $2V_{dc2}/3$ | 0 |
| 1 | 0 | $V_2$ | $(V_{dc2}-V_{dc1})/3$ | $(V_{dc1}+V_{dc2})/\sqrt{3}$ |
| 1 | 1 | $V_3$ | $-2V_{dc1}/3$ | 0 |
| 0 | 1 | $V_4$ | $(V_{dc2}-V_{dc1})/3$ | $-(V_{dc1}+V_{dc2})/\sqrt{3}$ |

When the capacitance of two split capacitors is large enough to keep $V_{dc1}$ and $V_{dc2}$ constant, $V_{dc1} = V_{dc2} = V_{dc}/2$, and the four voltage vectors are presented in Fig. 2(a) in which $V_2$ and $V_4$ are perpendicular to $V_1$ and $V_3$, respectively. In cases with a small capacitance of the two split capacitors, the unbalancing of the two dc-link voltages occurs, $V_{dc1} \neq V_{dc2}$, and the combination of the switching states leads to the four voltage vectors presented in Fig. 2(b). The dc-link voltage ripples lead to the change of both amplitude and angular of the voltage vectors. With the 4S3P inverter, the unbalance between the halves of the split capacitors is the main cause directly affecting its ability to generate balanced output currents. The dc-link voltage ripples occur for several reasons. The first is caused by rectification of the power supply. The second occurs as a result of phase current circulating through the dc-link capacitors. The solution for output distortions can be carried out by increasing the capacitances of two dc-link capacitors, but this increases the cost and size of the 4S3P inverter. Hence, some compensating methods were suggested to generate a balanced output without increasing the capacitance of the dc-link capacitors [5], [6].

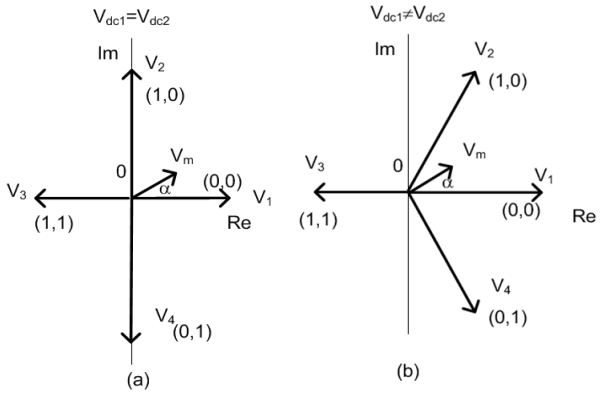


**Fig. 2.** Space voltage vectors in a 4S3P inverter in two cases. (a) Balanced dc-link voltages (b) Unbalanced dc-link voltages.

## 3. Proposed Adaptive Carrier-Based PWM Method

### 3.1 Conventional Space Vector PWM

Compared to six-switch three-phase (6S3P) inverters, there are no zero vectors in 4S3P inverters, only four active vectors. Let us define $V_m$ as the desired output voltage in

Fig. 2(b). The desired output voltage vector can be modulated by using the space vector technique. During each sampling period, three vectors among four active space vectors are used to generate the desired output voltage vector. Table 3 shows the selected vectors corresponding to the space sector.

**Table 3.** Sectors and selected vectors

| Sector | Selected vectors |
|---|---|
| 1 | $V_1, V_2, V_3$ |
| 2 | $V_1, V_3, V_4$ |

The time durations of each vector are given by:
In sector 1: $0 \le \alpha \le \pi$

$$T_1 = \frac{V_{dc1}}{V_{dc1}+V_{dc2}} T - \frac{\sqrt{3} T V_m}{V_{dc1}+V_{dc2}} \sin(\alpha - \frac{\pi}{3}) \quad (11)$$

$$T_2 = \frac{\sqrt{3} T V_m}{V_{dc1}+V_{dc2}} \sin(\alpha) \quad (12)$$

$$T_3 = \frac{V_{dc2}}{V_{dc1}+V_{dc2}} T - \frac{\sqrt{3} T V_m}{V_{dc1}+V_{dc2}} \sin(\alpha + \frac{\pi}{3}) \quad (13)$$

In sector 2: $\pi \le \alpha \le 2\pi$

$$T_1 = \frac{V_{dc1}}{V_{dc1}+V_{dc2}} T - \frac{\sqrt{3} T V_m}{V_{dc1}+V_{dc2}} \sin(\alpha - \frac{2\pi}{3}) \quad (14)$$

$$T_4 = \frac{\sqrt{3} T V_m}{V_{dc1}+V_{dc2}} \sin(\alpha - \pi) \quad (15)$$

$$T_3 = \frac{V_{dc2}}{V_{dc1}+V_{dc2}} T - \frac{\sqrt{3} T V_m}{V_{dc1}+V_{dc2}} \sin(\alpha - \frac{4\pi}{3}) \quad (16)$$

where $T_x$: time duration of voltage vector $V_x$ (x=1~4).

$\alpha$: angle of reference voltage vector. T: sampling period.

The time duration of each vector can be split in order to obtain a symmetrical distribution over the switching period as shown in Fig. 3(a).

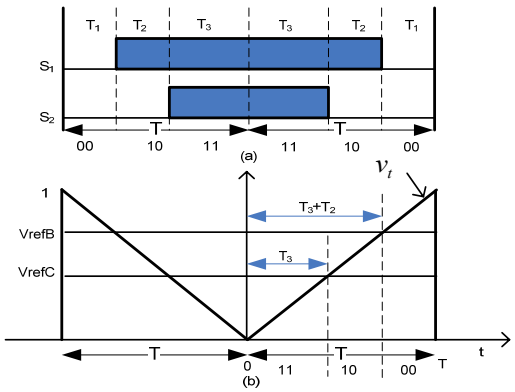


**Fig. 3.** Space-vector modulation and carrier-based PWM in sector 1. (a) Timing of gate pulse of space vector PWM. (b) Timing of gate pulse of carrier–based PWM.

### 3.2 Proposed Adaptive Carrier-based PWM Method

To make it easier to understand the proposed method, we assume that the desired output voltage vector is located in sector 1. Then, space vectors $V_1$, $V_2$ and $V_3$ are used to generate the desired output voltage vector with time durations $T_1$, $T_2$ and $T_3$, respectively. Fig. 3(a) illustrates the sequence and timing of the three selected space vectors in the first sector. Fig. 3(b) shows the carrier signal and the reference signals of the proposed carrier-based PWM method, in which the time duration $t_B$ and $t_C$ of gating pulses for switches $S_1$ and $S_2$ are defined as follows:

$$t_B = T_2 + T_3 \quad (17)$$

$$t_C = T_3 \quad (18)$$

The derivation of time durations, $T_2$ and $T_3$, using two active vectors $V_2$ and $V_3$ can be found in (12) - (13).

To correlate the carrier-based PWM with the space vector method, it is necessary to find the reference voltage signals, which are compared with the triangle carrier signal to generate the same gating pulses as the SVPWM method shown in Fig. 3(b). The normalized triangle signal between the peak value 0 and 1 in the positive slope, shown in Fig. 3(b), can be described as:

$$v_t = \frac{t}{T} \quad (0 \le t \le T) \quad (19)$$

where $v_t$ is the instantaneous carrier signal.

By using $t_B$ and $t_C$ in (17) - (18), the normalized reference signals $V_{refB}$ and $V_{refC}$ are obtained:

$$V_{refB} = \frac{t_B}{T} = \frac{V_{dc2}}{V_{dc1}+V_{dc2}} + \frac{\sqrt{3} V_m}{V_{dc1}+V_{dc2}} \sin(\alpha - \frac{\pi}{3}) \quad (20)$$

$$V_{refC} = \frac{t_C}{T} = \frac{V_{dc2}}{V_{dc1}+V_{dc2}} - \frac{\sqrt{3} V_m}{V_{dc1}+V_{dc2}} \sin(\alpha + \frac{\pi}{3}) \quad (21)$$

Eqs. (20) and (21) are used for sector 1. These are also suitable for the desired output voltage vector located in sector 2.

Using the carrier-based PWM technique for the desired output voltage $V_m$, two reference signals, $V_{refB}$ and $V_{refC}$, are compared with the triangle signal to generate the pulse gating signals for two switches $S_1$ and $S_2$. Due to the voltage offset component in the voltage references in (20) - (21), the problems resulted from the dc link voltage oscillation can be compensated.

The control block diagram for generating the reference modulating signals of the 4S3P inverter, using (20) - (21), is shown in Fig. 4. From the three-phase reference voltages $u_{refa}$, $u_{refb}$, $u_{refc}$ and the feedback voltages $V_{dc1}$, $V_{dc2}$, the reference signals $V_{refB}$ and $V_{refC}$ can be deduced for a 4S3P inverter. Compared with the SVPWM method, the proposed method is much simpler, and the calculation time reduction is obtained. Compared to the conventional method,

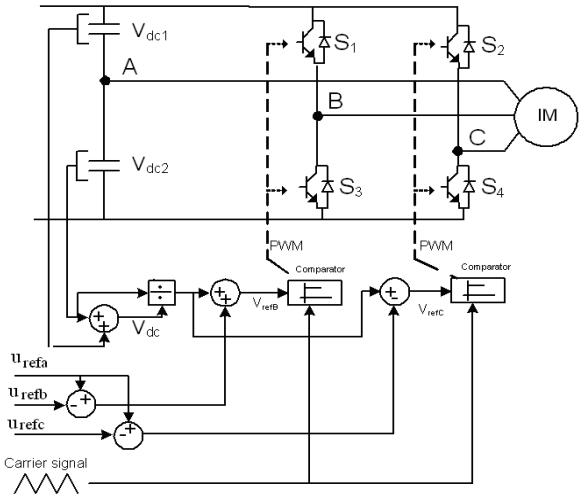


**Fig. 4.** Control block diagram of proposed method.

the calculation time of the proposed method is reduced around 50%. Concretely, the calculation time of the SVPWM method is 37 μs, while the calculation time of the proposed method is 20 μs. Essentially, SVPWM can be transformed into carried-based PWM. The difference is that the modulated waveforms of the SVPWM are obtained by vectors calculation, while the modulated waveforms of carrier-based PWM are calculated by sine wave with dc component injection. In the comparison between the two modulation methods, the carrier-based PWM method is more effective than the SVPWM method in the over-modulation region. In this paper, we proposed the carrier-based-PWM method to obtain the linear over-modulation.

## 4. Linear Over-Modulation Technique Using the Proposed Adaptive Carrier-Based PWM Method

The inherently nonlinear operation in the over-modulation region starts when the desired output voltage exceeds the hexagon boundary. However, the proposed carrier-based PWM method provides a linear control of the inverter output voltage over the entire over-modulation region. We call this region a linear over-modulation region especially because the inverter output voltage can be controlled linearly, even though it's in the over-modulation region.

The time durations of the selected space vectors in (11) - (16) and the reference signals in (20) - (21) are only valid in cases where the desired output voltage amplitude is smaller than the radius of the circle inscribed in the hexagon. This is normally defined as the linear-modulation region shown in Fig. 5(a). In this region, the reference signals, $V_{refB}$ and $V_{refC}$, have the sinusoidal waveforms and the maximum modulation index, $m_{max1}$, is obtained by:

$$m_{max1}=\begin{cases} 2k & \text{if } k<0.5 \\ 1 & \text{if } k=0.5 \\ 2(1-k) & \text{if } k>0.5 \end{cases} \tag{22}$$

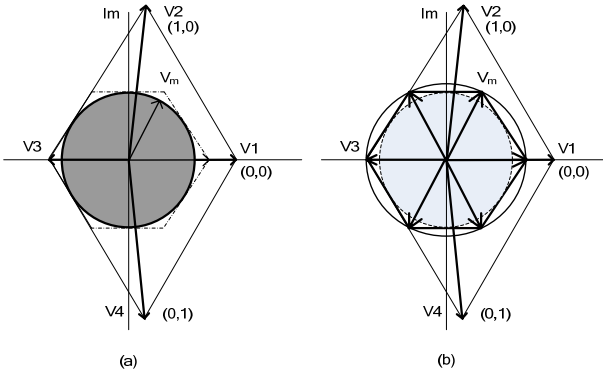


**Fig. 5.** Loci for maximum output voltage (a) Circular locus with modulation index $m_{max1}$ (b) Hexagonal locus with modulation index $m_{max2}$.

where $k=\dfrac{V_{dc1}}{V_{dc}}$.

In linear-modulation region, the maximum obtainable desired output voltage $V_{m,max1}$ is

$$V_{m,max1}=\frac{1}{\sqrt{3}}\min\left(V_{dc1},V_{dc2}\right) \tag{23}$$

Fig. 6(a) shows the reference signals $V_{refB}$ and $V_{refC}$ for the modulation index $m_{max1}$.

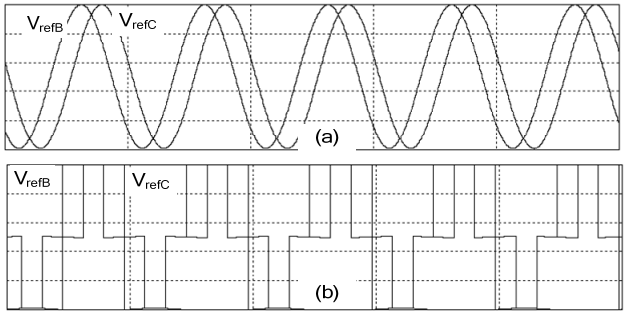


**Fig. 6.** Reference signals $V_{refB}$ and $V_{refC}$ with the modulation index (a) $m_{max1}$ (b) $m_{max2}$.

Assume that $V_{dc1}<V_{dc2}$, from (20) - (21), the reference signals at the lower bound of the over-modulation region with this modulation index, $m_{max1}$, are:

$$V_{refBmax1}=\frac{V_{dc2}}{V_{dc1}+V_{dc2}}+\frac{V_{dc1}}{V_{dc1}+V_{dc2}}\sin(\alpha-\frac{\pi}{3}) \tag{24}$$

$$V_{refCmax1}=\frac{V_{dc2}}{V_{dc1}+V_{dc2}}-\frac{V_{dc1}}{V_{dc1}+V_{dc2}}\sin(\alpha+\frac{\pi}{3}) \tag{25}$$

In the over-modulation region, the maximum hexagonal modulation gives a hexagonal vertex length as shown in Fig. 5(b). In this region, the references signals, $V_{refB}$ and $V_{refC}$, have the square waveforms and the maximum modulation index, $m_{max2}$, is obtained:

$$m_{max2}=\begin{cases} 4k/\sqrt{3} & \text{if } k<0.5 \\ 2/\sqrt{3} & \text{if } k=0.5 \\ 4(1-k)/\sqrt{3} & \text{if } k>0.5 \end{cases} \quad (26)$$

The maximum obtainable desired output voltage $V_{m,max2}$ is

$$V_{m,max2}=\frac{2}{3}\min\left(V_{dc1},V_{dc2}\right) \quad (27)$$

From Fig. 5(b), the reference signals with this maximum modulation index, $m_{max2}$, are:

$$V_{refBmax2}=\begin{cases} \frac{V_{dc2}-V_{dc1}}{V_{dc}} & \text{if } \alpha\in[\frac{-\pi}{2},\frac{\pi}{6}] \\ \frac{V_{dc2}}{V_{dc}} & \text{if } \alpha\in[\frac{\pi}{6},\frac{\pi}{2}]\cup\alpha\in[\frac{7\pi}{6},\frac{3\pi}{2}] \\ 1 & \text{if } \alpha\in[\frac{\pi}{2},\frac{3\pi}{2}] \end{cases} \quad (28)$$

$$V_{refCmax2}=\begin{cases} \frac{V_{dc2}-V_{dc1}}{V_{dc}} & \text{if } \alpha\in[\frac{-\pi}{2},\frac{\pi}{6}] \\ \frac{V_{dc2}}{V_{dc}} & \text{if } \alpha\in[\frac{\pi}{2},\frac{5\pi}{6}]\cup\alpha\in[\frac{3\pi}{2},\frac{11\pi}{6}] \\ 1 & \text{if } \alpha\in[\frac{5\pi}{6},\frac{3\pi}{2}] \end{cases} \quad (29)$$

Fig. 6(b) shows the square waveforms of reference signals $V_{refB}$ and $V_{refC}$ with the modulation index $m_{max2}$

To generate the desired output voltage in the linear over-modulation region, we use the control principle between the limited trajectories technique. This technique is described as follow by assuming $V_{refBmax1}$ and $V_{refBmax2}$ to be the reference signals of modulation index $m_{max1}$ and $m_{max2}$, respectively. The desired reference signals for the modulation index, $m_x$ ( $m_{max1}\le m_x\le m_{max2}$), are driven by:

$$V_{refBx}=\left(1-\eta\right)V_{refBmax1}+\eta V_{refBmax2} \quad (30)$$

where

$$\eta=\frac{m_x-m_{max1}}{m_{max2}-m_{max1}} \quad (31)$$

Similarly, the reference signal $V_{refCx}$ for switch $S_2$ is obtained by:

$$V_{refCx}=\left(1-\eta\right)V_{refCmax1}+\eta V_{refCmax2} \quad (32)$$

Finally, to modulate the desired output voltage with the modulation index between $m_{max1}$ and $m_{max2}$, the reference signals for two switches $S_1$, $S_2$ are determined by (30) - (32), where the reference signals with two bounds $m_{max1}$, $m_{max2}$ are provided in (24) - (25) and (28) - (29), respectively. The fundamental component of the output voltage is a linear function of modulation index $m_x$. Fig. 7 shows the reference signals with different modulation index $m_x$ values, different η values respectively. As easily seen in Fig. 7, the modulation waveform approaches the square wave when the reference modulation index, $m_x$, increases in the over-modulation region.

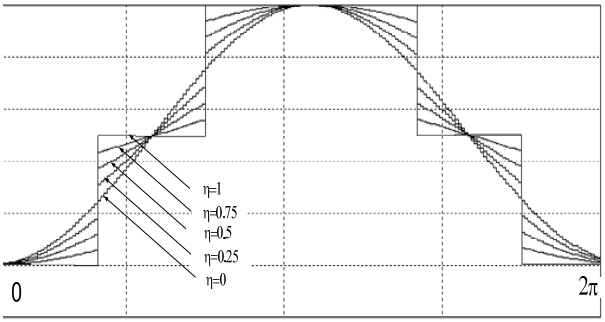


**Fig. 7.** Reference wave profiles for five different η values.

## 5. Simulation and Experimental Results

### 5.1 Simulation Studies

Some simulations were carried out by Psim 6.0 to verify the effectiveness of the proposed method. The system is simulated with the following parameters:

- dc-link voltage: $V_{dc}$ = 200V.
- $C_1$=$C_2$= 940μF.
- Switching frequency: T=10kHz.
- 4S3P inverter with ideal switches.
- Three-phase R-L load: R=20Ω, L=14mH.
- Induction motor's parameters are given in Table 4.

**Table 4.** Induction motor's parameters

| Parameters | Value |
|---|---|
| Rated Power | 3 [Hp] |
| Rated Voltage | 220/380 V |
| Number of Poles | 4 |
| Rated current | 9.0/5.2 A |
| Stator Resistance | 2.077 [Ω] |
| Rotor Resistance | 1.964 [Ω] |
| Stator Leakage Inductance | 0.026 [H] |
| Rotor Leakage Inductance | 0.026 [H] |
| Mutual Inductance | 0.239 [H] |

Figs. 8(a), (b) and (c) show the dc-link voltages, output currents waveforms using the uncompensated algorithm and the output currents using the proposed method at reference output voltage m=0.8, $f_o$=50Hz under the unbalanced capacitor voltage with R-L load. As shown in Fig. 8(b), the

output currents are unbalanced due to no voltage ripple compensation. The unbalanced currents cause the oscillation at the load side. This unbalance problem can be fully overcome by using the adaptive carrier-based PWM algorithm, which compensates the dc-link voltage ripples. As shown in Fig. 8(c), the output current waveforms become balanced through the proposed PWM method.

Fig. 9 shows the operation of the proposed adaptive PWM method for induction motor (IM). As explained before, the unbalanced output currents are resulted from the uncompensated voltage ripples. As easily seen in Figs. 8(c) and 9(c), the proposed method yields the balanced output currents.

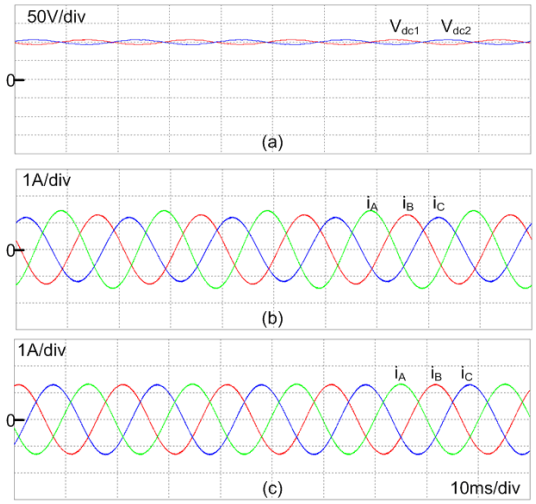


**Fig. 8.** Simulated 4S3P inverter m=0.8, $f_o$ = 50Hz, with RL load case (a) dc-link voltages (b) output currents without considering dc-link ripple (c) output currents with proposed method.

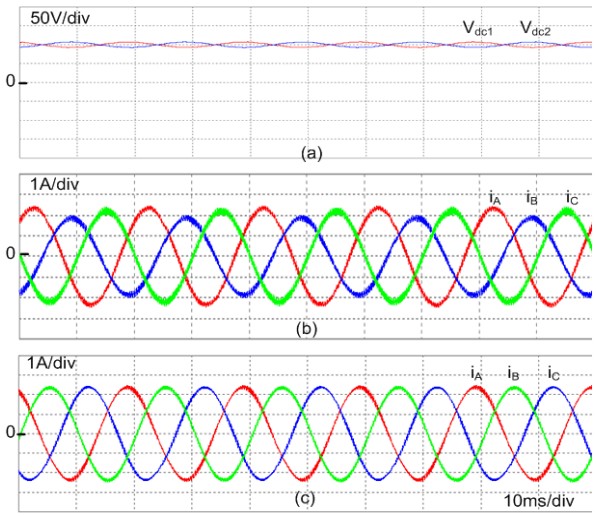


**Fig. 9.** Simulated 4S3P inverter m=0.8, $f_o$=50Hz with IM load case (a) dc-link voltages (b) output currents without considering dc-link ripple (c) output currents with proposed method.

Figs. 10 and 11 illustrate the output current waveforms in the over-modulation region by using linearized technique for five different η values: η=0, η=0.25, η=0.50, η=0.75 and η=1. The modulation index increases linearly from $m_{max1}$ to $m_{max2}$ as η value is increasing from (31): the modulation index is mmax1 at η=0, and the modulation index is $m_{max2}$ at η=1. As the value η or the modulation index is increased, a large amount of subcarrier frequencies in the voltage and current are generated, which means that output voltages and currents are distorted.

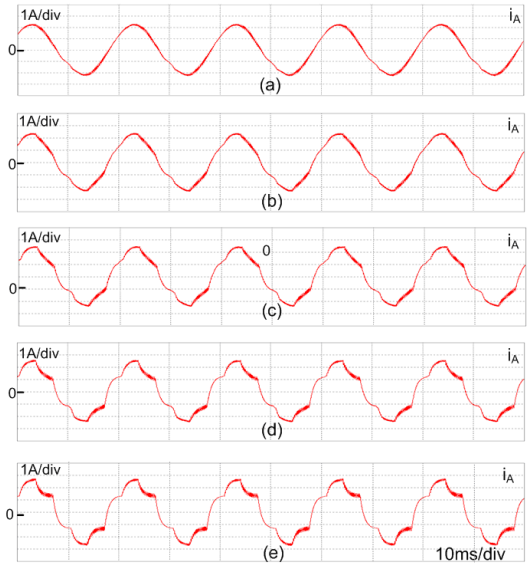


**Fig. 10.** Simulated output current, m=0.8, $f_o$=50Hz in over-modulation region with different η values for R-L load (a) η=0 (b) η=0.25 (c) η=0.5 (d) η=0.75 (e) η=1.

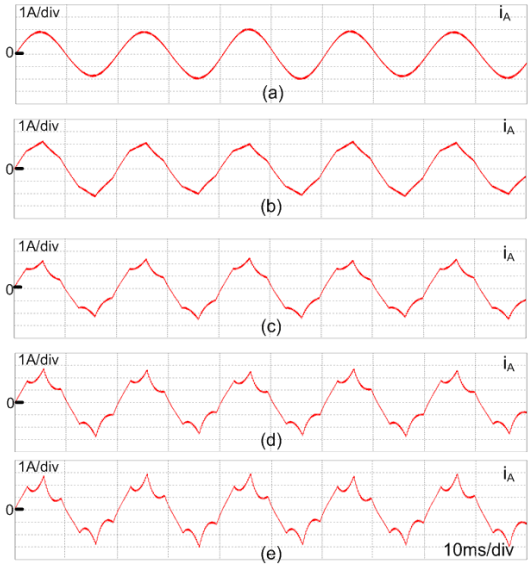


**Fig. 11.** Simulated output current, m=0.8, $f_o$=50Hz in over-modulation region with different η values for IM load. (a) η=0 (b) η=0.25 (c) η=0.5 (d) η=0.75 (e) η=1.

### 5.2 Experimental Results

To validate the theories and simulated results, the experiments were carried out for three-phase R-L load and induction motor load. The experiment parameters are the same as those used in the simulation. The control algorithm was implemented by a 150 MHz DSP - TMS320F2812 with a sampling frequency of 10 kHz.

Figs. 12 and 13 show the experimental data in two cases: R-L load and motor load. Figs. 12(a) and 13(a) show the measured dc-link voltage $V_{dc1}$ and $V_{dc2}$, both of them oscillate in the opposite direction, but the total magnitude of voltage is constant. Figs. 12(b) and 13(b) show the output current waveforms of the uncompensated method for each load case at the reference output voltage, m=0.8, $f_o$=50Hz. The corresponding waveforms for the proposed compensated PWM method are given in Figs. 12(c) and 13(c), respectively.

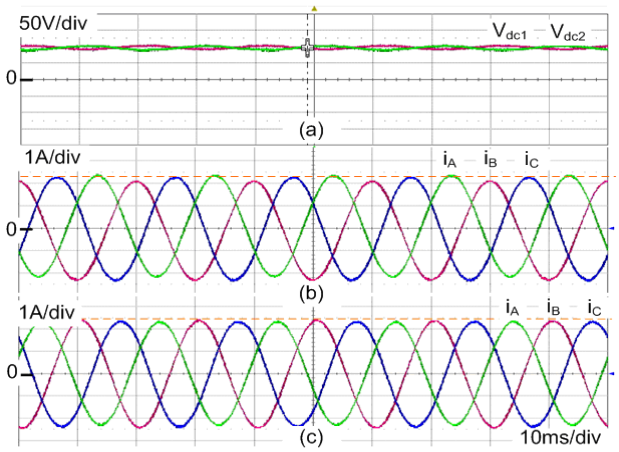


**Fig. 12.** Experimental results for RL load with m=0.8, $f_o$=50Hz (a) dc-link voltages (b) output currents without considering dc-link ripple (c) output currents with proposed method.

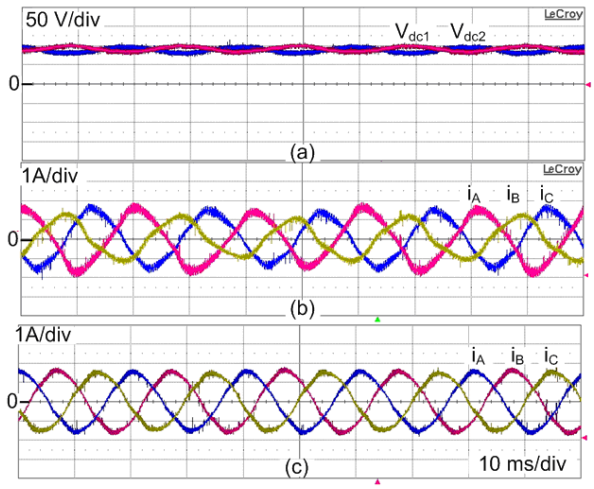


**Fig. 13.** Experimental results for IM load with m=0.8, $f_o$=50Hz (a) dc–link voltages (b) output current without considering dc-link ripple (c) output currents with proposed method.

As can be seen, the compensated PWM method generates balanced output currents, while the phase currents are distorted and unbalanced without compensation.

The combination of the bounds $m_{max1}$ and $m_{max2}$ with the linearized technique can make various modulation indexes inside the region [$m_{max1}$, $m_{max2}$] by using different values.

Figs. 14 and 15 illustrate the experimental inverter output current waveforms in the over-modulation region with the five different modulation index values, which increase linearly from mmax1 and $m_{max2}$ for two cases: R-L load and motor load. For the given switching frequency, the current distortion increases with the higher modulation index as shown in Figs. 14 and 15. As the modulation index reaches the limit modulation index $m_{max2}$ i.e. $\eta$=1, the waveform of the current becomes similar to that obtained from six-step inverter. In cases where a linearity of voltage output is guaranteed, the motor current is not changed suddenly, and this leads to a smooth operation during transition from the linear control range to the upper limit of over-modulation range. The experimental results totally verified the simulation results and demonstrated that the linearity of the output voltage can be extended to the over-modulation region for the 4S3P inverter due to the proposed method.

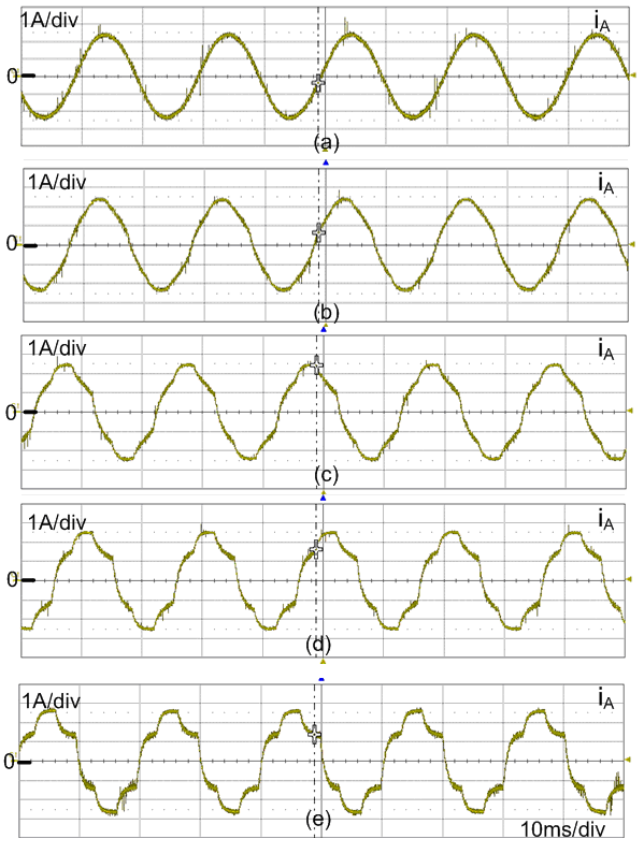


**Fig. 14.** Measured output currents for $f_o$=50Hz in over-modulation region with five different $\eta$ values for R-L load (a) $\eta$=0 (b) $\eta$=0.25 (c) $\eta$=0.5 (d) $\eta$=0.75 (e) $\eta$=1.

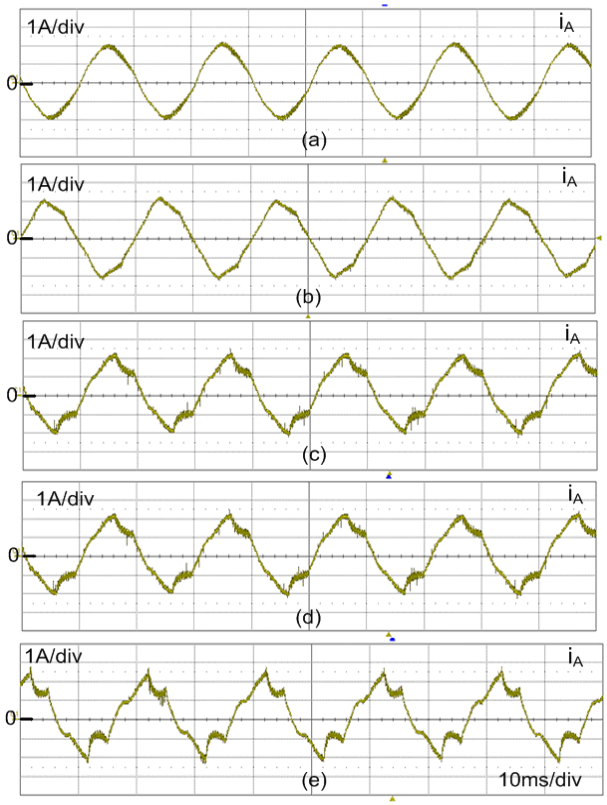


**Fig. 15.** Measured output currents for $f_o$=50Hz in over-modulation region with five different η values for IM load (a) η=0 (b) η=0.25 (c) η=0.5 (d) η=0.75 (e) η=1.

## 5. Conclusion

This paper presented a simple adaptive carrier-based PWM method to overcome the unbalance currents in a low-cost 4S3P inverter. The dc-link voltage ripples have been considered and the compensation method was proposed. The over-modulation region and the waveform of the carrier-based PWM method were investigated to extend the output voltage linearity. The calculation time is greatly reduced due to the carrier-based PWM method instead of the SVPWM method, and the linear operation in the over-modulation region for the 4S3P inverter is easily realized and implemented. Finally, both simulation and experimental results were provided to verify the effectiveness of the proposed theory.

## Acknowledgements

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