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Experimental investigation of Scalability of DDR DRAM packages

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Abstract : A two-facet approach was used to investigate the parametric performance of functional high-speed DDR3 (Double Data Rate) DRAM (Dynamic Random Access Memory) die placed in different types of BGA (Ball Grid Array) packages: wire-bonded BGA (FBGA, Fine Ball Grid Array), flip-chip (FCBGA) and lead-bonded microBGA®. In the first section, packaged live DDR3 die were tested using automatic test equipment using high-resolution shmoo plots. It was found that the best timing and voltage margin was obtained using the lead-bonded microBGA, followed by the wire-bonded FBGA with the FCBGA exhibiting the worst performance of the three types tested. In particular the flip-chip packaged devices exhibited reduced operating voltage margin. In the second part of this work a test system was designed and constructed to mimic the electrical environment of the data bus in a PC's CPU-Memory subsystem that used a single DIMM (Dual In Line Memory Module) socket in point-to-point and point-to-two-point configurations. The emulation system was used to examine signal integrity for system-level operation at speeds in excess of 6 Gb/pin/sec in order to assess the frequency extensibility of the signal-carrying path of the microBGA considered for future high-speed DRAM packaging. The analyzed signal path was driven from either end of the data bus by a GaAs laser driver capable of operation beyond 10 GHz. Eye diagrams were measured using a high speed sampling oscilloscope with a pulse generator providing a pseudo-random bit sequence stimulus for the laser drivers. The memory controller was emulated using a circuit implemented on a BGA interposer employing the laser driver while the active DRAM was modeled using the same type of laser driver mounted to the DIMM module. A custom silicon loading die was designed and fabricated and placed into the microBGA packages that were attached to an instrumented DIMM module. It was found that 6.6 Gb/sec/pin operation appears feasible in both point to point and point to two point configurations when the input capacitance is limited to 2pF.

Keywords: Ball grid array, DRAM packaging, flip-chip packaging, DIMM

1. Introduction

This paper describes experimental investigations of the electrical performance of selected package candidates under consideration for the next generation of DRAM such as DDR4. There were two major parts of the investigation: parametric performance measurement of packaged high speed DRAM using an Automatic Test Equipment (ATE) environment and a further investigation of the high speed signal integrity performance of the packages used in a representative system environment. The first part examined the relative performance of today's DDR3 die in three popular packages, while the second part examined the ability of the microBGA package to carry significantly higher speed signals in a realistic system environment as a way determining suitability of it for the next generation DRAM.

In the first part of the work, live DDR3 DRAM die were packaged into three different package types: FBGA, FCBGA and lead-bonded microBGA. Devices were assembled from the same wafer lot for the three package types and five randomly selected functional units of each type were tested using a Verigy 93 K high speed VLSI tester used in shmoo plotting mode.

The shmoo plots show the pass/fail delineation for a range of timing and power supply voltage conditions. Because the power supply voltage is included in the shmoo variables, the device operational window includes the effect of power supply noise: the higher the power supply noise, the smaller the operational window. While not appropriate for absolute noise measurements, shmoo plots provide a useful method to compare package alternatives to see which shows the largest operational envelope.

The lead-bonded microBGA has the smallest number of impedance discontinuities[1)] of the three package types tested: two total. One discontinuity is found where the leads are bonded to the die and the other is where the solder ball attaches to the substrate pad (Figure 1).

The wire bonded window BGA (FBGA) has one more impedance discontinuity than the lead-bonded microBGA: one on each side of the wirebond and one where the solder

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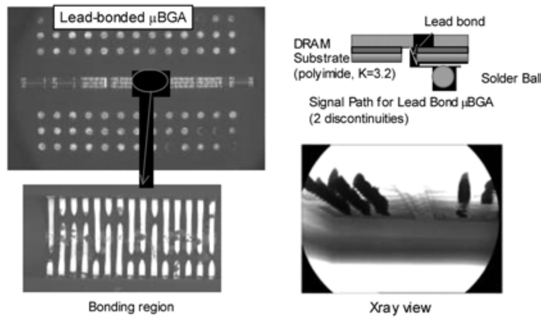

Fig. 1. Lead-bonded microBGA Details.

ball attaches to the substrate (Figure 2). The FCBGA substrate has a two layer substrate and has five impedance discontinuities: one on each side of the gold stud-bump on the die, another on each side of the via (each side of the substrate) and another where the solder ball attaches to the substrate (Figure 3). Neither the FBGA nor the lead-bonded microBGA substrates use vias: both are single layer substrates. The lead-bonded microBGA uses a polyimide substrate (K=3.2) while both the FCBGA and FBGA use FR4 or BT type substrates (K=4.7).

The shmoo results (figure 4) show that the worst operating window was obtained for the FCBGA packaged devices. The Lead-bonded microBGA demonstrated the best performance while the FBGA's performance was slightly worse.

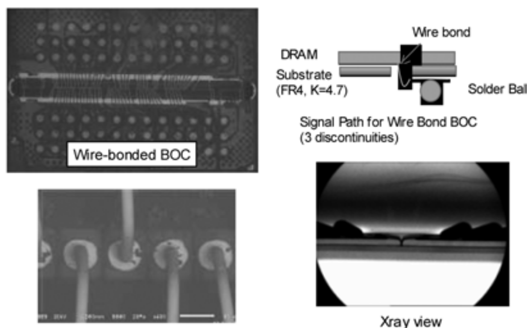

Fig. 2. Wire Bonded BGA (FBGA) Details.

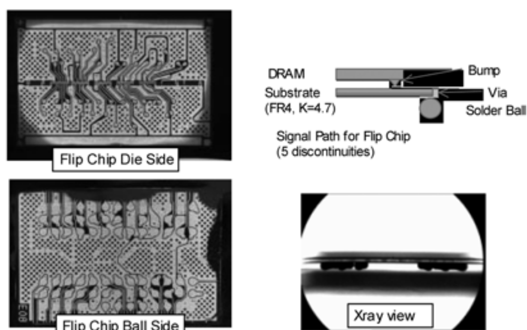

Fig. 3. Flip Chip BGA (FCBGA) Details.

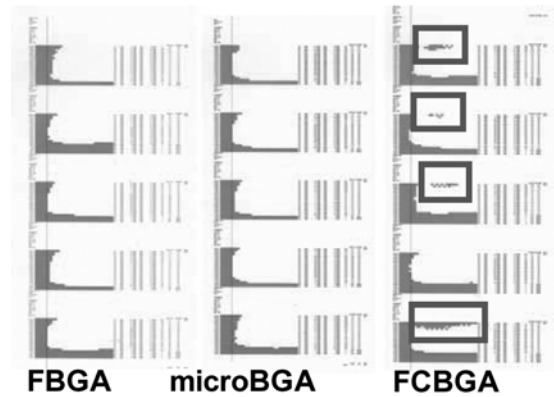

Fig. 4. Shmoo Plots of 15 live DDR3 DRAM in three package types (FBGA, Lead-bonded microBGA, FCBGA).

The shmoo plots of the FCBGA show failures at high voltage operation. Because devices switch faster at higher operating voltage, these failures may originate from noise on the internal power supply buses. Such noise normally arises from power bus switching currents within the DRAM interacting with the reactance of the signal routing within the package. Without a detailed knowledge of the internal design of the DRAM circuits, it is impractical to make a model of the DRAM die suitable for examining the issue of power supply routing in the package. As a result, the shmoo data was the best indicator available for monitoring the internal noise for the scope of this work.

2. Signaling Test System

In the second part of this work, high frequency signal propagation characteristics of the package used in a typical PC motherboard system configuration are studied in combination. For the high speed signal integrity measurements, custom designed hardware was constructed to emulate the data path found in a PC motherboard system using a single DRAM DIMM socket.

The hardware system includes a BGA packaged memory controller emulator connected to a motherboard emulator that includes a single DIMM socket. Plugged into the DIMM socket is a specially instrumented DIMM containing packaged DRAM loading die as well as a high speed line driver circuit. The memory controller emulator and the DIMM both include a GaAs high speed line driver capable of driving 50 ohm loads at frequencies beyond 10 Ghz.

The test system was configured to emulate the data path from memory to controller and vice versa. All signaling was unidirectional. Providing stimulus was a high-speed pulse

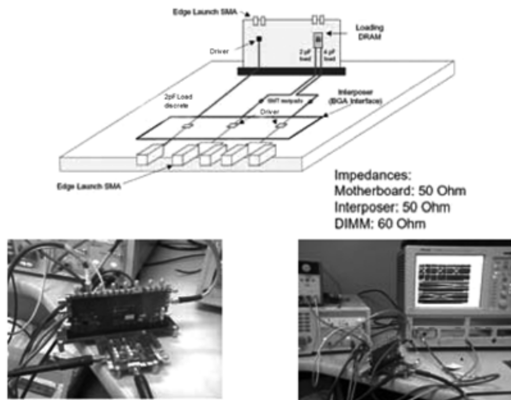

Fig. 5. Signaling Test System.

generator connected to the input of the high speed line driver. The output of the pulse generator is a Pseudo-Random Bit Sequence (“PRBS”) with a pattern length of 2^{32}-1. Monitoring the load end of the test system is a high speed sampling oscilloscope. Eye diagrams were captured for the configurations under test and were examined to ascertain the signal quality.

The DRAM used for the DIMM loading was a “dummy” die packaged in a standard microBGA substrate. This package is identical to the type used for DDR3 DRAM. The dummy loading die consisted of a custom-designed silicon circuit containing a linear RC network to emulate the loading presented by a DRAM DQ pin. The loading capacitance was 2pF to approximate pin loading capacitance found in high speed DRAM. Also placed on the DIMM was a high speed line driver providing the stimulus for exercising the interconnect network when the DIMM is the data source.

To emulate the DRAM controller a combination of a high speed line driver and a loading circuit were placed onto a BGA packaged interposer that was soldered to a PCB designed to emulate the physical length, impedance and layout of a PC motherboard’s memory data path. Also placed on the motherboard was a DIMM socket to accept the DIMM described above.

Two versions of the DIMM were made, with the difference being in the fanout of the DQ bus: Point To Point (PTP) and Point To Two Points (PTTP). For the PTTP configuration, the DRAM loading devices were placed on opposite of the DIMM PCB to replicate standard double sided assembly for a two rank module. Both the DIMM and the motherboard were outfitted with high quality SMA connectors to connect to the pulse generator and to the sampling oscilloscope.

The pulse generator was connected to a one of the controller end or to the DIMM end, depending on the data flow direction; writes to or reads of the memory. Using a Pseudo-Random Bit Sequence (“PRBS”), eye diagrams were measured at the signal destination, both at the controller end and at the DRAM loading end. Eye diagrams were captured for the PTP and PTTP configurations operating at 6.6 GHz using NRZ formatted PRBS stimulus. A set of traces was captured using the controller end as the source and another set was captured using the DRAM end as the source. In all cases the eye

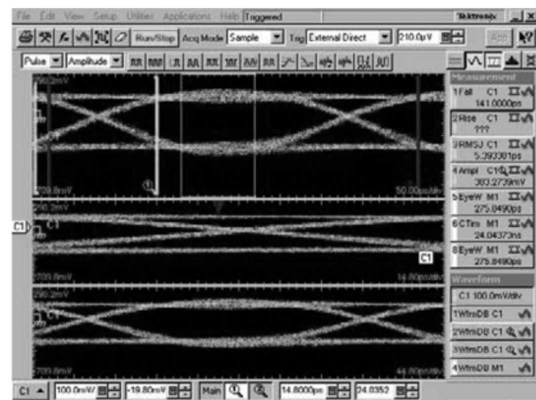

Fig. 6. 6.6 GHz PTP Writes 2pF load on DRAM.

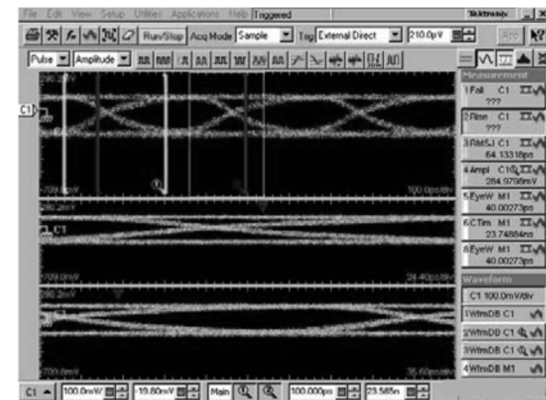

Fig. 7. 6.6 GHz PTTP Writes 2pF load on DRAM.

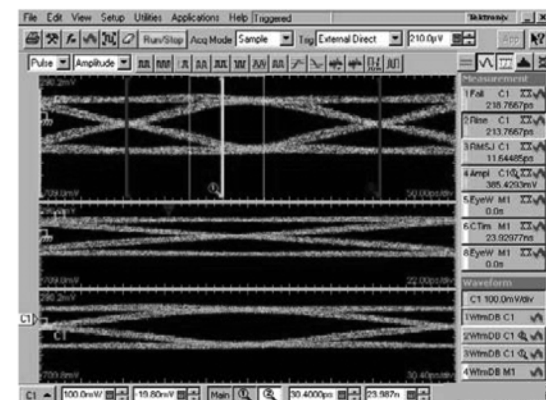

Fig. 8. 6.6 GHz PTP Reads 2pF load on Controller.

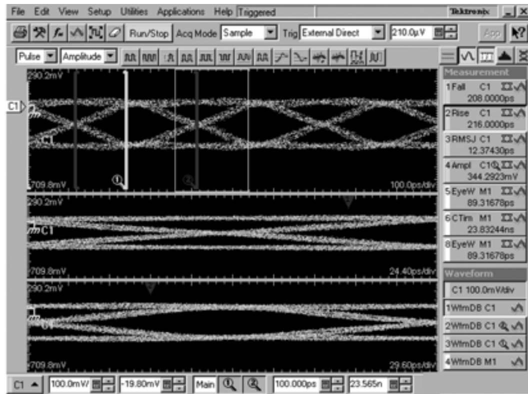

Fig. 9. Figure 6.6 GHz PTTP Reads 2pF load on Controller.

diagrams exhibited acceptable signaling (Figures 6 - 9).

3. Results and Discussion

The shmoo plot results show the best performance was obtained using the lead bonded microBGA.[4] The wire bonded FBGA was next best and had nearly the same performance while the gold stud-bumped FCBGA's performance clearly showed degraded voltage margin at higher operating voltages. Because these die were unable to be tested beyond 1600 MHz operation it is unknown if these die represent the fastest obtainable.

Since power bus/packaging noise issues are aggravated by higher speed operation, it is expected that devices capable of operation at greater than 2 GHz would show a greater difference in margin using the shmoo method. In future work such 'superspeed' devices will be sought for the comparison.

The results from the signaling test system shows the microBGA type packaged DRAM mounted on a standard DIMM module and using standard connectors is capable of supporting the data bus signaling requirements for PTP and PTTP configurations operating at frequencies over 6 Gb/s/pin. Taken in the context of recent reported work[2, 3] showing DRAM die operating at speeds in the 6 Gb/s/pin to 7 Gb/s/pin range, it is expected that same type low cost packages using today's manufacturing infrastructure can provide the electrical performance necessary to support the signaling requirements of the next generation of high speed DRAM described in current literature.

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