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A Method for Reducing the Number of Metal Layers for Embedded LSI Package

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Abstract: We have successfully demonstrated a high-pin-count and thin embedded-LSI package to realize next generation's mobile terminals. The following three design key points were applied: (i) Using Cu posts, (ii) Using the coreless structure, (iii) Using a Cu plate as the ground plane. In order to quantitatively determine the contribution of the three points, the five-stage process for reducing the number of metal layers is described by means of the electrical simulation. The point-(i) and (ii) are effective from the viewpoint of the power integrity (PI); that is, these points play important roles in reducing the number of metal layers, and especially the point-(ii) contributes at least twice as the point-(i). The point-(iii) is not effective in the PI, but has a few effects on the signal integrity (SI). For reducing the number of metal layers, we should, at first, pay attention whether the PI characteristics fulfill the specification, and then we should confirm the SI characteristics.

Keywords: Embedded-LSI packaging, power integrity characteristics, signal integrity characteristics, next generation mobile terminal

1. Introduction

Continuous demands for small form factor and multi functions for mobile terminals will definitely open a new market for personal devices. They will be realized with small and thin housing, just like fashionable mobile phones, and high-performance for multi-media contents, just like laptop PCs. As the early stage of next generation's mobile terminals, smart phones and netbook PCs have been emerged as examples. These kinds of terminals appear to be complement between mobile phones and laptop PCs.

From the viewpoint for the components of these terminals, the LSI package for the next generation's mobile terminals should be large size and compatible to high-pin-count LSIs, compared to the current devices. Therefore, it is important for the LSI package to be shrank, and we successfully developed a thin embedded LSI package and demonstrated its normal operation.[1-2)]

In order to realize our embedded LSI package, the electrical design technology for reducing the number of metal layers contributed greatly, as well as the fabrication process developments.

As shown in our previous study[1-2)], we described the following three design points to realize this package:

(i) Using Cu posts
(ii) Using the coreless structure
(iii) Using a Cu plate as the ground plane

This paper describes the five-stage design process for reducing the number of metal layers for embedded package, in detail. We analyzed how much each design point contributes to the electrical characteristics.

2. Package Structures

First, we describe the features of our LSI package by comparing with a reference FCBGA package. Figure 1

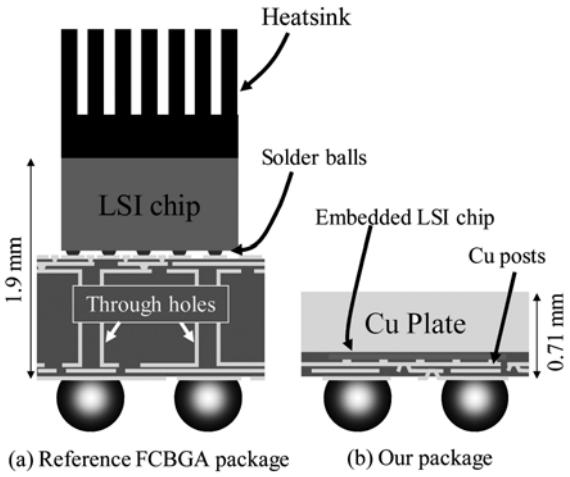

Fig. 1. A reference FCBGA package and our package.

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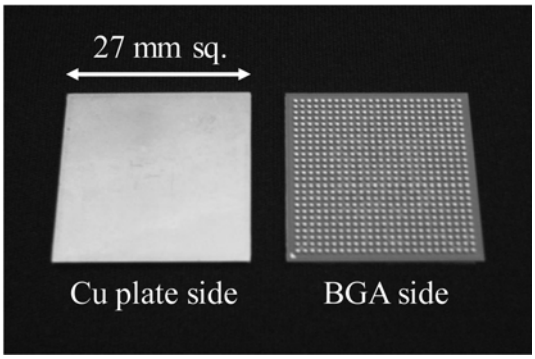

Fig. 2. A photograph of our LSI package.

shows the comparison of the cross-sectional views between the reference FCBGA package with six metal layers and our package with three metal layers. We found that our package is much thinner than the reference FCBGA, because our package employs the coreless structure. The coreless structure does not have any thick supporter, called as “core layers”, but only has thin resin layers, “build-up layers”. As shown in Figure 2, we found that our package looks like almost a Cu plate because of the coreless substrate.

The coreless substrate enables us to use very small vias as signal, power and ground between all the metal layers, as well as to realize the thin structure. The small vias help to reduce the PDN (Power Delivery Network) impedance and the discontinuity between signal traces and signal vias. We have developed original electrical design techniques to make the best use of these advantages.

Here, the electrical specifications for the LSI are briefly described. Table 1 shows the names of the power nets and DC voltages for the five kinds of the PDN. The LSI has several functions with own voltage; therefore, we must pay attention to design for power integrity (PI). On the other hand, the highest signal transmitted in the package is used for the DDR2 memory interface operating at 267 MHz, in another word, 533 Mbps as the data band width. We should confirm the signal characteristics of the DDR2 memory functions first for signal integrity (SI).

Table 1. Power DC Voltages

Name	Voltage	Used for
Power 1	1.2 V	LSI core
Power 2	1.8 V	DDR2 Memory
Power 3	2.5 V	I/O
Power 4	3.3 V	I/O
Power 5	1.2 V	I/O

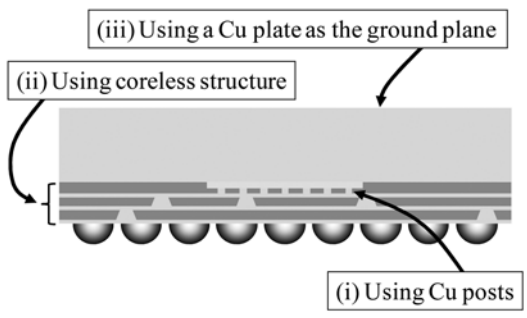

Fig. 3. Three design key points.

3. Three Key Points of the Package Designs

The three design techniques to realize our package are following, as shown in Figure 3:

(i) Using Cu posts
(ii) Using the coreless structure
(iii) Using a Cu plate as the ground plane

3.1. Using Cu posts

In the reference FCBGA package, two metal layers are needed to fan out the signal traces, because the diameters of the solder bump land and land pitch are as large as 160 μm and 320 μm, respectively. But the minimum line/space is 24/24 μm. To fan out the traces on the single metal layer, four rows of signal traces must be formed between the lands in our study. Therefore, it was necessary to reduce these sizes. We employed the Cu post, instead of the solder bump. The diameter of the Cu post land is only 100 μm. Thus, our LSI package allows the fan-out for four rows of signal traces, using the line/space of 20/20 μm, on the top metal layer.

From the above discussion, it is found that this point-(i) allows us to reduce one metal layer.

3.2. Using the coreless structure

In general, a build-up substrate is used for the FCBGA package. The build-up substrate is commonly used for high-pin-count LSI chips because of the design flexibility. But there is a disadvantage of the general build-up substrate in the electrical performance. The through-hole size in the core layer is quite large, resulting in high PDN impedance. In our previous research, the coreless structure enables us to reduce theoretically the via inductance in the core layer down to approximately 1/32.[2)] According to the reference (3), the coreless structure achieved the comparable electrical performance with four metal layers against the FCBGA with eight metal layers by using a simple model. The layer composition is not described in detail; we can estimate that the removed four metal layers consist of three power metal layers and one ground metal

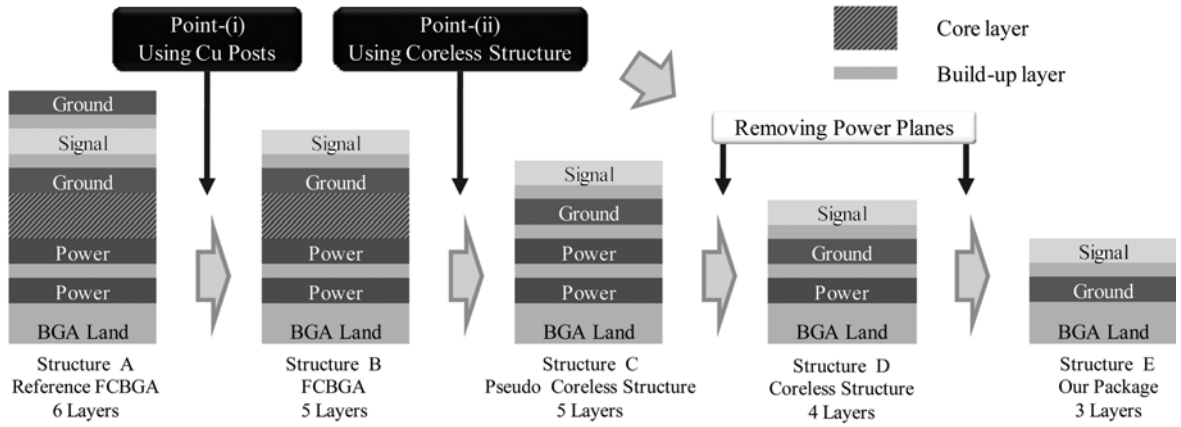

Fig. 4. A Procedure for reducing the number of metal layers.

layer. Therefore we expect to achieve low PDN impedance without the power metal layers by using the coreless structure. In addition, when the number of metal layers reduces, the number of vias, the discontinuity in the structure, also reduces generally. Also, the fine vias enable us to reduce the reflection at the discontinuities between signal traces and vias.[3] This is because the width of the signal trace and the diameter of the via are close to each other. Thus, we expect that this design technique will improve the SI as well as the PI.

By the above consideration, the coreless structure enables to improve the electrical performance, especially the PI characteristics. This point-(ii) allows us to reduce at least one metal layer. In particular, the power metal layer is suitable for the candidate of removal.

3.3. Using a Cu plate as the ground plane

We achieved a strip line structure sandwiching almost all the signal traces between the Cu plate and the second metal layer in order from the LSI side used as the ground.[2] This allows improving the SI characteristics such as the cross-talk noise and the characteristic impedance of signal lines. But this point-(iii) does not play so important role in reducing the number of metal layers.

4. A method for reducing the number of metal layers

Figure 4 shows a procedure for reducing the number of metal layers. The structure-A is the reference FCBGA package whose layer composition is ground, signal, ground, power, power, and BGA lands in order from the LSI side. By applying the point-(i) to the structure-A, the first ground metal layer is removed. We call this the structure-B with five metal layers. To apply the point-(ii) to the structure-B, the core layer thickness is decreased to the same thickness of the build-up layers, but the through-hole via pitch is still kept for convenience. Therefore, this structure-C with five metal layers can be called as the pseudo coreless structure. The structure-C is expected to be outstanding PDN impedance improvement.

Next, the via pitch in all metal layers is optimized as real “coreless” structure. Then, the two power planes are removed one by one because the point-(ii) improves the PDN impedance greatly. The structure-D with four metal layers, whose layer composition is signal, ground, power, BGA lands, is obtained. The structure-D is still expected to be much better PDN impedance than the structure-A. The final structure-E with three metal layers, our embedded LSI package[2], is estimated that the PDN impedance increases up to some extent, because a few power traces were used, instead of power planes.

Through the above procedure, the layer composition of our package was determined. This embedded package substrate is built using only three metal layers against the six metal layers of a build-up substrate in the reference FCBGA using the same chip. Figure 5 shows detailed layout patterns of our package substrate. The top metal layer, connected to the embedded LSI chip, is mostly used as the signal. Most of the middle metal layer is used as the ground. The bottom metal layer is used as the wide power traces together with the BGA lands.

4. Evaluation Method

4.1. Power Integrity (PI) Characteristics

We employed the PDN impedance of the reference FCBGA package as the guideline of normal operation. The PDN impedance is expected to have no resonance and keep low at high frequencies. That is to say, if PDN impedance of

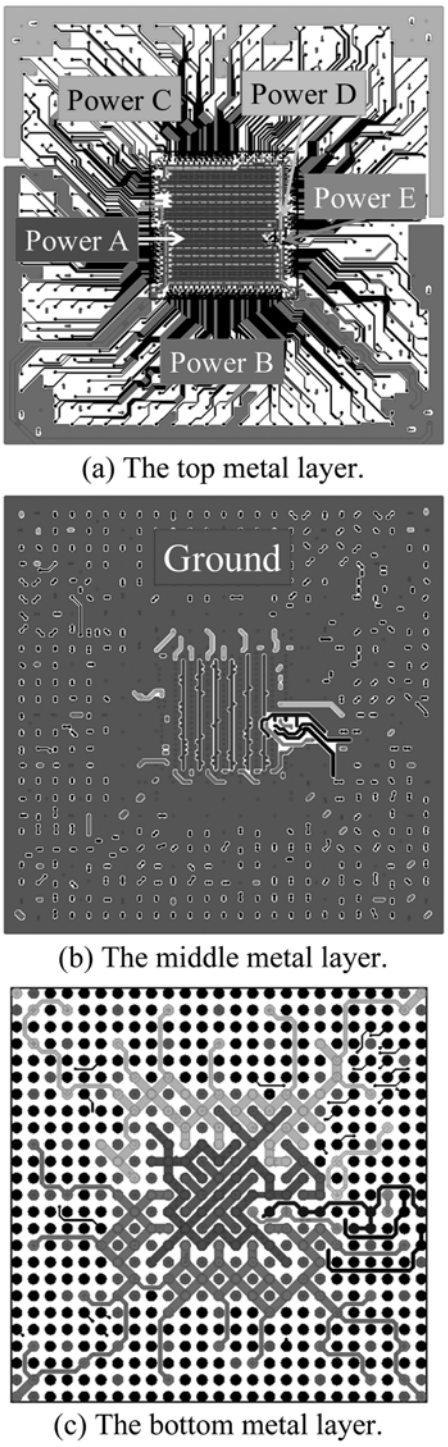

Fig. 5. Layer patterns we finally designed.

our LSI package is lower than that of the reference FCBGA, our package is expected to operate correctly. The PDN impedance from the LSI side was calculated by Ansoft SIwave. Figure 6 shows the method of calculating the PDN impedance.

4.2. Signal Integrity (SI) Characteristics

Signal integrity is evaluated by the insertion loss (S_{21}) of

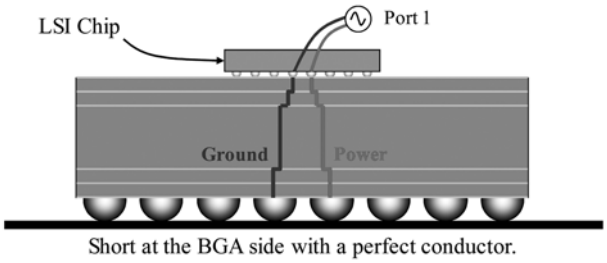

Fig. 6. The set-up for calculating the PDN impedance.

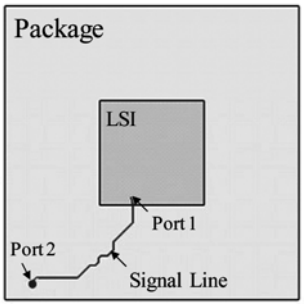

Fig. 7. The set-up for calculating the signal integrity.

one of the longest signal trace and its eye-diagram. Figure 7 shows the set-up for the calculation. The port-1 is at the LSI side and the port-2 is at the BGA side for the insertion loss; the port-1 is the drive point and the port-2 is the receive point for the eye-diagram.

5. Results and Discussion

5.1. PI Characteristics

Figure 8 shows the calculated results of the PDN impedance for each power. The results show that the PDN impedance is inductive at the frequency lower than approximately 1 GHz. Then the PDN impedance can regard as the inductance for all the frequency range. We define the PDN impedance at 267 MHz, the highest signal frequency in the package, as “the PDN inductance” as shown in Table 2. This helps us to distinguish among the structures quantitatively. Table 2 shows the following information: The difference of the structure-A and structure-B, the point (i), is caused by the via inductance of reducing one metal layer. But the difference is small and neglible, because the sizes of the removed vias are small. The difference of the structure-B and structure-C, the point (ii), is large, because the large sizes of through-holes are replaced with the small sizes of vias. We confirmed that the point-(i) and especially the point-(ii) are effective to improve the PDN impedance as expected. The difference of the structure-C, structure D and structure-E is mainly caused by the removal of the power

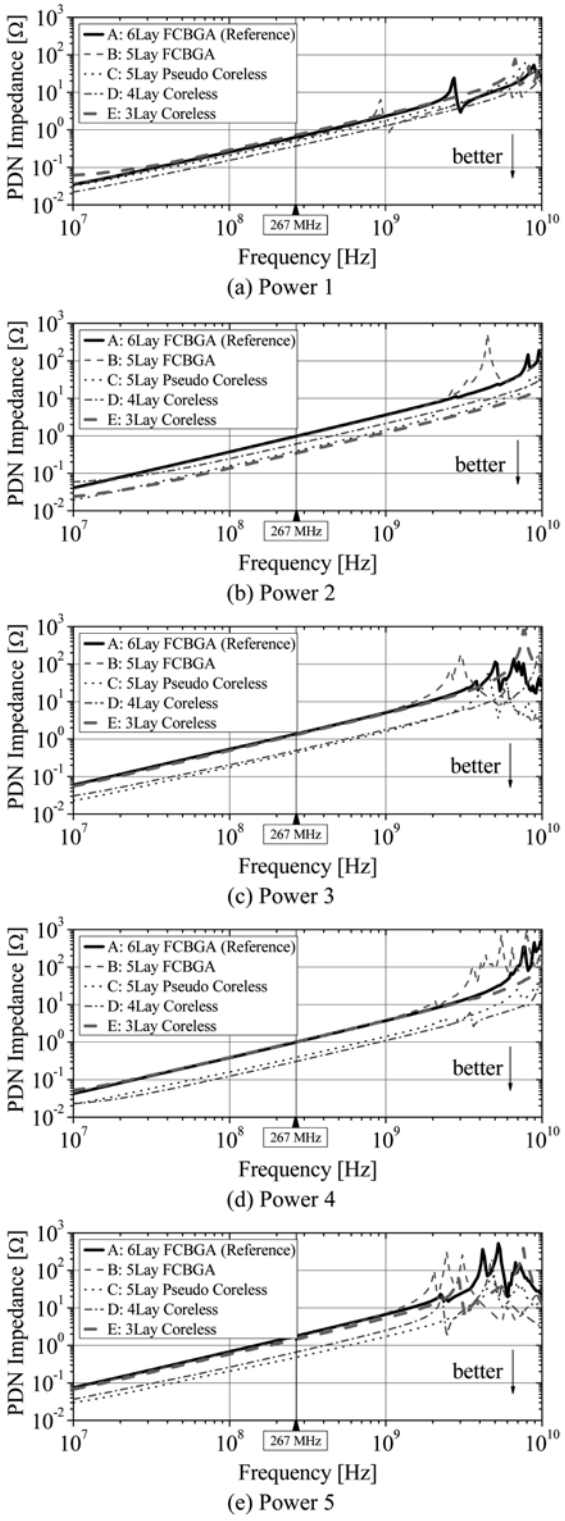

Fig. 8. The PDN impedance for each power.

metal layer. The removal becomes worse the PDN impedance. In particular, the difference of the structure-D and structure-E is large, because the structure-E has no power metal layer. But the structure-E has equivalent PDN impedance to the structure-A due to the improvement by the point-(i) and point-(ii).

Table 2. The PDN inductance at 267 MHz for each power (Unit: nH)

Structure	Power 1	Power 2	Power 3	Power 4	Power 5
A	0.38	0.58	0.82	0.60	1.0
B	0.33	0.54	0.79	0.63	0.99
C	0.30	0.24	0.26	0.23	0.28
D	0.22	0.36	0.30	0.18	0.39
E	0.43	0.21	0.78	0.60	0.86

Therefore, we found our package, the structure-E, has comparable PDN impedance to the reference FCBGA package, structure-A, as expected.

5.2. SI Characteristics

In Figure 9, the comparison of the insertion loss is shown for each power. The results are almost the same up to approximately 1 GHz. We selected the insertiion loss at 267 MHz, and show them in Table 3. We found the structure-D and structure-E are worse in the insertion loss than the other structures, because of the increase in the trace resistance. But the difference from the structue-A is quite small and neglible.

In addition, in order to confirm signal properties in detail, we calculated the waveforms in time domain with Synopsys HSPICE. As shown in Figure 9 and Table 3, the difference between the structure-E, our LSI package, and the struc-ture-A, the reference FCBGA package, is also expected to be neglible in the waveforms. First, we compared waveforms in the package structure only as shown in Figure 7. As shown in

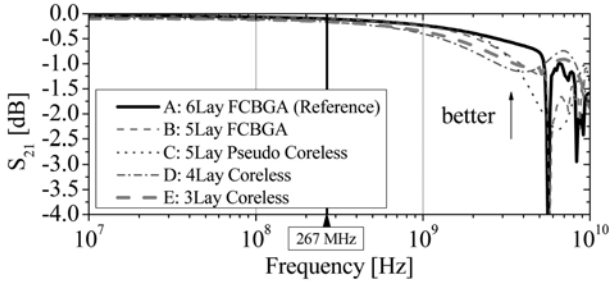

Fig. 9. Comparison of the insertion loss for each structure.

Table 3. The insertion loss of a signal trace at 267 MHz

Structure	Insertion loss [dB]
A	-0.11
B	-0.10
C	-0.10
D	-0.16
E	-0.16

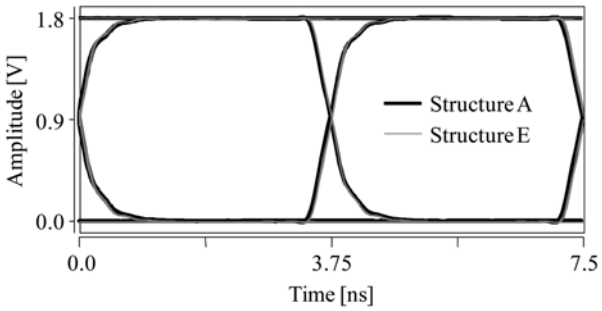

Fig. 10. Comparison between the structures at the receive point (Port 2).

Figure 10, they are almost the same as expected. We found that the structure-E has comparable SI characteristics with the structure-A.

Next, we assumed more actual configuration, as shown in Figure 11. Four DDR2-533 memory modules are connected to the package on a mother board with the same length of the address signal line. A resistance is placed at a junction to improve the effect of the reflection. Figure 12 shows the comparison of the waveforms between the structures. Figure 12(a) is the typical operation frequency, 267 MHz, and Figure 12(b) is twice as the typical operation frequency, 533 MHz to confirm the operating margin. The difference be-tween two waveforms is not large at each frequency. As compared to Figure 10, the waveforms are distorted because of the resistance. Since the waveform is almost the same at 533 MHz, the structure-E has the same operation margin as

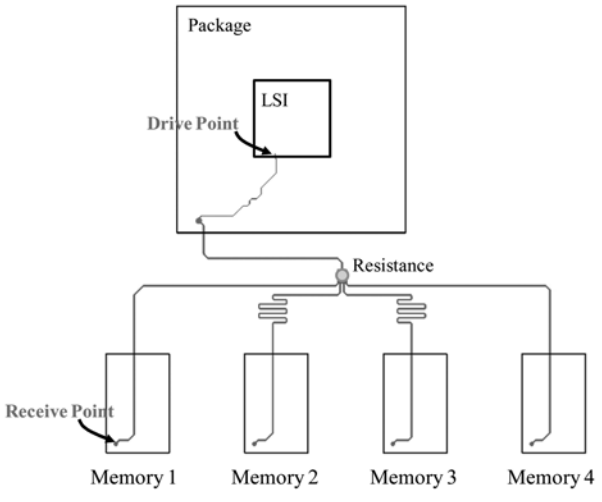

Fig. 11. Location of the simulated signal traces including four DDR2-533 memory packages.

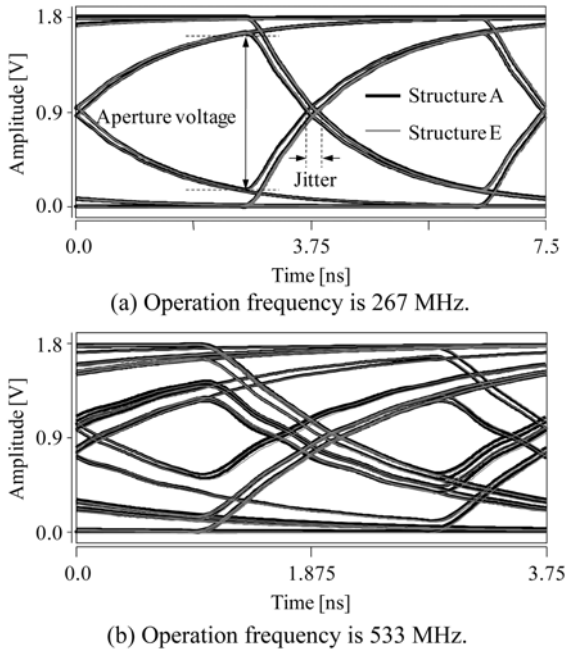

Fig. 12. Comparison of eye diagrams at the receive point.

Table 4. The jitter and the aperture voltage

Frequency [MHz]	Structure	Jitter [ps]	Aperture Voltage [V]
267	A	185	1.46
	E	180	1.47
533	A	610	0.68
	E	5.63	0.70

the structure-A. Table 4 shows the comparison for the jitter and the aperture voltage. We confirmed that our package provides comparable signal properties with the reference FCBGA package even for more actual case.

We found that the difference between the structures is much smaller for the SI than for the PI. In other words, the PI is more sensitive to the change of the layer composition than the SI. Therefore, we should pay attention to the PI first.

Finally we describe the contribution of the point (iii). By realizing the strip line structure, it is easy to control the characteristic impedance of the signal traces. As shown in Figure 13, when the gap between the Cu plate and the middle metal layer is adjusted, the characteristic impedance is matched to the suitable value. There is a problem in the structure-E, our package, that the characteristic impedance is not completely matched, because the embedded LSI and adhesive are too thick to adjust the gap between a Cu plate and the top metal layer. If the thickness of the LSI and adhesive is down to 20 μm and 5 μm, respectively, the

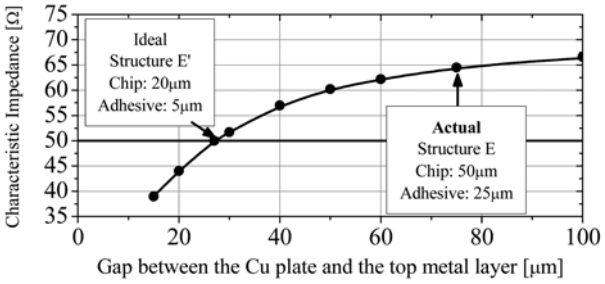

Fig. 13. Relationship between the gap and the characteristic impedance.

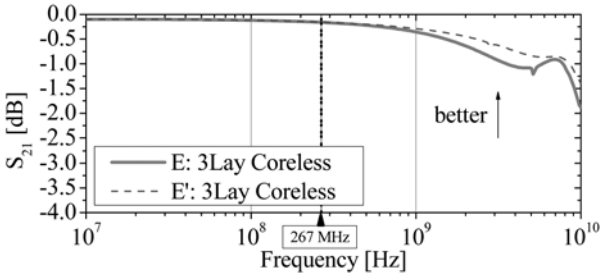

Fig. 14. The insertion loss characteristics.

characteristic impedance is successfully matched. This structure is named as the structure-E'. The comparison of the ideal gap and the actual gap is shown in Figure 14. The result shows that the difference between the ideal and the actual is neglible at the frequency lower than 1 GHz, the same as Figure 9. Therefore the point (iii) does not influence so much on the electrical performance for the specification in our study. But if the operation frequency becomes higher, or the package size becomes larger, the point (iii) will improve the electrical performance.

6. Conclusions

A method for reducing the number of metal layers for embedded LSI package was described. In the three design key points we previously discussed, the point-(i), "Using Cu posts", allows us reducing one metal layer because of the finer interconnection. The point-(ii), "Using coreless struc-267 A 185 1.46E 180 1.47533 A 610 0.68E 563 0.70 ture", allows us reducing two metal layer because of the reduction of the via inductance. The point-(iii), "Using Cu plate as the ground plane", does not contribute effectively for reducing of the number of metal layers for this embedded LSI package. But if the thickness of the resin layer including an LSI chip reduced to that of the build-up layer, the point-(iii) could allow us reducing one metal layer.

In order to reduce the number of metal layers for this kind of the LSI embedded package, we should pay attention to the PI characteristics first, because the number of metal layers affects the PI seriously, compared to the SI. But when the operation frequency becomes higher, or the package size becomes larger, we also must take deep consideration into the SI.

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