플랙시블 기판 위에서 제작된 단일 ZnO 나노선 inverter 논리소자

논 문
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Single ZnO Nanowire Inverter Logic Circuits on Flexible Plastic Substrates

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Abstract - In this study, inverter logic circuits on a plastic substrate are built with two top-gate FETs in series on a single ZnO nanowire. The voltage transfer characteristics of the ZnO nanowire-based inverter logic circuit exhibit a clear inverting operation. The logic swing, gain and transition width of the inverter logic circuit is about 90 %, 1.03 and 1.2 V, respectively. The result of mechanical bending cycles of the inverter logic circuit on a plastic substrate shows that the stable performance is maintained even after many hundreds of bending cycles.

Key Words : ZnO, Naowires, Logic circuits, Inverter

1. Introduction

Semiconducting nanowires have attracted a great deal of attention as potential candidates for various nanodevices including field-effect transistors (FETs) [1]-[2] photodetectors [3], biochemical sensors [4], memory devices [5], and thin-film transistors (TFTs) [6]. In particular, the application of semiconducting nanowires to electronic devices has been intensively researched due to the various advantages of nanowires, such as their good transportation of charge carriers and high crystalline quality [7]-[8]. Recently, logic circuits using semiconducting nanowires and nanotubes have been reported [9]-[10]. In the logic circuits, resistors are utilized as a load to pull up an output of the logic circuits. However, a large area is required to fabricate the resistor of high resistance on a chip. To solve this problem, the FET should be utilized as an active load instead of the resistor.

ZnO nanowires are more attractive than other semiconducting nanowires due to their simple synthetic procedure, high crystalline quality, and good electrical characteristics, which are favorable for electronics [4], [11]-[12]. Recently, the enhancement of the electron mobility (1000~4000 cm2/V • s) by depositing a polymer or a SiO2/Si3N4 layer on the surface of the ZnO nanowires was reported by W. I. Park et al. [13] and P. -C. Chang et al. [14]. The passivation of the ZnO nanowires by a polymer or a SiO2/Si3N4 suppresses the interaction between the surface of the ZnO nanowires and molecular species and the carrier trapping or scattering caused by surface defects. In addition, a rational synthetic method of p-type ZnO nanowires has been reported by B. Xiang et al. [15]. P-type ZnO nanowires were synthesized by a thermal chemical vapor deposition (CVD) method using P2O5 powders as dopants. These studies of high performance and p-type doping of the ZnO nanowires facilitate the application of the ZnO nanowires to nano-electronic devices.

In this study, a ZnO nanowire-based inverter logic circuit was built using two top-gate ZnO nanowire FETs. The top-gate FETs were utilized as a driver as well as an active load of the inverter logic circuits. The electrical characteristics of two top-gate FETs were evaluated and the output characteristics of the inverter logic circuits were estimated.

2. Experimental

A inverter logic circuit was fabricated by forming two top-gate FETs in series on a single ZnO nanowire. For the fabrication of the two top-gate FETs, ZnO nanowires synthesized by a thermal CVD method [16] were first dispersed on a plastic substrate. A common source and two drain patterns were formed on the central and end parts of a selected single ZnO nanowire by

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photolithography, metal deposition, and lift-off processes. Ti (80 nm) and Au (20nm) metals deposited by an e-beam evaporator were utilized as the common source and two drain metal electrodes. A 20-nm-thick Al2O3 layer was deposited conformally on the whole structure by an atomic layer deposition (ALD) [17]-[18]. To form two top-gate electrodes, Al (100 nm) metal was deposited after patterning of two gate regions, and then the Al metal was lifted off. For electrical contact, the Al2O3 layer on the source and drain electrodes was etched by using hot phosphoric acid (H3PO4) at 55 ℃. The optical microscopy image and the circuit diagram for the ZnO nanowire-based inverter logic circuit are illustrated in Fig. 1. The distance between the common source and drain electrodes is 10 ㎛ and the widths of source and gate electrodes are 10 and 5 ㎛, respectively.

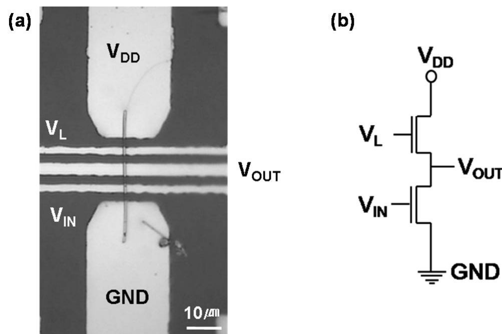

Fig. 1 (a) Optical microscopy image and (b) circuit diagram of the ZnO nanowire - based inverter logic circuit.

3. Results and discussions

The IDS-VGS transfer characteristics of the load FET and the driver FET are shown in Fig. 2. The load FET is constructed between the power supply voltage (VDD) and the output voltage (VOUT) electrodes and the driver FET is constructed between the GND and the VOUT electrodes as well. The IDS increases at first and then saturates as the VGS increases from -0.8 to 5 V, and is depleted in the VGS range from -5 to -0.8 V. The threshold voltages of the load FET and the driver FET are -0.8 and -0.7 V, respectively.

These characteristics reveal that these FETs are nearly identical to n-type depletion mode ones. The Ion/Ioff ratios of these FETs are as high as 107, and the maximum values of transconductance for the load FET and the driver FET are 112 and 98 nS, respectively. The oxide capacitance is estimated to be 5.9 fF from the equation [19],

$$C_{ox} = 2\pi\epsilon_r\epsilon_0 L_g/\ln(r_g/r_{nw}) \quad (1)$$

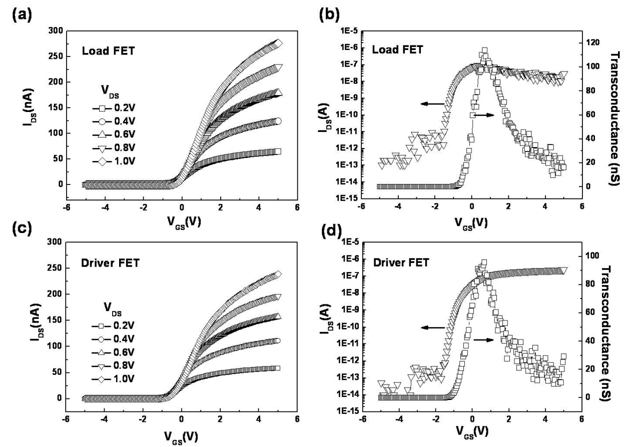

Fig. 2 IDS-VGS transfer characteristics of the two top-gate ZnO nanowire FETs ((a-b) for the load FET, and (c-d) for the driver FET) in the inverter logic circuit.

where ϵ_r is the dielectric constant of Al2O3 (8.4), L_g the gate length (5 ㎛), r_g the outer radius of the Al2O3-coated nanowire (95 nm), and rnw the radius of the nanowire (75 nm). The field-effect mobilities for the load FET and the driver FET are estimated to be 16.5 and 15.3 cm2/V • s on the basis of the equation [19],

$$\mu_{FE} = L_c L_g g_m r_g / C_{ox} V_{DS} r_{nw} \quad (2)$$

where L_c is the channel length between source and drain electrodes (10 ㎛). The details for this equation is described in our previous paper [20].

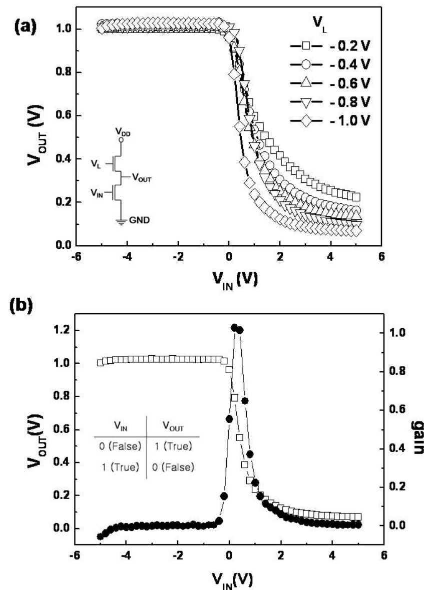

Fig. 3 (a) Voltage transfer characteristics of the ZnO nanowire-based inverter logic circuit as a function of load gate voltage, and (b) the representative voltage transfer characteristic and voltage gain at VL=-1 V.

Fig. 3(a) shows the voltage transfer characteristics of the ZnO nanowire-based inverter logic circuit with an active load of the n-type depletion mode FET. The output voltage in Fig. 3(a) exhibits a high state at the input voltage of -5 V, and a low state at the input voltage of 5 V. This behavior indicates the clear inverting operation of the output voltage for the input voltage. When the input voltage is in a low state, the channel of the driver FET is fully depleted so that the output voltage goes VDD. When the input voltage is in a high state, the channel of the driver FET is accumulated and the resulting output voltage switches from VDD to GND. As the input voltage increases from -5 V to 5 V, the output voltage decreases from 1 V to about 0.1 V under VDD = 1 V and VL = -1 V. For the clear inverting operation for the low state of the output voltage, the negative gate voltage VL is required for the active load in order to achieve a large resistance.

When the negative voltage is applied to the gate of the load FET, the resistance in the active load becomes large, and the output voltage in low state decreases. As the gate voltage of the active load goes negative, the inverting operation becomes more obvious. The maximum value of voltage gain (($(\Delta V_{OUT}/\Delta V_{IN})_{MAX}$) is estimated to be 1.03, which is higher than the unity, and the logic swing and the transition width is measured to be about 90 % and 1.2 V at VL = -1.0 V, respectively.

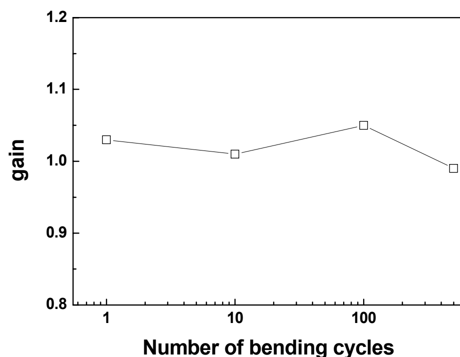

Fig. 4 The voltage gain of the ZnO nanowire-based inverter logic circuit after many hundreds of bending cycles with a strain of 1.02 %.

Mechanical bendability with stable performance is an important factor in flexible electronics. To evaluate the endurance of bendability, some bending tests are performed 500 times. Fig. 4 shows the variation of the gain of our ZnO nanowire-based inverter circuit. The flexible substrate was bent under a strain of 1.02 %. The strain value described in this work was obtained by [15]-[16], [21],

$$Strain = 100 \times \frac{d_{substrate} \times r_{ZnO}}{2 \times R_c} \qquad (3)$$

where R_c is the radius of curvature of the bent PES substrate (1.3 cm), and the thickness of the PES substrate is 200 ㎛. As shown in Fig. 4, the performance of the ZnO nanowire-based inverter logic circuit is maintained even after many hundreds of bending cycles.

4. Summary

The Cu_2O film-based photodetector is successfully fabricated on a glass substrate by a spin-coating process. Under the illumination of the 325nm wavelength light, the photocurrent efficiency of the Cu_2O film in air at room temperature is estimated to be about $1.8x10^5$ μA/W at a bias voltage of 2.5 V. The transparent Cu_2O film easily formed by a spin-coating technique is a promising material in application of UV photodetectors.

4. Conclusion

An inverter logic circuit on a plastic substrate is constructed with two top-gate FETs in series on a single ZnO nanowire. The threshold voltages of the load FET and the driver FET are -0.8 and -0.7 V, respectively, and their transconductances are 112 and 98 nS, respectively. The logic swing, gain and transition width of the inverter logic circuit is estimated to be about 90 %, 1.03 and 1.2 V, respectively. The bending endurance test result shows that the stable performance is maintained even after many hundreds of bending cycles.

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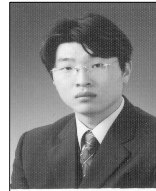

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