JPE 10-1-6

A Fault-Tolerant Control Strategy for Cascaded H-Bridge Multilevel Rectifiers

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Abstract

Reliability is an important issue in cascaded H-bridge converters (CHB converters) because they use a high number of power semiconductors. A faulty power cell in a CHB converter can potentially lead to expensive downtime and great losses on the consumer side. With a fault-tolerant control strategy, operation can continue with the undamaged cells; thus increasing the reliability of the system. In this paper, the operating principles and the control method for a CHB multilevel rectifier are introduced. The influence of various faults on the CHB converter is investigated. The method of fault diagnosis and the bypassing of failed cells are explained. A fault-tolerant protection strategy is proposed to achieve redundancy in the CHB rectifier. The redundant H-bridge concept helps to deal with device failures and to increase system reliability. Simulation results verify the performance of the proposed strategy.

Key Words: Cascaded H-bridge rectifier, Fault diagnosis and protection, Fault-tolerant design, Redundancy and reliability

I. INTRODUCTION

With the advancement of power electronics and the emergence of new multilevel converter topologies, it is possible to work at voltages beyond the level of individual power devices. Multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the rating of the individual power devices [1], [2]. Moreover, the cascaded H-bridge converter (CHB) is the most attractive topology as far as front-end applications are concerned. In fact, it allows both fewer components to be used and a simple layout because of its modular structure. These converters can be used as inverters in AC motor drives, high power conditioning and active power filters [3]–[5]. In addition, they can be utilized as active front-ends or PWM rectifiers [6], [7].

Since several H-bridge converters are required in a CHB multilevel converter, a large number of power switching devices will be used. Each of these devices is a potential failure point, which will reduce the reliability of the system. It is important to maintain normal operation under fault conditions because failed operation of a converter could cause tremendous losses for consumers, especially when the CHB converter is feeding critical loads. It is, therefore, a key issue to design a fault-tolerant system to improve system reliability.

Manuscript received Apr. 6, 2009; revised Nov. 23, 2009
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For a fault-tolerant system, the basic goal is to continue operation in the event of a power failure. Relevant research on fault-tolerant design for multilevel converters focuses mainly on motor drive system. [8], [9] discuss the fault-tolerant solutions for diode-clamped and capacitor-clamped converters, respectively. [10], [11] discuss the operation of a cascaded H-bridge multilevel inverter with faulty cells for the drive system. In the latter, additional switches are used to bypass the faulty cells.

In this paper, a fault-tolerant control strategy for cascaded H-bridge rectifiers is presented. The proposed strategy for the fault-tolerant system is redundancy. In fact, the modularized CHB converter is very suitable for achieving this goal because all H-bridge cells are identical. One H-bridge is added to the CHB converter as a backup to maintain operation even when one of them fails. The redundancy is achieved if we can bypass the H-bridge cell that contains the failed device, so that a cascade failure is prevented and normal operation is maintained. Compared with previous solutions, this strategy saves bypasses and isolated switches and keeps the same input voltage level. The control strategy and fault-tolerant design are explained in detail and confirmed with simulation results.

II. CASCADED H-BRIDGE RECTIFIER

This section describes the structure and control strategy used for the CHB converter. Some background material is provided and the method of control is explained.

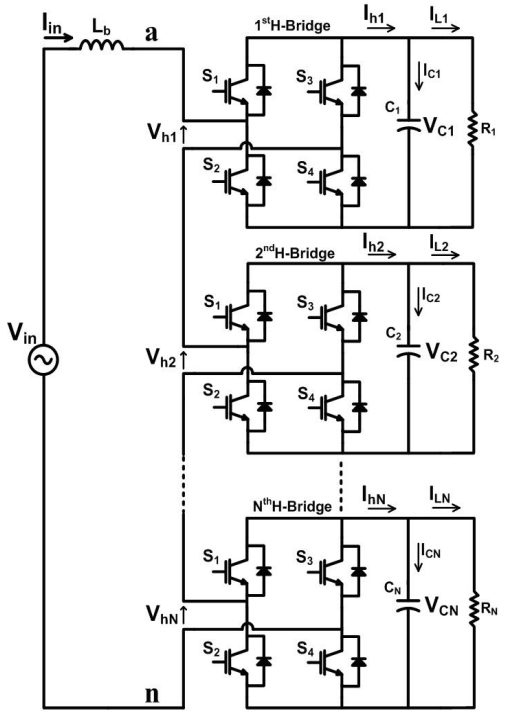


Fig. 1. Bidirectional CHB rectifier with N H-bridge cells.

A. Configuration of cascaded H-bridge rectifier

A CHB converter is the best choice for working in high-voltage and high-power applications due to its extreme modularity, simple physical layout and low losses. As can be seen from Fig. 1, the CHB converter has N H-bridge cells connected in series. Each H-bridge consists of four power switches (with anti-parallel diodes) and a DC bus capacitor. Each capacitor feeds its own load denoted by: R_i $(i = 1, \ldots, N)$.

In Fig. 1, the AC terminal voltage of the rectifier, V_{an}, can be written as follows:

$$V_{an} = V_{h1} + V_{h2} + \cdots + V_{hN} \quad (1)$$

$$V_{hi} = h_i \cdot V_{C_i},\ i = 1, 2, \ldots, N \quad (2)$$

where V_{hi}, V_{Ci}, and h_i are the AC terminal voltage, the capacitor voltage, and the switching function of the i^{th} H-bridge (or cell), respectively. Assuming that $V_{C1} = V_{C2} = \ldots = V_{CN} = V_C$, where V_C is the reference voltage of the DC buses, each cell can generate three voltage levels: $+V_C$, $-V_C$, and zero on the AC side. Therefore, using N H-bridge cells, a maximum of L = 2N+1 different voltage levels are obtained to synthesize V_{an}. Applying the Kirchhoff Voltage Law (KVL) at the input voltage loop yields:

$$V_{in} = V_{an} + L_b \frac{dI_{in}}{dt} \quad (3)$$

where V_{in} is the input voltage, I_{in} is the input current and L_b is the input inductance which is used to shape the input current. Applying the Kirchhoff Current Law (KCL) for each cell leads to:

$$I_{hi} = h_i \cdot I_{in},\ i = 1, \ldots, N \quad (4)$$

where I_{hi} is the current of i^{th} H-bridge and is a function of the input current. The equations (1)–(4) describe a linear time varying system with one input (V_{in}) and N+1 states (V_{C1} to V_{CN} and I_{in}).

B. Control of the cascaded H-bridge converter

The main challenges associated with CHB rectifier control are shaping the input current, controlling the input power factor and keeping the DC link voltages at the desired reference value. In rectification mode, the CHB converter aims to achieve N equal DC voltages across the capacitors (C_1 to C_N). However, this can become difficult if the loads (or converters) attached to the H-bridge cells are not equal, or if the series H-bridges have slightly different characteristics.

In Fig. 2(a), the basic block diagram of the utilized controller is shown [12]. This diagram consists of analog and digital controllers. The analog controller generates the pulse width modulated (PWM) signal, Q, and the digital controller determines the appropriate switching functions h_1 to h_N. The digital controller also generates a synchronized square-wave signal $\{V'_{in}(\varphi)$ in Fig. 2(a)$\}$ to control both the active and reactive powers.

Fig. 2(b) shows the basic block diagram of an analog controller. This controller is intended to shape the input current and regulate the total voltage of the primary DC links. The controller has two control loops: the inner current loop and the outer voltage loop. The voltage loop contains a PI controller to regulate the total voltage of the DC buses to the reference value, i.e. $\sum V_{Ci} = N \cdot V_C$. In the classical methods, the output of the PI regulator is multiplied by a sample of the input voltage to generate a sinusoidal reference current, ${I_{in}}^*$. Here, the digital controller generates a square wave alternative signal, ${V'}_{in}$, from the input voltage which is in the opposite direction of V_{in}. The square wave signal has the same frequency as the input voltage and its phase, i.e. $\pi - \theta$, is adjusted by the digital controller (see Fig. 2(b)). This signal is then filtered by a low-pass Butterworth filter and multiplied by the output of the voltage regulator. Using this method, a pure sinusoidal reference is generated, even in environments polluted with noise and harmonics. Additionally, the phase of the input current, φ, and the power factor are controlled, and the gain of the voltage loop becomes independent from the input voltage variations. After generating the reference current ${I_{in}}^*$, the inner current loop programs the input current I_{in} to follow the reference signal by PWM control (or by generating a Q signal).

The digital controller determines the appropriate switching functions, h_1 to h_N, for the series-connected H-bridges. Each switching function h_i $(i = 1, \ldots, N)$ corresponds to the four operating modes: "0", "+1", "-1", and PWM. The switching functions are determined by the digital controller and are applied to the H-bridge cells. The operating mode "0" corresponds to the conduction of the bottom switches (S_2, S_4) or zero voltage at the AC terminal. It is also possible to alternate between the conduction of the top and bottom switches in mode "0" to evenly spread the switching stress among the switches. In modes "+1" and "$-$1" the diagonal switches (S_1, S_4) and (S_2, S_3) are turned on, respectively. In mode "+1" the corresponding AC terminal voltage is "$+V_C$", and in

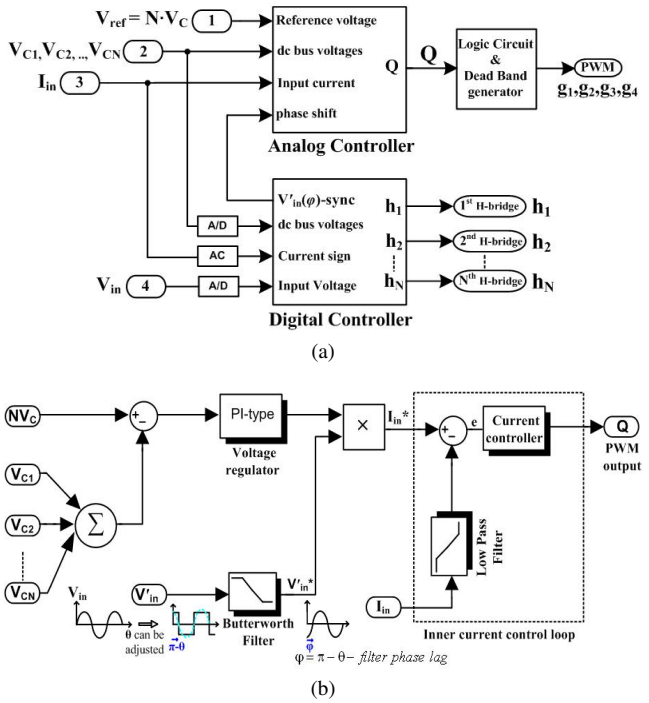


Fig. 2. Block diagram of the CHB controller: (a) main controller, (b) analog controller.

mode "-1" it is "$-V_C$". In PWM mode, the corresponding cell alternates between modes "0" and "+1" if the input voltage is positive; otherwise it alternates between modes "0" and "-1". The gate signals in PWM mode are determined by Q and the sign of the input voltage [12].

It is worth noting that all of the gate signals in the CHB converter are modified so that during the conduction of an anti-parallel diode, the respective switch is off. This effect can reduce the losses of the driver circuits and the possibility of DC-bus short circuits. The second point is achieved by preventing the complementary commands for switches in the same leg. The modified gate signals are applied to the H-bridge drivers as follows:

$$\begin{aligned} g_{1mod} &= g_1 \bar{S}_i S_v \\ g_{2mod} &= g_2 S_i \\ g_{3mod} &= g_3 S_i \bar{S}_v \\ g_{4mod} &= g_4 \bar{S}_i \end{aligned} \tag{5}$$

where S_v is the sign of input voltage and it is one if the input voltage is positive; otherwise it is zero. S_i is the sign of the input current I_{in}.

C. Definition of voltage regions and control rules

To take advantage of both low frequency (stepped modulation) and high frequency (PWM) modulation techniques, we employ the hybrid modulation method as shown in Fig. 3. In this method, the input voltage V_{in} is divided into equal sections with the scale of V_C (V_C is the reference of the DC link voltages). Now we define the voltage region K as follows:

$$(K-1)\cdot V_C < |V_{in}| < K \cdot V_C,\ K = 1, \ldots, N \tag{6}$$

$$N_{min} = ceil(V_m/V_C) \tag{7}$$

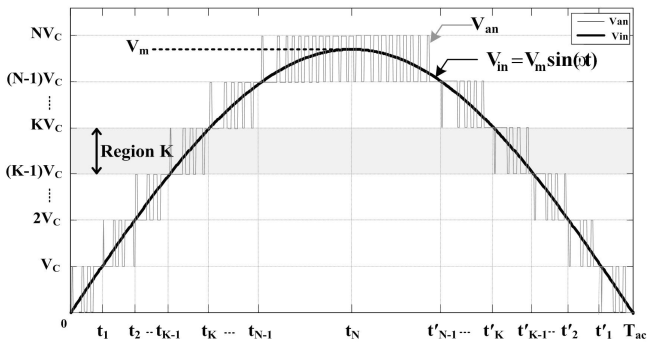


Fig. 3. Definition of voltage regions for $K = 1, \ldots, N$.

Region K is the voltage interval in which the magnitude of the input voltage, $|V_{in}|$, lies between $(K-1)V_C$ and KV_C. The minimum number of cells to synthesize the multilevel waveform, V_{an}, is derived from the following equation:

$$N_{min} = ceil(V_{in}/V_C) \tag{8}$$

where $ceil(A)$ is the closest integer greater than A, and V_m is the peak input voltage.

In Fig. 3, T_{ac} is the mains half-cycle, t_K and t'_K ($K = 1, \ldots, N-1$) correspond to a change of voltage region (where $V_{in} = KV_C$), and t_N are equal to $T_{ac}/2$.

The following benefits can be achieved by utilizing the hybrid modulation technique:

- Considerable reduction in size and volume of the input inductor L_b; because it will not need to tolerate voltages more than V_C.
- Lower current ripple due to multilevel operation (or a reduction in the THD value).
- Lower EMI at the input side because of a lower dv/dt.
- Low switching loss because at each time interval only one cell operates in HF mode.

The digital controller performs the control algorithm to maintain a voltage balance across the capacitors, while the analog controller regulates the sum of the DC link voltages to $N \cdot V_C$. The proposed control rules defined below, aim to synthesize the waveform shown in Fig. 3 and to maintain a voltage balance across the DC link capacitors.

1) If $V_{in} > 0$, $I_{in} > 0$ and the voltage region is K, then the $(K-1)$ cells with the lowest DC bus voltage are chosen to be charged in mode "$+1$", the K^{th} cell in PWM mode and the rest in mode "0".
2) If $V_{in} > 0$, $I_{in} < 0$ and the voltage region is K, then the $(K-1)$ cells with the highest DC bus voltage are chosen to be discharged in mode "$+1$", the K^{th} cell in PWM mode and the rest in mode "0".
3) If $V_{in} < 0$, $I_{in} > 0$ and the voltage region is K, then the $(K-1)$ cells with the highest DC bus voltage are chosen to be discharged in mode "-1", the K^{th} cell in PWM mode and the rest in mode "0".
4) If $V_{in} < 0$, $I_{in} < 0$ and the voltage region is K, then the $(K-1)$ cells with the lowest DC bus voltage are chosen to be charged in mode "-1", the K^{th} cell in PWM mode and the rest in mode "0".

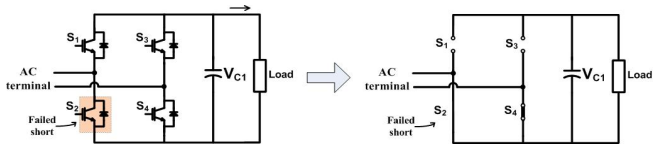


Fig. 4. Bypassing an H-bridge cell when a switch fails short.

To perform the above rules, the digital controller takes the voltage and current samples with the sampling frequency f_o ($f_o < f_{PWM}$). Then, the region of the input voltage, K, is updated according to (6), the control algorithm is performed and the appropriate switching functions, h_1 to h_N, are determined. The switching functions are applied to the H-bridge cells and the operating modes are performed. This procedure is repeated in the following sampling periods. As a result, the voltage of the DC buses is controlled by adjusting the average current fed to the H-bridge cells, over the mains half-cycle.

III. Redundancy and Reliability

To analyze the reliability of a CHB converter, it is supposed that the CHB converter contains N cells and can not tolerate any failures; then, if the probability of a single cell functioning properly during a time interval is R, then the probability that all N cells that will function properly during the same time interval would be R^N because the CHB converter is considered as a series association of H-bridges. According to [13], for the case of m tolerated cells, the reliability function of the CHB converter is derived as:

$$R_m = \sum_{i=0}^{m} \frac{(N+m)!}{(N+m-i)!i!} \times R^{(N+m-i)} \times (1-R)^i \quad (9)$$

where $(N+m)$ is the number of cells in the CHB structure, m is number of tolerated cells (redundant cells) and R_m is total reliability of the system. A numerical reliability example of a CHB is illustrated in Table I. Suppose that the CHB converter in Table I has a cell reliability R = 98% and that it contains N = 5 cells. As can be seen, with one tolerated cell, the reliability of the CHB converter can increase from 90.4% to 99.4%; therefore, a fault diagnosis and fault reconfiguration (bypass) system can improve the reliability of the whole system.

TABLE I
Numerical example of N = 5 CHB converter with 98% reliability in each cell

Number of tolerated cells	Reliability function	Reliability (percentage)
$m = 0(N\text{cells})$	$R_0 = R^N$	90.39%
$m = 1(N+1\text{cells})$	$R_1 = R^{N+1} + (N+1)(1-R)R^N$	99.43%
$m = 2(N+2\text{cells})$	$R_2 = R^{N+2} + (N+2)(1-R)$ $R^{N+1} + 0.5 \cdot (N+2)(N+1)$ $(1-R)^2 R^N$	99.97%

A. Investigation of different fault situations

Commercial IGBTs can be categorized into plastic-pack (module type) and press-pack in terms of packaging. Plastic-pack IGBTs have single-sided cooling and act as open-circuits in failure mode with the possibility of case rupture and an arc flash event [14]. Press-pack IGBTs act as short-circuits in the event of a failure. When the chip fails, the silicon is metallurgically alloyed with an optimized contact partner and a permanent conductive path is formed through the chip [15]. Devices operating in this so called "circuit failure mode (SCFM)" will remain in a low impedance state under all possible load conditions for a certain period of time. Reference [16] calculates analytically the short circuit failure mode endurance and estimates an appropriate service interval, after which the failed devices have to be removed and replaced with new ones.

In this paper, it is assumed that the semiconductor devices are based on press-pack technology and have SCFM capability. Additionally, open-circuit failure is not studied. Only short circuit failure is investigated, since our goal is to show how to improve system reliability by using additional features in the control system.

When one of the power semiconductor devices fails, the key to achieving redundancy is to bypass the failed switch. In fact, we use the failed state of a device to bypass the corresponding H-bridge without any additional bypass power switch. This requires that the failed H-bridge DC side is opened and that the AC side is shorted [17]. To achieve this goal, if one top/bottom switch fails another top/bottom switch is turned on and the other two complementary switches are turned off. Fig. 4 shows the principle behind bypassing the failed H-bridge.

In the above strategy, sensing a device short and bypassing the failed H-bridge in time and correctly are very important to prevent failure propagation. Therefore, to diagnose the faults, an arbitrary H-bridge cell (from N H-bridge cells) is investigated under different operating conditions. For this study, it is assumed that only one switch fails short, during operation. Figures 5 to 8 illustrate different fault-free conditions and Tables II to V show the corresponding AC terminal voltages under faulty conditions.

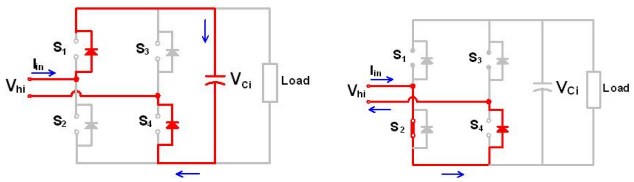
Case 1: $V_{in} > 0$ and $I_{in} > 0$
(cf. Fig. 5 and Table II)

Case 2: $V_{in} > 0$ and $I_{in} < 0$
(cf. Fig. 6 and Table III)

Case 3: $V_{in} < 0$ and $I_{in} > 0$
(cf. Fig. 7 and Table IV)

Case 4: $V_{in} < 0$ and $I_{in} < 0$
(cf. Fig. 8 and Table V)

We study case 1 which has been evaluated in Table II. If the switch S_1 fails (e.g., due to a fault in the driver of the S_1 switch), the operating mode "0" will generate a short circuit condition through S_2 and the DC bus capacitor. This fault can be detected by the IGBT fault protection schemes, described in most of the up to date literature [18], [19], with the V_{ce} sensing through a desaturation diode. Fortunately, most of the recent IGBT drivers provide this protection feature (see, e.g., Semikron IGBT/MOSFET drivers). In fact, if the S_2 driver



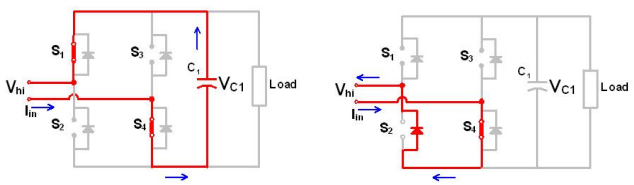
(a) Mode: $+1$ (b) Mode: 0

Fig. 5. Switching state in an H-bride cell when $V_{in} > 0$ and $I_{in} > 0$ (case 1).

TABLE II
AC TERMINAL VOLTAGE OF AN H-BRIDGE CELL WHEN $V_{in} > 0$, $I_{in} > 0$, AND A SWITCH FAILS SHORT

Failed switch	Operating mode	State of the switches (or diodes)				AC ter. Volt.	Fault type
		D_1	S_2	S_3	D_4		
S_1	"+1"	short	0	0	1	V_C	—
	"0"	short	1	0	1	—	SC[a]
S_2	"+1"	0	short	0	1	0	ML[b]
	"0"	0	short	0	1	0	—
S_3	"+1"	1	0	short	0	0	ML
	"0"	0	1	short	0	$-V_C$	ML
S_4	"+1"	1	0	0	short	V_C	—
	"0"	0	1	0	short	0	—

[a] SC denotes a Short Circuit condition in the DC buses.
[b] ML denotes a Missed Level condition at the cell AC terminal voltage.



(a) Mode: +1 (b) Mode: 0

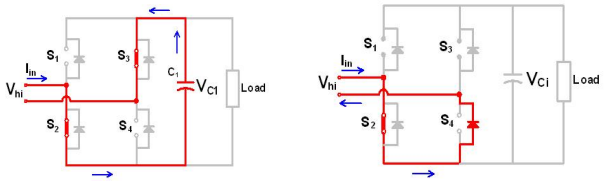
Fig. 6. Switching state in an H-bride cell when $V_{in} > 0$ and $I_{in} < 0$ (case 2).

TABLE III
AC TERMINAL VOLTAGE OF AN H-BRIDGE CELL WHEN $V_{in} > 0$, $I_{in} < 0$, AND A SWITCH FAILS SHORT

Failed switch	Operating mode	State of the switches (or diodes)				AC ter. Volt.	Fault type
		D_1	S_2	S_3	D_4		
S_1	"+1"	short	0	0	1	V_C	—
	"0"	short	0	0	1	V_C	ML
S_2	"+1"	1	short	0	1	—	SC
	"0"	0	short	0	1	0	—
S_3	"+1"	1	0	short	1	—	SC
	"0"	0	1	short	1	—	SC
S_4	"+1"	1	0	0	short	V_C	—
	"0"	0	1	0	short	0	—

senses that the voltage across the IGBT (at the ON state) is greater than its typical value, the short circuit condition is detected, the respective driver output is slowly turned off and the fault output is immediately activated. The fault output provides an interrupt to the protection algorithm, in order to make a decision and bypass the failed H-bridge cell.

If S_4 fails, it will affect neither the "0" nor the "+1" operating modes. However, when the operating condition changes, it can cause abnormal results. If S_2 or S_3 fails, the desired AC terminal voltage ($+V_C$ in mode "+1") will not develop (ML-type fault). In this situation, the voltage of the input inductor $V_{Lb} = V_m \sin(\omega t) - V_{an}$ becomes positive and the inductor current start to increase due to the positive current slope. Additionally, the capacitor of the failed cell is not charged and its voltage starts to decrease. This mechanism is repeated in the next sampling periods, therefore, the voltage of the healthy

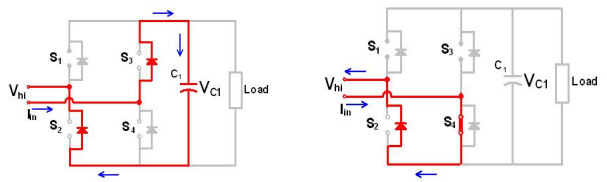


(a) Mode: -1 (b) Mode: 0

Fig. 7. Switching state in an H-bride cell when $V_{in} < 0$ and $I_{in} > 0$ (case 3).

TABLE IV
AC TERMINAL VOLTAGE OF AN H-BRIDGE CELL WHEN $V_{in} < 0$, $I_{in} > 0$, AND A SWITCH FAILS SHORT

Failed switch	Operating mode	State of the switches (or diodes)				AC ter. Volt.	Fault type
		D_1	S_2	S_3	D_4		
S_1	"+1"	short	1	1	0	—	SC
	"0"	short	1	0	1	—	SC
S_2	"+1"	0	short	1	0	$-V_C$	—
	"0"	0	short	0	1	0	—
S_3	"+1"	0	1	short	0	$-V_C$	—
	"0"	0	1	short	0	$-V_C$	ML
S_4	"+1"	0	1	1	short	—	SC
	"0"	0	1	0	short	0	—

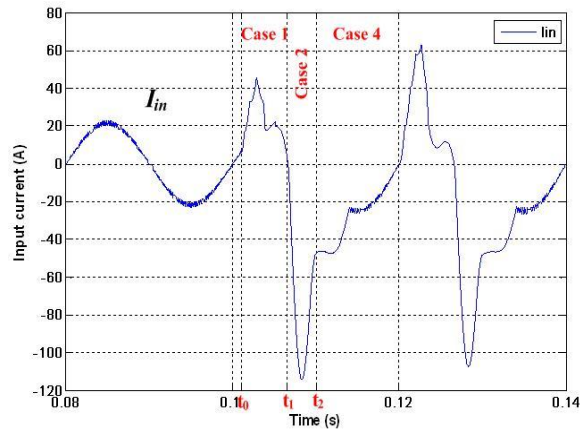


(a) Mode: -1 (b) Mode: 0

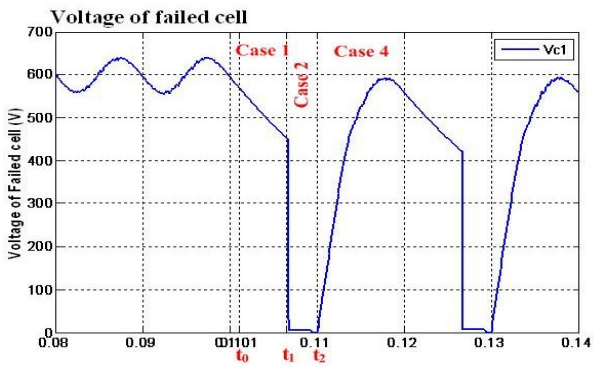
Fig. 8. Switching state in an H-bride cell when $V_{in} < 0$ and $I_{in} < 0$.

TABLE V
AC TERMINAL VOLTAGE OF AN H-BRIDGE CELL WHEN $V_{in} < 0$, $I_{in} > 0$, AND A SWITCH FAILS SHORT

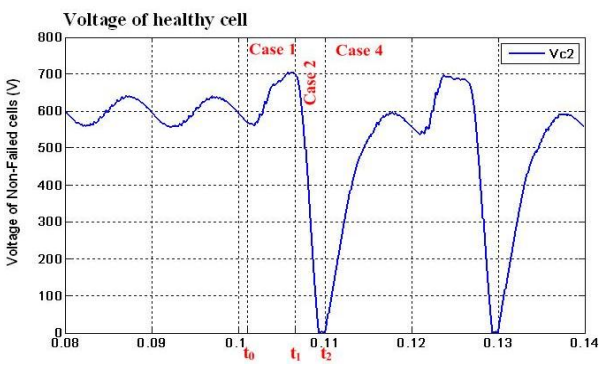
Failed switch	Operating mode	State of the switches (or diodes)				AC ter. Volt.	Fault type
		D_1	S_2	S_3	D_4		
S_1	"+1"	short	0	1	0	0	ML
	"0"	short	0	0	1	V_C	ML
S_2	"+1"	0	short	1	0	$-V_C$	—
	"0"	0	short	0	1	0	—
S_3	"+1"	0	1	short	0	0	—
	"0"	0	1	short	1	—	SC
S_4	"+1"	0	1	0	short	0	ML
	"0"	0	1	0	short	0	—



(a)



(b)



(c)

Fig. 9. Evaluation of switch failure in the CHB converter (S_2 fails short at t_0), (a) input current waveform, (b) voltage of failed cell V_{C1}, (c) voltage of healthy cells (only V_{C2} is shown).

cells start to increase temporarily (in contrast with the failed cell) to satisfy the condition $\sum V_{Ci} = NV_C$.

To verify the above discussion, the failure of a power switch in a CHB converter has been simulated. It is assumed that the CHB converter operates correctly until t_0 = 0.101s, when switch S_2 of cell #1 fails. Fig. 9 shows the corresponding input current I_{in}, the voltage of the failed cell V_{C1} and the voltage of the healthy cells, e.g. V_{C2}.

As can be seen from Fig. 9(a), when switch S_2 fails (at t_0) the current amplitude increases and the voltage of the failed cell decreases. This situation is valid until $t = t_1$. At $t = t_1$, the current sign changes and according to Table III, the failed switch S_2 generates a short circuit (SC) condition through S_1 and the DC link capacitor C_1. Then, the voltage of the first cell decreases sharply and the control function is no longer valid. At $t = t_2$ (t_2 = 0.11s), the voltage sign becomes negative, and according to Table IV, the failed switch does not have any effect up to t = 0.12s. In the time interval (t_2, 0.12s) the CHB controller tries to restore the initial condition.

B. Fault diagnosis and protection strategy

The proposed method's ability to diagnose a faulty situation is based on the behavior of the input current and the DC link voltages in fault situations. An evaluation of all the ML-type faults in Tables II to V shows that if a switch fails, the input current will increase abruptly and exceed the marginal limits. In fact, if the current direction is positive, an abnormal positive voltage will be applied to the input inductor ($di/dt \uparrow$), and if the current direction is negative, an abnormal negative voltage will be applied to the inductor ($di/dt \downarrow$). Furthermore, the voltage of the failed cell will start to decrease in comparison with the average voltage and the voltage of the healthy cells will start to increase.

As a result, we can diagnose a faulty cell according to a sudden increase in the current amplitude and a voltage decrease in only one cell. In this method, only the sampled signals for the control unit, V_{C1} to V_{CN}, and I_{in} are enough for the protection algorithm. As a result, it is a cost free solution. After finding the faulty cell, the faulty switch will be diagnosed in order to take the proper action. In SC-type faults, the respective switch driver is automatically turned off and the fault output is immediately activated. This fault along with the predetermined SC conditions in Tables II to V reveals which switch has failed.

When a ML-type fault is detected, depending on the input voltage and current signs, the failed switch is diagnosed. For example, in cases 2 and 3 only one switch could generate the ML-type fault, so it is simple to detect. But, in cases 1 and 4 two switches could generate the ML-type faults. In case 1, switch S_3 is permanently off while switch S_2 has switching actions. So, the failure probability of S_2 is much more than S_3. Similarly, in case 4, the failure probability of S_4 is much more than S_1. In these cases, the protection circuit will turn on the bottom switches S_2 and S_4. However, if the failed switch is S_1 or S_3, it will cause a SC condition and a SC fault is generated. The SC fault is then used to correct the previous decision.

After the fault is detected and the failure location is diagnosed, the protection algorithm should bypass the failed cell using the strategy shown in Fig. 4 and inform the main controller to operate with N cells instead of $N+1$ cells. Since voltage balancing control has been implemented by a digital controller, this adaptation is easily done by a software program and the reference voltage is changed from $(N+1) \cdot VC$ to $N \cdot V_C$.

Based on the above explanations, the algorithm shown in Fig. 10 is proposed to detect a faulty cell, to bypass it and to continue operation with N cells.

The following points about the protection algorithm are worth noting:

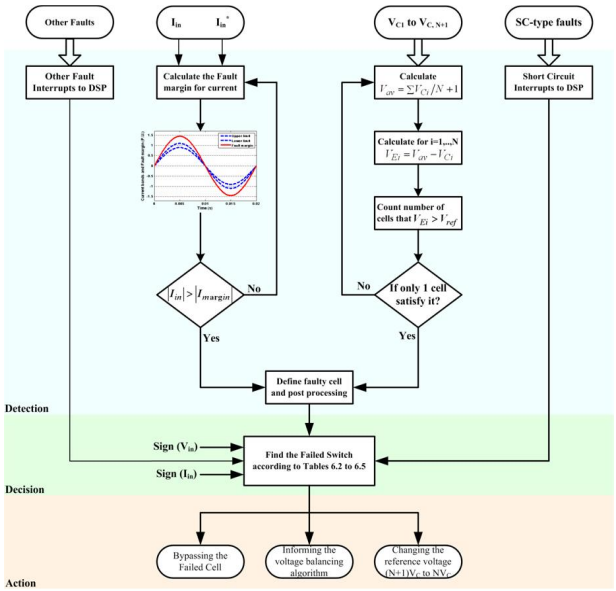


Fig. 10. Proposed protection algorithm to achieve a fault-tolerant design in a CHB rectifier with 2N+1 voltage levels.

- Part of the detection algorithm can be implemented by analog circuits.
- Post processing of faults is necessary to avoid incorrect decisions.
- In the above algorithm, it is assumed that simultaneous faults don't occur.
- Other faults such as over current and open circuit faults are also evaluated to avoid abnormal decisions.

IV. Simulation Results

To verify the performance of the protection algorithm, two different fault cases have been investigated for a CHB converter with N = 5+1 cells (where m = 1 cell is used as a backup). The peak $Ph-N$ input voltage is 2700 V, the reference voltage for the DC buses is V_C = 600 V and the nominal load power for each cell is 5 kW. In the first investigation, switch S_2 of cell #1 fails and a ML-type fault is generated (case 1). In the second study, switch S_4 of cell #1 fails and a SC-type fault is generated (case 3, where the input current leads the input voltage by the angle $\pi/4$). The computer simulations are carried out using the MATLAB/SIMULINK program and the results are shown in Fig. 11 and 12.

In the above simulations, only the voltage waveforms of two cells (V_{C1} and V_{C2}) have been shown. The behavior of the other cells will be same as V_{C2}. As it can be seen, the CHB converter, without the protection algorithm, will lose the control action and may lead to the failure of more switches. However, when the protection circuit is applied, the faulty situation is immediately detected and the failed cell is bypassed by an appropriate action. After bypassing the failed cell, the remaining cells will continue their operation. It can be seen that the input current is sinusoidal and in phase with the input voltage, and that the number of voltage levels remains constant (L = 11-level) before and after applying the protection algorithm. Also, the DC link capacitors closely follow the

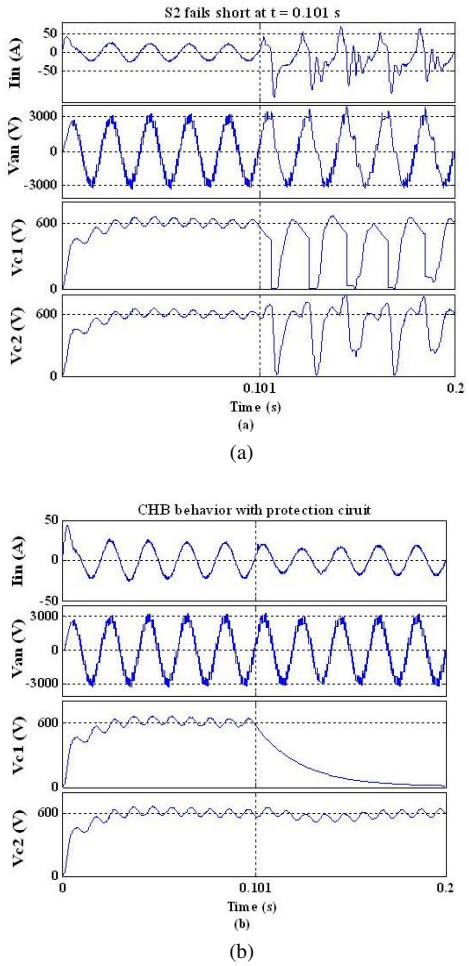


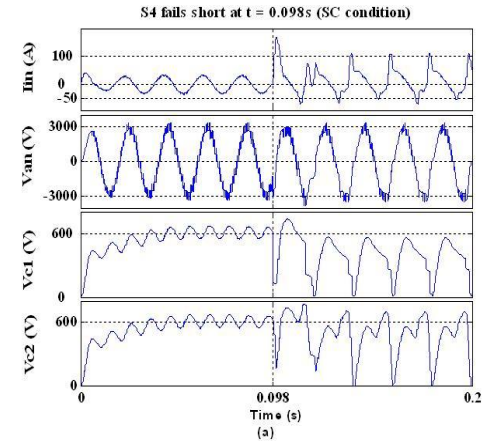
Fig. 11. A ML-type failure at cell #1, (a) before, and (b) after applying the protection circuit.

reference value V_C = 600 V, which confirms the validity and the effectiveness of the control method for CHB rectifiers.

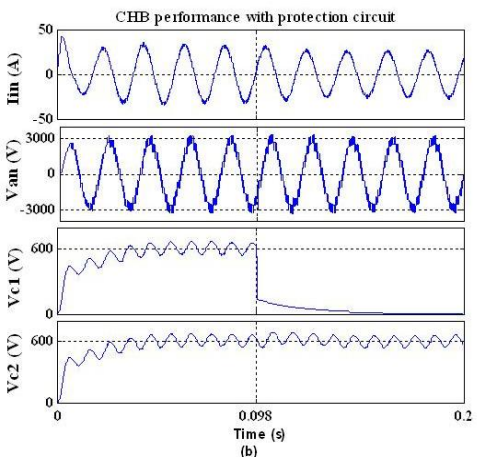
When an H-bridge cell is added to the CHB structure to design a fault-tolerant system and to increase system reliability, two other benefits are also achieved. First, the capability to handle over voltages and swells is improved. By using an additional cell, the CHB converter will be able to handle voltage levels as high as $(N+1)\cdot V_C$ instead of $N\cdot V_C$. Second, the safe operating area for different cells increases. This means that the CHB controller would be able to maintain a voltage balance among the CHB cells, even cells feeding very different loads (e.g., one cell can have no load, while the other feeds a very large load) [12].

V. Conclusions

In this paper, a fault detection and reconfiguration technique for CHB converters was developed. An H-bridge cell was added to the CHB rectifier to achieve redundancy and a fault-tolerant design. The added cell improves the converter performance against voltage surges, enhances system stability and increases system reliability. The system faults were divided into SC and ML-type faults, where SC faults can be detected by the desaturation method (a standard feature of driver ICs)



(a)



(b)

Fig. 12. An SC-type failure at cell #1, (a) before, and (b) after applying the protection circuit.

and the rest by the proposed algorithm. The presented fault-tolerant algorithm, detects switch failures, diagnoses the fault location, bypasses the faulty cell and reorganizes the CHB converter with the remaining cells. The simulation results confirmed that the proposed redundancy and diagnostic mechanism can be applied to CHB converters. The proposed method does not need any additional sensors since it uses the available capacity of digital controllers. The extra cost and size (due to additional H-bridges) is relatively small in comparison with the increased reliability and system performance.

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