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DSP Based Series-Parallel Connected Two Full-Bridge DC-DC Converter with Interleaving Output Current Sharing

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Abstract

Input-series-output-parallel (ISOP) connected DC-DC converters enable low voltage rating switches to be used in high voltage input applications. In this paper, a DSP is adopted to generate digital phase-shifted PWM signals and to fulfill the closed-loop control function for ISOP connected two full-bridge DC-DC converters. Moreover, a stable output current sharing control strategy is proposed for the system, with which equal sharing of the input voltage and the load current can be achieved without any input voltage control loops. Based on small signal analysis with the state space average method, a loop gain design with the proposed scheme is made. Compared with the conventional IVS scheme, the proposed strategy leads to simplification of the output voltage regulator design and better static and dynamic responses. The effectiveness of the proposed control strategy is verified by the simulation and experimental results of an ISOP system made up of two full-bridge DC-DC converters.

Key Words: Current sharing, Digital control, Input-series and output-parallel, Modular DC/DC converters, Phase-shifted full-bridge, Voltage sharing

I. INTRODUCTION

A phase-shifted full-bridge (PSFB) DC-DC converter permits all switching devices to operate under zero-voltage switching (ZVS) by using parasitic parameters such as leakage inductance and junction capacitance to achieve resonant switching. But under high input voltages, the switches have to withstand high voltage stress with the conventional PS-full-bridge StateDC-DC topologies. Three-level FB PS-PWM DC-DC converters enable low-voltage rating switches to be used under high-voltage input applications. However, system reliability can not be guaranteed for a large quantity of diodes or flying capacitors [1],[2].

The input-series output-parallel (ISOP) configuration consists of several modular DC-DC converters connected in series at the input and in parallel at the output, enabling the use of high switching frequency metal oxide semiconductor field effect transistors (MOSFETs) with low voltage ratings, which leads to a high power density and a high conversion efficiency [3]. Besides, modular architecture has the advantage of redundant operation capability [4], and therefore, the overall reliability is improved.

Generally, analog PWM controllers are used to implement the control of ISOP connected FB-PS DC-DC converters. However, analog control circuits are complex and lack flexibility. These PWM controllers sometimes need to be synchronized to generate interleaving duty cycles. Besides, the cost of phase shifted PWM controllers is less competitive than digital controllers because each module needs one single controller. Although a digital PS PWM control strategy has been used for one full-bridge converters [5], digital PS PWM generation and control of ISOP connected modules has not been discussed.

To make an ISOP system work normally, the power sharing among the constituent modules should be ensured, and this also implies input voltage sharing (IVS) and output current sharing (OCS). Several control schemes have been proposed in earlier works. Common duty ratio control results in stable operation, but excellent IVS and OCS can only be achieved for modules with well-matched parameters [6],[7]. A charge control scheme with input-voltage feed forward has been implemented for a two-converter ISOP system [3]. However, input currents as well as input voltages have to been sensed. A three loop control scheme is implemented by sensing both the input voltages and the output currents [8],[9]. However, from the point view of power balance, achieving IVS can automatically realize OCS. As a result, it is unnecessary to implement both IVS and OCS control. A decoupling IVS control scheme [10]-[12], master/slave control [13] and uniform input voltage distribution control [14] for ISOP converters have been implemented with IVS loops without sensing the output currents at all. Sensorless current mode control is effective for an ISOP system [16], but component tolerances will lead to unbalanced voltage sharing among the modules.

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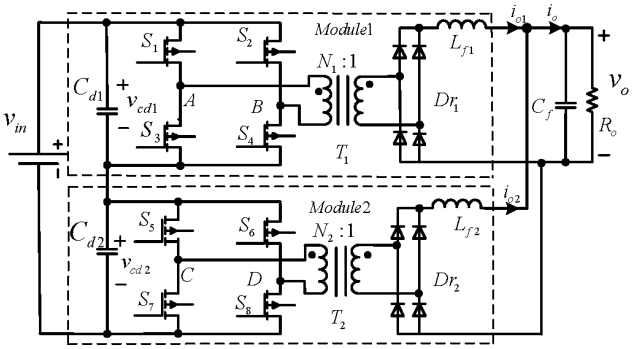

Fig. 1. ISOP connected two FB DC-DC converters.

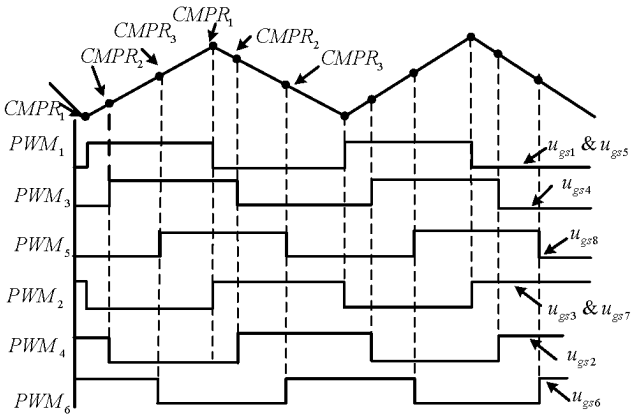

Fig. 2. Schematic of digital PWM generation.

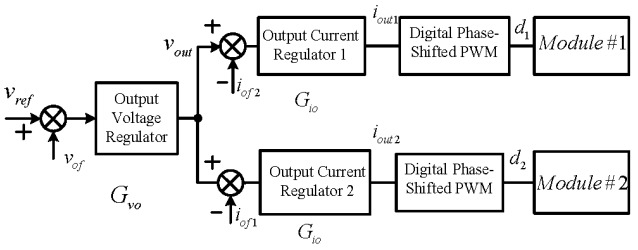

Fig. 3. Proposed control strategy.

In practice, these schemes [3],[8]-[16] belong to voltage mode control instead of current mode control. For ISOP converters, direct OCS control results in run-away conditions due to equivalent negative resistance characteristics from each module's input terminals [8],[11]. As a consequence, to achieve a power sharing balance, IVS control loops have to be used in order to achieve excellent power sharing for the ISOP modules. However, current mode control can simplify the design of the outer voltage loop control and improve the power supply performance in many ways, including better dynamics [16].

This paper proposes a digital PS PWM control strategy for ISOP connected two FB DC-DC modules. Moreover, to achieve a power balance between the two modules, an interleaving OCS (IOCS) control strategy is also proposed without any IVS control loops. As a result, the sensing of high input voltages is avoided. Besides, the whole system has many advantages such as simplification of the output voltage regulation (OVR) design. Small signal analysis and loop gain design are also made with the proposed control strategy and a 120W prototype is fabricated and experimentally evaluated.

II. Control Strategy For the System

Fig. 1 shows the schematic of an ISOP converter made up of two FB DC/DC converters. In this configuration, the total input voltage v_{in} is divided by the input capacitors C_{d1} and C_{d2}, thus we obtain the voltages v_{cd1} and v_{cd2} working as individual input voltages for each module respectively.

A. Digital PS PWM generation

A Texas Instrument DSP TMS320F2812 is selected to implement the PWM generation and the closed loop control. The PS-PWM gate signals for all of the switches are generated using the Full Compare Unit 1, the Full Compare Unit 2, the Full Compare Unit 3 and the General Purpose Timer 1 working in up/down counting mode, which can be seen from Fig.2, in which the left legs are leading while the right legs are lagging in phase. CMPR1, CMPR2 and CMPR3 are written to compare the registers and are updated once an underflow or period interrupt occurs. The value of the period register T1PR is determined by the preferred switching frequency and the system clock. There are two interrupts. One is a period interrupt and the other is an underflow interrupt. The values of the three compare registers are reloaded and updated at each interrupt, and hence, the three compare matches occur in either the up or down counting mode. In the up counting mode, the compare values are written as:

$$CMPR1 = 0, CMPR2 = T1PR - i_{out1}, CMPR3 = T1PR - i_{out2} \quad (1)$$

While in the down counting mode, they are expressed as:

$$CMPR1 = T1PR, CMPR2 = i_{out1}, CMPR3 = i_{out2} \quad (2)$$

where i_{out1} and i_{out2} are the inner current loop outputs of module #1 and module #2 respectively, which will be explained later. With the right values set for the three compare registers according to the closed loop regulator output, the six PWM signals are generated as shown in Fig. 2 when the compare match is set high effective. Besides, the PWM signals distribution principle can also be seen. The top switches (S_1&S_5) of the left legs are driven with PWM_1 while the bottom switches of the left legs (S_3&S_7) are driven with PWM_2. S_2 and S_4 of the right top legs are driven with PWM_4 and PWM_3 respectively while S_6 and S_8 of the right bottom leg are driven with PWM_6 and PWM_5 respectively. Note that actually, there is a dead time band between the gate signals for arbitrary legs.

B. Interleaving OCS control

Fig. 3 illustrates the proposed interleaving OCS control, where a common output voltage regulator provides the current reference v_{out} for both of the inner current loops. It should be noted that the inner current loop feedbacks are interleaving. This can be explained as follows, the current feedback for

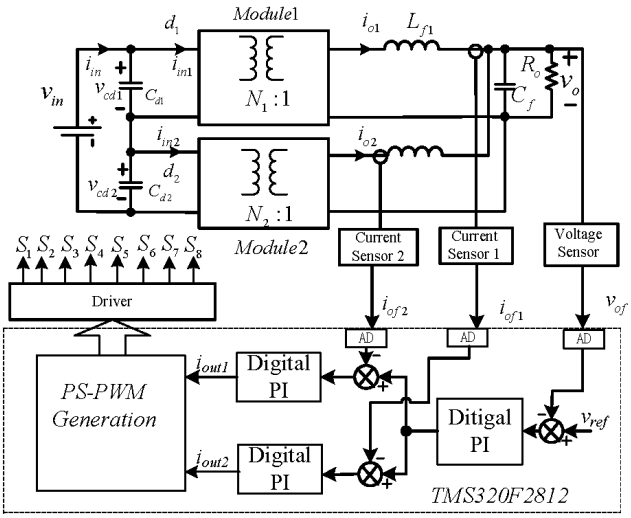

Fig. 4. Block diagram of the digital control system.

one module is the output current of another module while its own output current works as the current feedback of another module. Through compensation of the output current regulator G_{io}, we can derive the inner current loop outputs i_{out1} and i_{out2} which determine the duty ratios d_1 and d_2 respectively.

The stability of the proposed control scheme can be seen as follows. Assuming that the input voltage v_{in} is constant and that the system works under the steady state, if the input voltage v_{cd1} increases due to a disturbance, then the input voltage v_{cd2} decreases, and the output current i_{o1} increases while the output current i_{o2} decreases. Based on the control scheme shown in Fig. 3, the duty ratio d_1 increases while the duty ratio d_2 decreases. This increases the average input current drawn by module #1, resulting in a decrease of the input voltage v_{cd1} and an increase of the input voltage v_{cd2} until, in the end, equal sharing of the input voltage v_{in} can be obtained again. On the other hand, when v_{cd1} decreases due to a disturbance, equal sharing of the input voltage and the load current can be obtained. In the steady state, both of the output currents i_{out1} and i_{out2} track the OVR output v_{out} with negligible errors. Therefore, we can derive:

$$v_{out} = i_{of1} = i_{of2}. \tag{3}$$

Since the sensing gains of the two output currents are the same, we have $i_{of1} = K_i i_{o1}$ and $i_{of2} = K_i i_{o2}$, where K_i is the sensing gains of the current sensors. According to (3), under the steady state, OCS can be achieved.

The digital control diagram for a ISOP configuration comprising of two modules is shown in Fig.4. The whole control is implemented with a DSP TMS320F2812. The output voltage and the output currents of the individual modules are sampled by an internal AD of the DSP. By interleaving the two output currents as shown in Fig.3 and through digital proportion-integral (PI) compensation, i_{out1} and i_{out2} which determine the duty cycles for the two modules respectively are obtained. Based on the two values and the digital PWM generation shown in Fig.2, all the gate signals for the two PSFB DC/DC converters are generated.

TABLE I
SYSTEM SPECIFICATIONS

Item	Value	Item	Value
Input voltage v_{in}	700V	Inductance L_r	60 μH
Output voltage v_o	12V	Frequency f_s	50 kHz
Load R_o	1.2Ω	Inductance L_f	0.1 mH
Turns ratio $N_1$1 : 1	4:1	Capacitor C_f	1.0 mF
Turns ratio N_2 : 1	8:1	C_{d1}, C_{d2}	10 μF

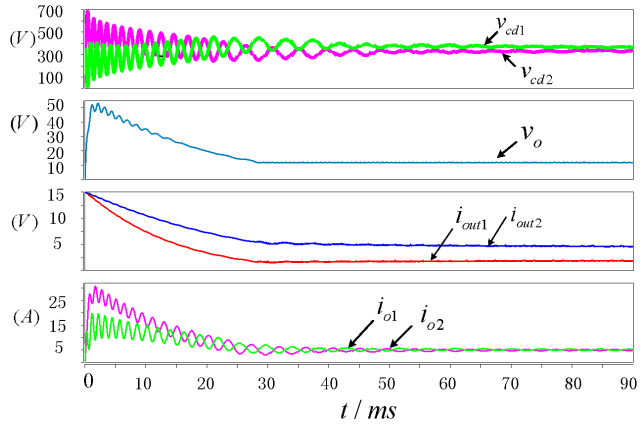

Fig. 5. Simulation waveforms of two-module ISOP system.

For an ISOP connected two full bridge DC-DC converter, a simulation is carried out to verify the effectiveness of the proposed control strategy. The simulation parameters are shown in Table I. As illustrated in the Table, the turns ratios of the two transformers are intentionally made different, with 8:1 for transformer T_1 and 4:1 for transformer T_2.

Fig.5 shows the simulation results for the two-module ISOP converter. As seen, during the initial state of the starting process, both the OVR and the current loop outputs saturate. As a result, both modules work under maximum duty cycles, causing unbalanced sharing of the input voltage due to their different turns ratios. Once the output voltage and output currents increase, both the OVR and the inner current controllers come out of saturation, and both the input voltage and the load current are eventually evenly shared under the steady state despite turns-ratio mismatches.

III. Small Signal Analysis and Regular Loop Gain Design

A. Small signal modeling of ISOP connected two PS StateDC-DC converters

Based on the small signal model of PS-FB DC-DC converters, we can derive the small signal model of a two-module ISOP system, as shown in Fig. 6, where $\hat{d}_1$ and $\hat{d}_2$ are the perturbations of the duty ratios d_1 and d_2, $v_{cdi}(i = 1,2)$ and $i_{oi}(i = 1,2)$ represent perturbations of individual input voltages and output currents, and $d_{ij}(j = 1,2)$ and $d_{vj}(j = 1,2)$ denote perturbations due to output currents and input voltages, which are expressed as:

$$\begin{cases} \hat{d}_{ij} = \dfrac{8L_r f_s}{NV_{in}} \hat{i}_{oj,(j=1,2)} \\ \hat{d}_{vj} = \dfrac{4L_r D_e f_s}{N^2 V_{in} R_o} \hat{v}_{cdj,(j=1,2)}. \end{cases} \tag{4}$$

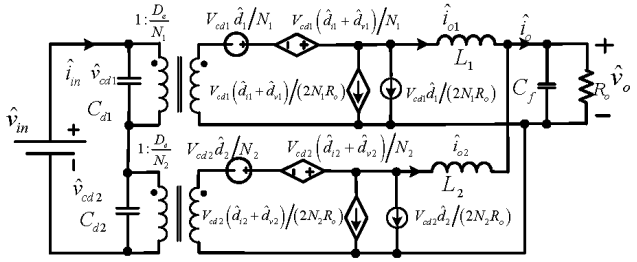

Fig. 6. Small-signal average model of the converter.

For simplicity of analysis, the two modules are assumed to have the same turns-ratio and the same output inductance, i.e., $N_1 = N_2 = N$ and $L_1 = L_2 = L$. Under the steady state, we have $V_{cd1} = V_{cd2} = v_{in}/2$. According to Fig.6, we obtain:

$$\begin{cases} \dfrac{D_e}{N_1}\hat{v}_{cd1} + \dfrac{V_{in}}{2N}\left(\hat{d}_1 + \hat{d}_{i1} + \hat{d}_{v1}\right) = sL\cdot\hat{i}_{o1} + \dfrac{R_o}{R_oC_fs+1}\left(\hat{i}_{o1} + \hat{i}_{o2}\right) & (5a) \\ \dfrac{D_e}{N_2}\hat{v}_{cd2} + \dfrac{V_{in}}{2N}\left(\hat{d}_2 + \hat{d}_{i2} + \hat{d}_{v2}\right) = sL\cdot\hat{i}_{o2} + \dfrac{R_o}{R_oC_fs+1}\left(\hat{i}_{o1} + \hat{i}_{o2}\right). & (5b) \end{cases}$$

Substituting (4) into (5a) and (5b), and then setting $\hat{v}_{cdi}$ $(i = 1,2)$, we obtain:

$$\begin{cases} \left(sL + \dfrac{R_o}{R_oC_fs+1} - \dfrac{4L_rf_s}{N^2}\right)\hat{i}_{o1} + \dfrac{R_o}{R_oC_fs+1}\hat{i}_{o2} = \dfrac{V_{in}}{2N}\hat{d}_1 & (6a) \\ \dfrac{R_o}{R_oC_fs+1}\hat{i}_{o1} + \left(sL + \dfrac{R_o}{R_oC_fs+1} - \dfrac{4L_rf_s}{N^2}\right)\hat{i}_{o2} = \dfrac{V_{in}}{2N}\hat{d}_2. & (6b) \end{cases}$$

According to (6a) and (6b), we derive:

$$\left[A^2 - \left(\frac{R_o}{R_oC_fs+1}\right)^2\right]\hat{i}_{o1} = \frac{V_{in}}{2N}\hat{d}_1\cdot A - \frac{V_{in}}{2N}\hat{d}_2\frac{R_o}{R_oC_fs+1} \quad (7)$$

where:

$$A = sL + \frac{R_o}{R_oC_fs+1} - \frac{4L_rf_s}{N^2}. \quad (8)$$

From (7), we have the transfer functions of the control-to-output current $\hat{i}_{oi}$:

$$\begin{cases} G_{11} = \left.\dfrac{\hat{i}_{o1}}{\hat{d}_1}\right|_{\hat{d}2=0} = \dfrac{AV_{in}}{2N\left[A^2 - \left(\frac{R_o}{R_oC_fs+1}\right)^2\right]} & (9a) \\ G_{12} = \left.\dfrac{\hat{i}_{o1}}{\hat{d}_2}\right|_{\hat{d}1=0} = \dfrac{-R_oV_{in}}{2N\left(R_oC_fs+1\right)\left[A^2 - \left(\frac{R_o}{R_oC_fs+1}\right)^2\right]}. & (9b) \end{cases}$$

Likewise, we can obtain the transfer functions of the control-to-output current $\hat{i}_{o2}$. They are identical to those of the control-to-output current $\hat{i}_{o1}$, as can be seen from the following:

$$G_{22} = G_{11}, G_{21} = G_{12};. \quad (10)$$

Hence, the output currents can be written in terms of the controls $\hat{d}_1$ and $\hat{d}_2$ in the following matrix:

$$\begin{bmatrix} \hat{i}_{o1} \\ \hat{i}_{o2} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix}\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} = \begin{bmatrix} G_m & G_n \\ G_n & G_m \end{bmatrix}\begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix}. \quad (11)$$

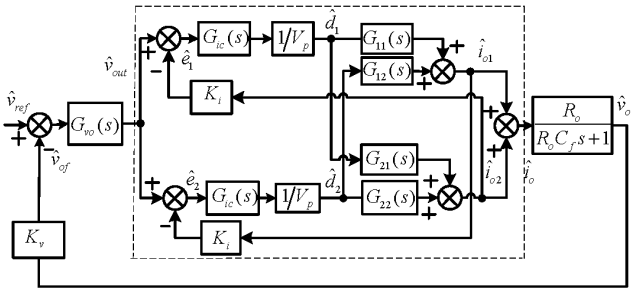

Fig. 7. System block diagram the system with IOCS control.

Based on (11), a closed-loop diagram of the system with the proposed control strategy is illustrated in Fig.7, where K_v and K_i are the sensor gains of the voltage and the current sensors respectively. $G_{vo}(s)$ is the voltage compensator while the compensators of both inner current loops are identical and denoted as $G_{ic}(s)$. V_p is the peak value of the ramp working as a carrier waveform. Then, the plant transfer function of the inner current loop for module #1 can be written as:

$$G_{id1}(s) = \left.\frac{\hat{i}_{o2}}{\hat{d}_1}\right|_{\hat{d}2=0} = G_{21}(s) = G_n(s). \quad (12)$$

Similarly, the plant transfer function of the inner current loop for module #2 is expressed as:

$$G_{id2}(s) = \left.\frac{\hat{i}_{o1}}{\hat{d}_2}\right|_{\hat{d}1=0} = G_{12}(s) = G_n(s). \quad (13)$$

B. Regulator loop design

Therefore, the loop gain of each inner current loop can be written as:

$$T_{id}(s) = K_iG_{ic}(s)G_n(s)/V_p. \quad (14)$$

According to the system diagram, the output currents can be written as:

$$\begin{cases} \hat{i}_{o1} = \dfrac{G_m(s)G_{ic}(s)\left(\hat{v}_{out} - K_i\hat{i}_{o2}\right)}{V_p} + \dfrac{G_n(s)G_{ic}(s)\left(\hat{v}_{out} - K_i\hat{i}_{o1}\right)}{V_p} & (15a) \\ \hat{i}_{o2} = \dfrac{G_m(s)G_{ic}(s)\left(\hat{v}_{out} - K_i\hat{i}_{o1}\right)}{V_p} + \dfrac{G_n(s)G_{ic}(s)\left(\hat{v}_{out} - K_i\hat{i}_{o2}\right)}{V_p}. & (15b) \end{cases}$$

Add the expressions (5a) and (15b), because we have $\hat{i}_o = \hat{i}_{o1} + \hat{i}_{o2}$. Thus, the equivalent transfer function shown within the dashed box is given by:

$$G_{iovout} = \frac{\hat{i}_o}{\hat{v}_{out}} = \frac{2G_{ic}(s)(G_m(s) + G_n(s))}{V_p + G_m(s)G_{ic}(s)K_i + G_n(s)G_{ic}(s)K_i}. \quad (16)$$

Thereby, the loop gain of the OVR loop is expressed by:

$$T_{vo}(s) = K_vG_{vo}(s)G_{iovout}(s)R_o/\left(R_oC_fs+1\right). \quad (17)$$

The specifications of the system are the same with those of the simulation except for the turns ratio. Both of the two transformers have the same turns ratios with 4:1. The voltage sensor gain K_v and the current sensor gain K_i are 0.1 and 0.05 respectively and the ramp amplitude V_p is 6V.

Both the proportional-integral (PI) type compensations for the output voltage and the inner current loops are made. While

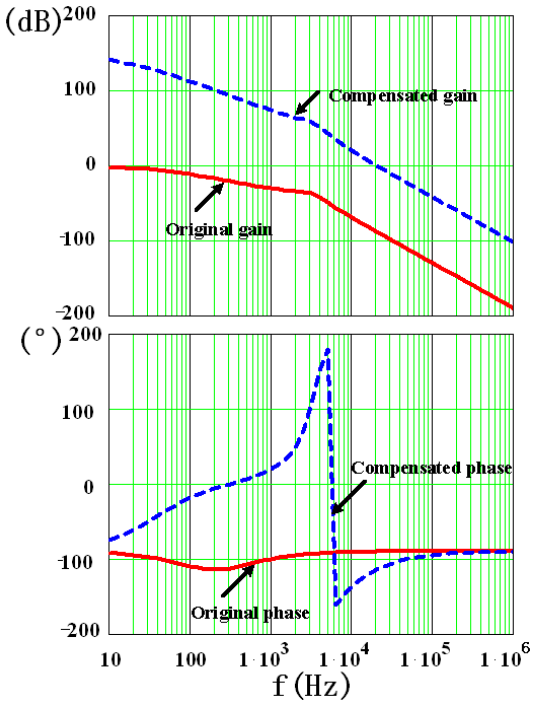

Fig. 8. Uncompensated and compensated OCS loop gain with the IOCS control.

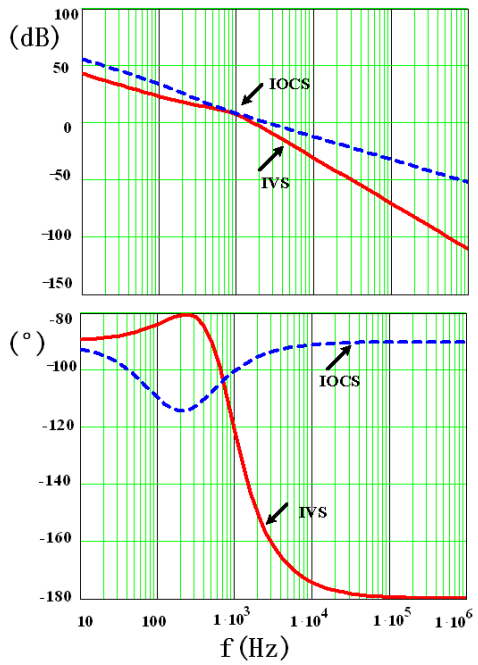

Fig. 9. Compensated OVR loop gains with IVS and IOCS.

under uncompensated conditions, both the transfer functions of the compensators $G_{ic}(s)$ and $G_{vo}(s)$ equal 1. The crossover frequency of the current loop is chosen to be 20 kHz, which is below the half switching frequency. The compensator of the inner current loop is shown as follows:

$$G_{ic}(s) = 10 + \frac{25000}{S}. \tag{18}$$

As illustrated in Fig.8, the original loop gain of $T_{id}(s)$ has a magnitude of -88.5dB at 20 kHz. However, after compensation, at the crossover frequency, the compensated loop gain has a phase margin of 65.57°, which is sufficient for stability.

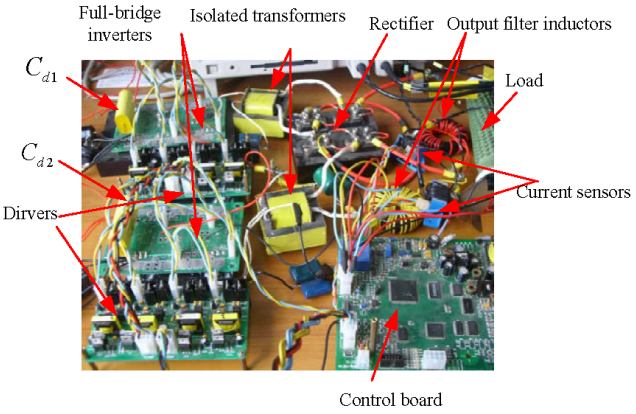

Fig. 10. Prototype of the two phase-shift full-bridge.

For the OVR loop gain design, the compensator is written as:

$$G_{vo}(s) = 4 + \frac{8000}{S}. \tag{19}$$

Fig.9 shows the compensated OVR loop gains with conventional IVS and the proposed control schemes based on the same voltage compensator shown in (18). As can be seen, while in the low frequency region, the magnitude of the loop gain with the IOCS control is larger than that with the IVS control. This implies that the output voltage can track the reference with fewer static errors. Moreover, the compensated loop gains of the OVR with the IOCS control strategy has a crossover frequency of 2.55kHz with a phase margin of 85.94o which is sufficiently large to make the whole system stable. However, with the conventional IVS control, the compensated loop has a crossover frequency of 1.67 kHz with a phase margin of 35.49o which is not large enough to guarantee stability. Because the crossover frequency of the OVR loop with the IVS control is lower than that with the proposed control scheme, the system with the proposed scheme has better dynamic performance. Otherwise, to achieve stability with the IVS control, the compensator function as shown in (18) has to be modified with lower values of the proportion and integration coefficients, but this will result in a decrease of the crossover frequency, leading to further deterioration of the dynamic performance.

IV. Experimental Results

Experiments on a prototype with the same parameters as those for simulation are made. The system specifications are shown in Table I. The prototype is shown in Fig.10. However, it should be noted that to verify the effectiveness of the proposed control scheme in the presence of mismatches in the converter parameters, the turns ratios of the two power transformers are intentionally designed to be different. The turns ratio of transformer T_1 is 4:1, while turns ratio of T_2 is 8:1.

Fig.11 shows gate signals with the proposed digital PS-PWM generation method under its rated input voltage and its rated load. Because the turns ratio of transformer T_1 is

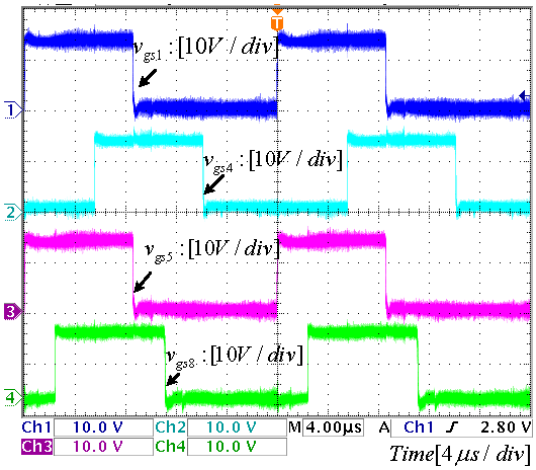

Fig. 11. Generation of digital PS PWM signals.

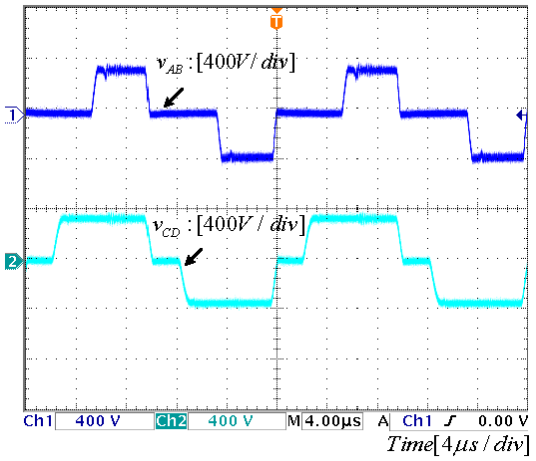

Fig. 12. Transformer primary voltages.

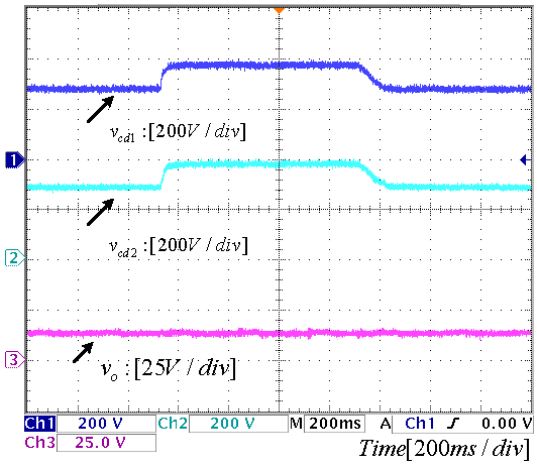

Fig. 13. Response to a step change in total input voltage.

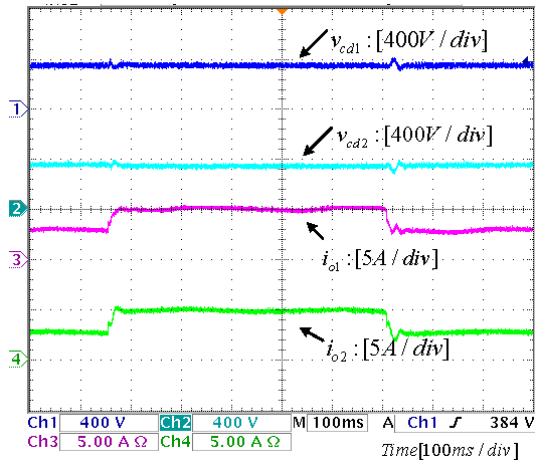

Fig. 14. Response to a step change between full and half load.

less than that of transformer T_2, the phase shifted angle of module #1 is therefore smaller than that of module #2. Fig.12 illustrates the primary voltages of the power transformers in the system with the gate signals shown in Fig.11. Their amplitudes reveal the corresponding individual input voltages resulting from achieving excellent IVS. Fig.13 illustrates the individual input voltages corresponding to a step change in the total input voltage varying between 600V and 800V. As seen, before and after the transient, the input voltage can be shared equally between the two modules and the output voltage is almost unaffected. Fig.14 shows the individual input voltages corresponding to a load stepping between half load(5A) and full load(10A). Despites the transients, the total input voltage can be shared equally fairly well.

V. Conclusions

In this paper, a method of generating digital PS PWM gating signals for ISOP connected full bridge DC-DC converters is presented.

This paper also proposes an IOCS control strategy for achieving power balance between the ISOP connected two DC-DC modules without using any input voltage control loops. With this scheme, excellent sharing with IVS and OCS can be obtained during the steady state as well as transients in spite of mismatches in the module parameters. In addition, based on small signal analysis and loop gain design for the system, when compared to the widely used IVS control strategies, with the IOCS control, the outer voltage loop design is simplified and the whole system has better static and dynamic performance. A 120W prototype based on a TMS320F2812 DSP control has been fabricated and tested, and the experimental results validate the effectiveness of the digital PS-PWM generation method and the IOCS control scheme.

It should be pointed out that the IOCS control strategy can also be applied to other buck-derived ISOP connected two modules by setting the duty cycle losses to zero.

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