Distributed ECU System Design for High Speed and High Precision Control of a Marine Engine

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***Abstract*— Efficient control of a marine engine requires an engine control unit (ECU) system that handles fast and precise signal processes for in-coming and out-going signals from fast running engines. In order to handle these roles, the sequential control has been adapted in the ECU system in small and medium size ship engines, which has caused high production cost and complexity of the system. Hence, this paper is focused on developing an distributed ECU system for high speed and high precision control of a marine engine by efficiently combining a CPLD chip and a microprocessor. By sharing load at the MCU with the designed CPLD chip, we could achieve in driving a marine engine with high speed and precise control so that the ECU board has been simplified and its production cost has been reduced**

***Index Terms*—Marine engine, ECU system, CPLD, microprocessor**

I. INTRODUCTION

For efficient driving of marine engines, a well designed ECU system is critically important. Hence this paper presents an efficient ECU system by using a simple microprocessor and a CPLD. The major missions for the developed ECU system of marine engines are detecting speeds of its engine and T/C(turbo charger), displaying engine speed into LED meters, and handling various input and output signal processes, two or more channels of 4~20mA analog signal I/Os and D/A conversion, and so on, which causes naturally overload to a single MCU to handle. In order to reduce such overload of MCU, we want to distribute some of the overall jobs to an independent high speed processing IC chip, CPLD as a peripheral device. Then we could achieve in driving a marine engine with high speed and precise control and simplify the ECU board with low cost.

The overall ECU system was then accomplished by using TI's 16 bit MSP430F133 as the main MCU and Xilinx's CPLD XC95288XLTQ100 as the peripheral CPLD chip. The software used in designing the CPLD chip is the Verilog HDL(Hardware Description Language) which was introduced in 1990 and adapted as IEEE 1364-1995 standard in 1995.

The final design of the ECU was composed of one CPLD chip, one MCU and one engine/TC(turbo charger) LED meter panel. The CPLD chip then takes charge in functions of a engine pulse counter, a turbo charger counter, a control unit and a Berrel shift. The engine/TC LED meter displays the speed of the engine or TC on the circular LED panel. The control unit selects input signal out of the engine speed and the TC. After this final design was verified by simulation with the simulation tool, ModelSim, the ECU was assembled to evaluate its performance using a logic analyzer Tektronix's TLA 720. From the evaluation, the designed ECU system shows better performance than conventional sequential controllers do by sharing the assigned jobs to MCU and the peripheral CPLD chip. Especially, since digitalizing a conventional sequential controller, the job producing precise 4~20mA analog output became simple in this newly designed ECU, the examining process in factories as well as the regular testing process could have been simply proceeded. Furthermore, we can easily modify or update the ECU system by virtue of digitalization, when any change is required in the control mechanism of the engine.

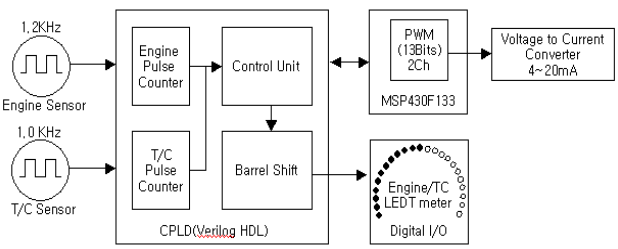

Fig. 1 Schematic diagram for the system

II. ECU SYSTEM CONFIGURATION

The ECU system of a marine engine receives two signals such as engine speed pulse and turbo charger speed pulse from its engine. Most of marine engine systems generally produce high speed engine pulses with the 1.2 kHz maximum and turbo charger speed pulses with the 1.0 kHz maximum as shown in Fig. 1. In order to count these two pulses, one CPLD chip will be designed in this chapter. In Fig. 1, the CPLD chip will include two counters to handle two input signals and a

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control unit to pass the speed information to the main control processor MSP430F133, which will pass the digital control input to the current converter ranging from 4 mA to 20mA. It also include one Barrel shift to display the engine speed or the turbo charger speed on the circular type LED Meter.

The CPLD chip implemented with Verilog HDL can be described as peripheral device, which correlates with MCU. The block diagram for the CPLD chip is shown in the Fig. 1, where each block was classified according to each function.

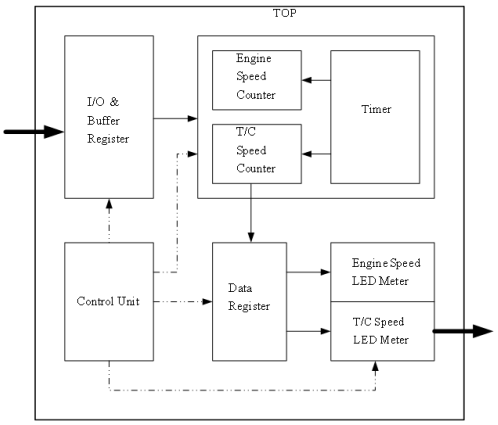


Fig. 2. CPLD internal block diagram

Those blocks are I/O buffer register block, data register block, control unit block, engine and turbo charger counters and timer block.

The I/O control and buffer register block is used to receive I/O signals, to initialize most of the internal registers and to be the main path of control signals. The data register block stores the data acquired through input channels or the data transmitted though output channels and the data generated from other internal registers. The control unit block controls overall units in the ECU so that the others blocks can be enabled or disabled by this unit. As the main block of the CPLD chip, the engine speed counter and the turbo charger counter are imbedded. The two counters receive pulses generated by a pick-up sensor installed with 50ms sampling time. This action is performed by a control signal from the control unit. The timer block then synchronizes to control the speed counters and data buses of the CPLD chip.

After the CPLD chip was designed with Verilog, TI's MSP430F133 micro-controller is selected as MCU to corporate with it. The connection between MCU and CPLD chip is shown in Fig. 3, where we can see it is similar to the one easily observed in general embedded systems. The $R/\overline{W}$ control pin at the MCU is directly connected to the CPLD $R/\overline{W}$ control pin, P4(b7), and the engine speed or turbo charger speed data is passed to the P1 pin at the MCU using the CntDat parallel port in the CPLD chip.

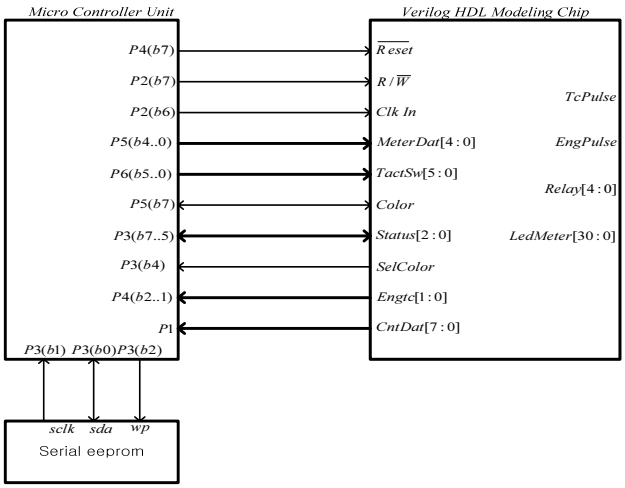


Fig. 3. The pin connection of MCU and CPLD

III. BLOCK DESIGN OF CPLD CHIP

The blocks in the CPLD chip are composed of I/O controller, buffer register, data register, control unit, timer, engine and turbo charger speed counter blocks.

3.1 Data I/O Block

This block exchanges the data form outside of the CPLD. Since CPLD chip does not have three-state buffer, input and output ports are separated. In order to use the I/O port as bi-directional data bus, the chip selection signal $\overline{CS}$ and read and write signal $R/\overline{W}$ can be utilized. When the $\overline{CS}$ signal is high, the data bus becomes high impedance state. As the $\overline{CS}$ signal keeps low state, the read state is selected as high $R/\overline{W}$ so that the data in the I/O buffer register are transmitted outside of the CPLD through a data bus. As the write state is selected as low in $R/\overline{W}$, the data goes into the I/O buffer register of the CPLD from the MCU through the data bus.

3.2 I/O Control Block

This block decides the direction of data flow between internal control register and the data register, stores input data from outside at a specified register, or controls output and data flow to the other internal register. It is operated based on the engine pulse counter and the turbo charger speed pulse counter. Fig. 4 explains how the data of the engine pulse counter and the turbo charger counter are passed to the MCU according to timer counter. At 10ms, the count data at the engine counter is stored at engine counter buffer and it is passed to the CntDat [6:0] bit at 20 ms. On the other hand the count data from the turbo charger counter is stored at a turbo charger counter buffer at 35ms and it is passed to the CntDat[6:0] bit at 45 ms. These procedures are repeated by 50ms period time.

3.3 Data Register Block

The data register block temporarily stores data received from outside or data to transmit to other register block. The data register has 14bits per unit and the size of the data bus is 1byte. Hence the MCU need to read data from CPLD twice such as first for its lower byte and second for its upper byte. Then the data temporarily stored in the data register move to a specified register according to the signal of the register control.

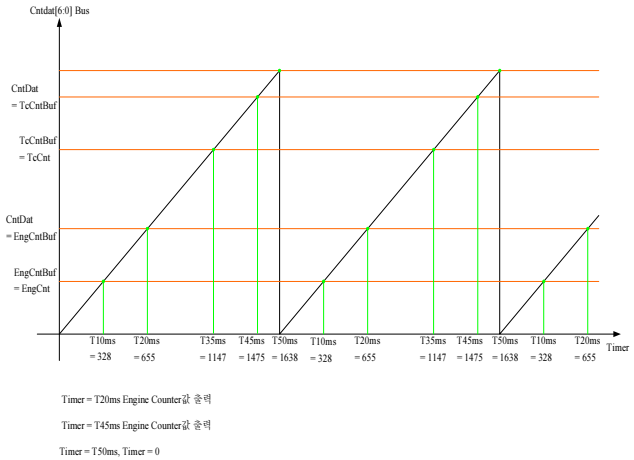


Fig. 4. The relation of Timer and Cnt[6:0] bit

3.4 Pulse Counter Block

The pulse counter uses 50ms period of the pulse scanning time and the pulse counter block is composed of one 8bit engine count register and one 8bit turbo charger count register with 1.2KHz and 1.0KHz frequencies, respectively. The two counters count 1200 pulses and 1000 pulses per second, respectively, so that 60 and 50 pulses are counted in 50ms of one pulse scan time. Based on those input pulse speeds, the count register is designed to handle higher engine speed than normal speed.

3.5 Control Unit Block

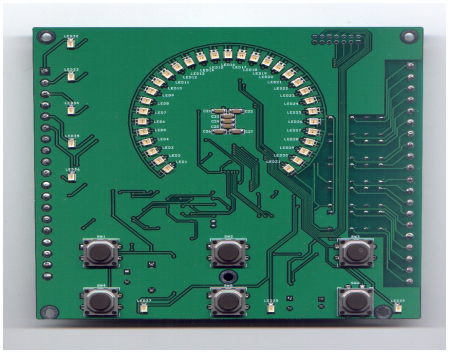
The control unit block triggers the I/O block so that it gives a command to each unit in ECU, after receiving various input signal. It controls the Cntdat[7:0] bus and Meterdat[4:0] bus to receive engine data and turbo charger data according to the control signals, selcolor, color, Engtc[1:0].

3.6 Display Block

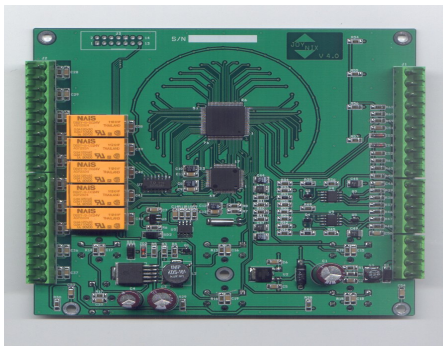
After this block sends the counted data to MCU by 50ms period, the MCU takes a moving average of the data, of which the result is transferred to CPLD through the data bus Meterdat[4:0]. The Meterdat is linked to LED meter by 31 pieces of LED which is using the barrel shift to show a engine speed or the turbo charger speed, and its brightness can be adjusted by the pulse duty ratio. This block uses a 5bit register that stores data to be shifted in the Barrel shift.

3.7 ECU(Engine Control Unit) Hardware

The marine ECU hardware is built based on Ti's MCU MSP430F133 and Xilink's CPLD XC9544XLTQ100. On the front panel, there is a circular array of LED to display the engine rpm and the turbo charger rpm as shown in Fig 5(a), (b). The ECU is designed to receive 32bit counter input of the engine rpm and turbo charger rpm and to display each at the LED array and to send 4 ~ 20 mA current proportional to rpm through two analog output channels.



(a) Front View



(b)Rear View

Fig. 5 Assembled ECU board

IV. ECU SIMULATION

This chapter will show the verification process through simulation after designing CPLD. The simulation tool is ModelSim by ModelSim Technology as HDL simulator that is using optimized direct compile architecture so that it provides fast compilation and simulation time. It is also a single kernel simulator that can accept VHDL, Verilog, or Mixed HDL(Verilog and VHDL).

By using ModelSim in simulation, the input and the output signals from each unit can be examined at each time step. Because a physical routing length was not applied in the simulation model, slight delays due to propagation through H/W lines are not considered here.

The engine speeds applied in the simulations are 0Hz, 300Hz, 600Hz and 1.2KHz, and the turbo charger output signals are 0Hz, 250Hz, 500Hz, 750Hz and 1KHz. In the

simulations, each signal was displayed in the monitor.

In the HDL simulation clock period was set 10ns without considering time delay between each node and each signal. Fig. 6 shows the simulation results under condition of 900Hz engine speed and 750Hz turbo charger speed. After the detected signal is counted, it(engine count data = 45) is stored in EngCnt and TcCnt registers, and the EngCntBuf and the data (turbo charger count data = 38) in TcCntBuf are transferred to MCU with 50ms period.

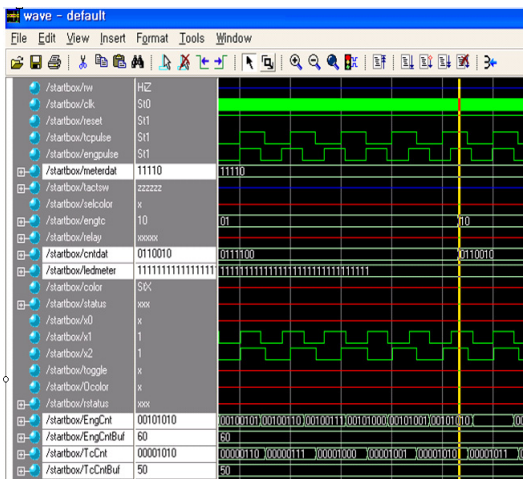


Fig. 6 Simulation results with engine speed 900Hz and turbo charger speed 750Hz

V. EXPERIMETAL RESULTS

After an experimental test bed was composed of the ECU and a marine engine, various experiments could be performed. The experimental results are observed through a logic analyzer Tektronix TLA 720 so that a proper operation of the each unit and its proper signal output could have been checked.

The experiments were performed by Busan-Ulsan test institution according to IACS E10('97) standard which specifies experiment conditions of room temperature, dry and hot temperature(70 C for 2 hours), humid and hot temperature(55C, 96%humidity for 12 hours). Fig 7. shows that the simulation results and experimental results are identical at the operational condition of engine pulse speed 900Hz and turbod charger pulse speed 750Hz where signals of cntdat[6:0] = b0101101↔b0100110, engtc[1:0]=b01↔b10, and meterdat[4:0]=b10110 transmitted to the MCU with 25ms period. Table 1 shows the output currents and the prescribed currents measured at every hundred Hz speed pulse increment. The maximum error observed here is 0.025% in 4~20mA signal range which is so small to be neglected. The other experiments performed in the dry and hot condition and the humid and hot condition also produce negligible errors. Fig 8. shows the experimental results of engine speed at dry and hot condition, which are quite identical to the experimental results of turbo charger speed in Fig.9.

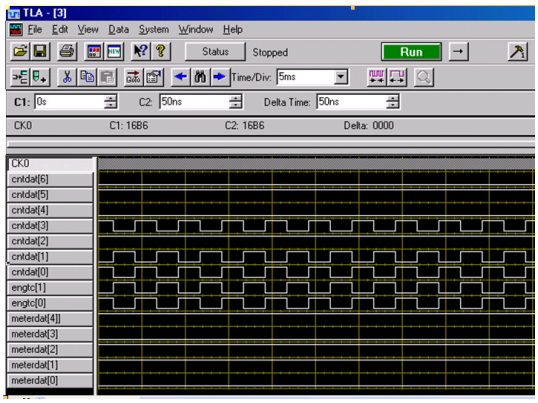


Fig. 7. Experiment results with engine speed 900Hz and turbo charger speed 750Hz

TABLE 1.
RESULTS OF EXPERIMENTS

	Freq (Hz)	Output current (mA)	Reference (mA)	Error (%)
Engine RPM				
1	100	5.333	5.333	0
2	200	6.667	6.667	0
3	300	8.001	8.000	0.0125
4	400	9.334	9.333	0.011
5	500	10.669	10.667	0.010
6	600	12.002	12.000	0.016
7	700	13.336	13.333	0.023
8	800	14.668	14.667	0.013
9	900	16.002	16.000	0.0125
10	1000	17.333	17.333	0
11	1100	18.667	18.667	0
Turbo Charger RPM				
1	0	4.000	4.000	0
2	100	5.601	5.601	0
3	200	7.200	7.200	0
4	300	8.802	8.800	0.025
5	400	10.402	10.400	0.020
6	500	12.001	12.000	0.008
7	600	13.601	13.600	0.008
8	700	15.201	15.200	0.007
9	800	16.801	16.800	0.006
10	900	18.400	18.400	0
11	1000	20.000	20.000	0

VI. CONCLUSIONS

This paper shows that the sequential control used in the ECU system of small and medium size ship engines could be substituted to a digital circuit, which is combined with a CPLD chip and a microprocessor. If this substitution is achieved only with FPGA, program size needs to be so

huge though the circuit could be reduced a lot. The huge program size may cause a burden to developers. If only a microprocessor takes care of the mission, then data processing speed and precision could be down though the cost could be saved. The best way to compromise such problems is combination of a CPLD and a microprocessor as the CPLD is adapted for the part requiring high speed processing and the microprocessor is assigned to take care of the rest part.

From the similarity between the simulation results and experimental results, it is concluded that the suggested system was operated properly. Specially, by combining MCU and CPLD in ECU, the overall circuit became simple with more functions and by digitalizing the analog correcting process of output current (4~20mA) quality inspection process and modification became simplified.is achieved Then this paper shows design of CPLD chip and its simulation with the microprocessor. this paper is focused on developing an distributed ECU system for high speed and high precision control of a marine engine by efficiently combining a CPLD chip and a microprocessor. By sharing load at the MCU with the peripheral CPLD chip, we could achieve the high speed driving and precise control of a marine engine so that the ECU board has been simplified and its production cost has been reduced.

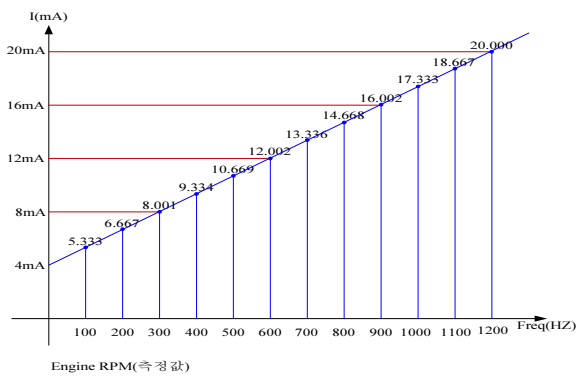


Fig. 8 Engine RPM test results at dry and hot condition.

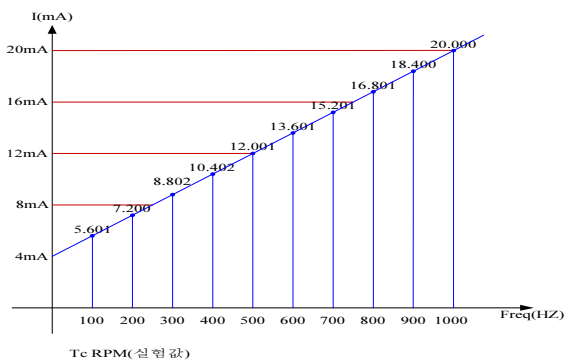


Fig. 9 Turbo Charger RPM test results at dry and hot condition

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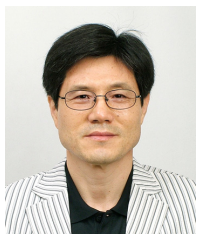

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