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Hexagonal Material Flow Pattern for Next Generation Semiconductor Fabrication

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차세대 반도체 펩을 위한 육각형 물류 구조의 설계

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The semiconductor industry is highly capital and technology intensive. Technology advancement on circuit design and process improvement requires chip makers continuously to invest a new fabrication facility that costs more than 3 billion US dollars. Especially major semiconductor companies recently started to discuss 450mm fabrication substituting existing 300mm fabrication of which facilities were initiated to build in 1998. If the plan is consolidated, the yield of 450mm facility would be more than doubled compared to existing 300mm facility. In steps of this important investment, facility layout has been acknowledged as one of the most important factors to be competitive in the market. This research proposes a new concept of semiconductor facility layout using hexagonal floor plan and its compatible material flow pattern. The main objective of this proposal is to improve the productivity of the unified layout that has been popularly used to build existing facilities. In this research, practical characteristics of the semiconductor fabrication are taken into account to develop a new layout alternative based on the analysis of Chung and Tanchoco (2009). The performance of the proposed layout alternative is analyzed using computer simulation and the results show that the new layout alternative outperforms the existing layout alternative, unified layout. However, a few questions on space efficiency to the new alternative were raised in communication with industry practitioners. These questions are left for a future study.

Keywords: Semiconductor Wafer Fabrication, Semiconductor Facility Layout, Wafer Fabrication Layout

1. Introduction

Typical wafer fabrication (fab) has about 20 to 35 processing layers consisting of more than 300 total processing stages (Turley, 2003); however, they keep increasing because of sophisticated device technologies. It is expected that about 40 layers with a correspondent increase of processing stages will be used in a decade (Singer, 2006). Each layer needs one litho operation to make a pattern on chips in the wafer, which is the most important and bottleneck stage in a fab. Including litho toolsets, many different types of toolset groups are repeatedly used to fabricate the layers of conductors, semiconductors, and their insulators on wafers; hence, the material flow system of the fab can be seen as a typical process department system (Tompkins *et al*., 2003). A fab line consists of about 500 processing tools in a standard fab size that is defined by WSPM (wafer start per month). It takes about 50 days from input to finish and a wafer has to travel more than 12.9km in the fab to be completed (Lin *et al*., 2003a).

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A fab is characterized by random yields with low toolset flexibility, diverse equipment characteristics, reentrant flow, and mixed processing models (Fowler *et al.*, 2002, Montoya-Torres 2006). There are about a 35%～45% of WIP and wafer waiting times in front of litho toolsets to prevent their starvation (Lee *et al.*, 2001). And also random disturbance has been regarded as one of the important characteristics of semiconductor fab (Fowler *et al*., 2002), apparently because of the high standard on toolset utilization and the low toolset flexibility for the expensive toolsets. Consequently, optimizing fab designs is even more important.

The importance of the facility layout research in the semiconductor industry has been recognized in several different aspects of the problem. First, in many cases, once the layout is set up, it is difficult to change or its modification cost is typically very high because of not only reconstruction cost but also opportunity cost due to down time. Since it is a very expensive facility, the latter cost is much higher. Second, an efficient facility layout keeps material handling cost low and provides fast and flexible infrastructure for operations in a facility. Sometimes, other operational issues such as scheduling, dispatching, and material handling control are under its downstream activities (Chung and Jang, 2007). Finally, since a large investment follows a new facility layout design for chip manufacturers, it is very risky from the perspective of decision making. It takes a long time for a new layout alternative or layout methodology to be applicable for an actual layout project. In the industry, companies use a similar layout design repeatedly for a long time partly because of the high risk and partly because of a lack of prior study on new layouts. More specifically, the industry has used the spine flow for more than 20 years with slight modifications when new fabs were constructed. Recently, it started to prepare a next generation fab system for the larger wafer size including a new layout alternative and material handling system.

The hexagonal flow pattern was initially proposed by Chung and Tanchoco (2009) for general manufacturing and service facilities. They showed that the hexagonal flow plan and its compatible material flow pattern have many quantitative and qualitative advantages. This paper applies the hexagonal material flow pattern to design a machine layout for a semiconductor wafer fab line. To analyze the performance of this practical application, this research conducts simulation experiments comparing it with an existing popular layout alternative. The layout criterion focused in this paper is the material flow cost that is generally the most important criterion for FLP (facility layout problem).

The rest of this article consists of the following sections. Section 2 summarizes previous studies on the semiconductor facility layout. Section 3 reviews details of the hexagonal flow pattern that was introduced by Chung and Tanchoco (2009) and then the proposed hexagonal layout for the next generation wafer fab will be explained with detailed assumptions of the layout. A simulation analysis comparing the hexagonal layout with the unified layout is charted in section 4. Section 5 concludes the research.

2. Previous Research

Recently the industry started to discuss the design of the next generation fab, generations of which are defined by the wafer sizes (Singer, 2006, Pettinato and Pillai, 2005). The move from 150 to 200 mm took about five years and the transition to 300 mm took eight years (Singer, 2006). Recently, International Technology Roadmap for Semiconductors (ITRS) decided the next wafer size as 450 mm temporally and some practitioners already started to discuss alternative fab layout designs and automated material handling systems. Based on the time frame, Singer expects that 450 mm technology will be required by 2011～2015 and different paradigms in the design of fab layout and AMHS (automated material handling system) are necessary to reduce increased cost. It is expected that the batch processing toolsets will be minimized in the next generation fab. There is also a drive towards methods that address the long term requirements for reduced microscopic defects, lower processing temperatures, lower cost of ownership, reduced cycle times, smaller feature sizes, and environmentally friendly process.

Koike *et al*. (1995) propose a new concept of the wafer fab line for the super-quick TAT (turn around time). The concept adopts both single wafer and batch processing modules accordingly. Batch processing lines are replaced by an extra single wafer processing paths. The research also uses a reduced number of wafers in a lot to reduce TAT. This super-quick TAT concept helps the fab to reduce a ramp up period dramatically. Koike (2000) also claim that it is very important to reduce periods of fab construction and equipment start-ups as well as to obtain more accurate forecasts to reduce fluctuated market risk. The research also proposes a scalable fab strategy, a minimum expansion unit of 7K WS PM in order to minimize investment risk and to maintain flexibility to market changes.

Performance evaluation is an important part of the layout and AMHS design. Many simulation experiments have been conducted for these purposes in the literature. The typical performance measures are generally throughput, utilization, lead time, delivery time, and fixed cost; however, they vary by focuses of problems. Analytical models based on the queuing theory are also used for analyzing layout and AMHS designs. Although an analytical model cannot consider a

problem as detailed as a simulation model, it has a great benefit from quick response times.

Hase *et al*. (1994) and Geiger *et al*. (1997) perform simulation studies on a few different types of the cell layout based on the dedication degree of tools. Their simulation models compare the cell layouts with a conventional bay layout. In the analysis, among different types of the cell layout, the dedicated cell layout shows better performance due to the reduced setup time, improved yield, and simpler material flow than others. However, the cell layout lacks flexibility because it assigns tools into cells based on process routings of a few product types.

Many researchers including Campbell and Ammenheuser (2000), Noben *et al*. (2001), and Mackulak and Savory (2001) use computer simulations to compare layout and AMHS design alternatives. However, this approach is limited by the long implementation times. Mackulak *et al*. (1998) study reusable simulation models to reduce a simulation lead time. They use a generic model to construct a situation with a reasonably small set of unique components, and reuse it repeatedly for changing models. Pillai *et al*. (2004) also study a dynamic simulation model that can be reused for different problems using five simulation modules. Kong (2007) introduces a two-step simulation approach. His method has been used for practical fab simulations and consists of the production capacity simulation and AMHS simulation. Data including utilization of toolsets from the first simulation are used as input data in the second simulation.

Analytical methods evaluating layout and AMHS designs are drawing more attentions recently because of its very short modeling lead time compared to a simulation model. Chen *et al*. (1988) develop a queuing network model to predict the performance of a wafer fab, which is presented by the output quantities of the fab. In their model, individual toolsets are servers and NPWs (non-productive wafers) are modeled using an open queuing network model while productive wafers are modeled by a closed queuing network model. Connors *et al*. (1996) and Hopp *et al*. (2002) determine required number of toolsets meeting a targeted production quantity using a queuing network model. To estimate performance of AMHS, Nazzal and McGinnis (2007) develop a queuing network model that considers relatively detailed aspects of an OHT (overhead hoist transporter) loop in a conventional bay type layout. The model estimates throughput and rate of delayed move requests in the given bay served by an OHT system operated by the FEFS (first encountered first service) polity. States of the pickup and drop off stations are modeled with a discrete set of states. The loop and stations are represented by Markov chain of which transfer requests are arrived with a Poisson process. Using relations between states and stations, a transition matrix and its stead state probabilities are obtained using the positive recurrent Markov chain.

Over the past decades, most of previous studies on semiconductor facility layout in the literature have been performed based on a few conventional material flow patterns. Also, as reviewed in this section, the vast majority of revolutionary layout alternatives that have been proposed by academia are turned out to be difficult to implement in near future since they adopt single wafer production that faces too many obstacles in practice. Based on these two observations, this research proposes a practical but adopting unconventional material flow pattern to improve the performance of the wafer fab layout.

3. Hexagonal Layout and Semiconductor Hexagonal Layout

This section briefly reviews a background of this research by explaining the expected travel distance of the hexagonal floor plan with other floor plans explored by Chung and Tanchoco (2009). The proposed semiconductor hexagonal layout that uses the hexagonal floor plan and its compatible material flow pattern will be explained in detail with assumptions to develop the layout.

3.1 Expected Travel Distance of Hexagonal Layout

<Table 1> compares the expected travel distances, their variances, and maximum travel distances of the various floor plans in the rectilinear travel model as shown in Chung and Tanchoco (2009). The expected distance of the hexagonal floor plan is less than those of rectangular, square, and dia-

Table 1. Expected travel distances and variances for different floor plans

Floor plans	Rectilinear distance			
	ETD[1]	ETD(%)[2]	Var	Max
Rectangular12	11.40	1.085	36.12	34.19
Rectangular34	10.85	1.032	30.07	32.57
Square	10.75	1.023	28.78	32.24
Diamond	10.63	1.011	25.39	32.24
Hexagon	10.51	1.000	25.62	27.38
Octagon	10.50	0.999	25.50	27.11
Circle	10.48	0.997	25.45	25.72

Note) ETD[1] : expected travel distance.
ETD(%)[2] : $\frac{ETD}{ETD\ of\ Hexaogn}$.

mond plans, and slightly larger than those of the octagonal and circular plans. Based on column 2, the ETD of the hexagon only is 0.3% larger than those of the circle creating the minimum distances; however, they are 1.1% less than the diamond that is ranked right next to the hexagon. The variance and maximum criteria show similar performance results to the comparison of the expected travel distance but the reduction becomes more noticeable with the variance. Compared to the octagonal and circular floor plans, the hexagonal floor plan is more scalable to expand and more compatible for designing material flow patterns. Note that the circular and octagonal floor plans do not pack well for multiple patterns (Newell, 1973) whereas the rectangle, square, diamond, and hexagon pack without empty spaces between them. More discussion on the qualitative analysis of the hexagonal layout was provided in Chung and Tanchoco (2009).

The authors of this research note that one important assumption of Chung and Tanchoco (2009) is that sources and destinations of trips are randomly and uniformly distributed in the floor plans. This assumption is generally applied to a process department system but not to a product department system (Tompkins *et al*., 2003). Also the semiconductor fab typically uses a process department system since it consists of very complicated processes including re-entrant flow, many process stages, and a large number of toolsets as mentioned earlier in section 1. As the product mix of a fab increases the complexity of its operation becomes even more complicated, and the material flow pattern in the fab tends to be random and independent from the perspective of material handling.

3.2 Semiconductor Hexagonal Layout

Based on the conclusion of the previous section, this research proposes the hexagonal semiconductor layout for designing the next generation wafer fab facilities. The proposed block layout under the hexagonal flow pattern is shown in <Figure 1>. This layout has a regular hexagonal floor plan with an edge of 50 m, and its total area is about 6,500 m2. It was developed based on semiconductor layout design principles presented in Quinn and Bass (1999). It is noticeable that, in the layout, litho toolsets are placed close to the core of the hexagon because they are the most important and frequently used toolsets. This layout utilizes a combined OHT (overhead hoist transporter)/OHS (overhead shuttle) system as the main transportation system and the system uses a double track unidirectional or variable path as seen in the figure. Though it is not shown in the layout, there are many shortcuts between two parallel tracks.

Based on the block layout, a machine layout was developed as illustrated in <Figure 2>. In the machine layout, actual sizes of machines, clearances, and flow paths were taken into account. Since this paper focuses on the material flow pattern, it does not develop any analytical or mathematical models for designing the block or machine layout under the hexagonal material flow pattern for the semiconductor layout, which will be left for a future study of this work. The layout design is named as the hexagonal semiconductor layout.

<Figure 3> illustrates the scalability of the hexagonal layout for the semiconductor fab. Generally, major semiconductor companies such as Intel and Samsung build three or more fab lines in a generation defined by the wafer size. Wafers in the same size can be processed in different fab lines. By connecting those fab lines, toolset utilization can be increased due to a central pooling effect. More specifically, toolsets and lots in a larger layout would share their capacities more to prevent starvation of important toolsets and delays of processing time due to toolset breakdowns. In <Figure 3>, each hexagon is set up one at a time as a modular structure, and has the capacity of 25K WSPM (wafer start per month) hence, the total capacity would be more than 100K WSPM.

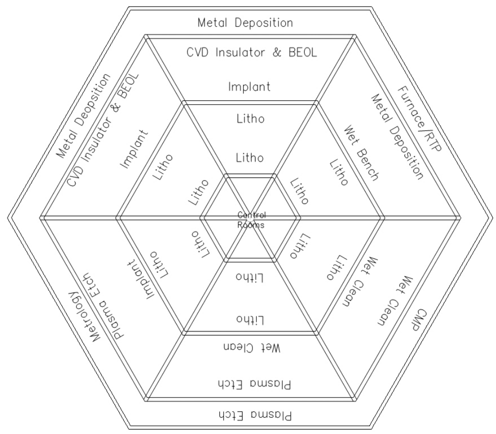

Figure 1. Block layout using hexagonal material flow pattern

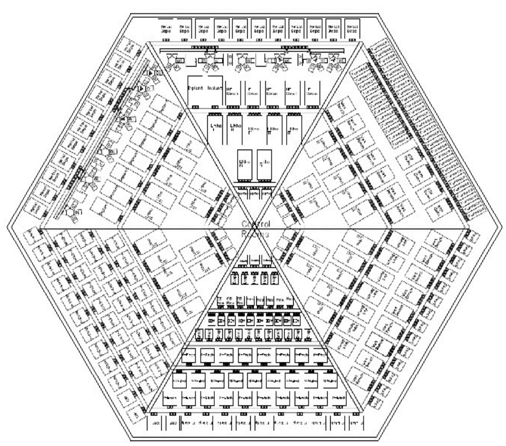

Figure 2. Hexagonal semiconductor layout

There are a few different types of wafer fab lines based on product types fabricated in the lines as well as the capacities of the lines. To clarify focuses of this research the following assumptions are used. Also the new layout alternative presented in <Figure 2> was developed based on the following assumptions.

(1) The wafer size in the new facility is 450 mm, which is considered as the next generation wafer size.
(2) The process plan in the new layout is based on 0.18 μm process presented by International SEMATECH (Quinn and Bass, 1999).
(3) In addition to the process above, relationships between toolset groups based on opinions of process engineers are taken into account.
(4) The layout type proposed in this section is a farm layout (Quinn and Bass, 1999) that the same types of toolsets are placed in the same area to maximize material flow flexibility.
(5) Wafers are handled by lots consisting of 20 wafers per carrier, and the production capacity meets 25K WSPM (wafer start per month) for the layout shown in <Figure 2>.
(6) The number of toolsets, their sizes, and other data such as processing times and toolset clearances are based on the data provided by the International SEMATECH, which is based on 300 mm wafer size; however, the toolset sizes are 1.5 times larger than those of the SEMATECH to consider 450 mm.
(7) For the newly developed layout, there will be no problems related to building construction, chemical supply, and utility hookup.
(8) Since the layout uses the TSS (track storage system), there are no stockers.

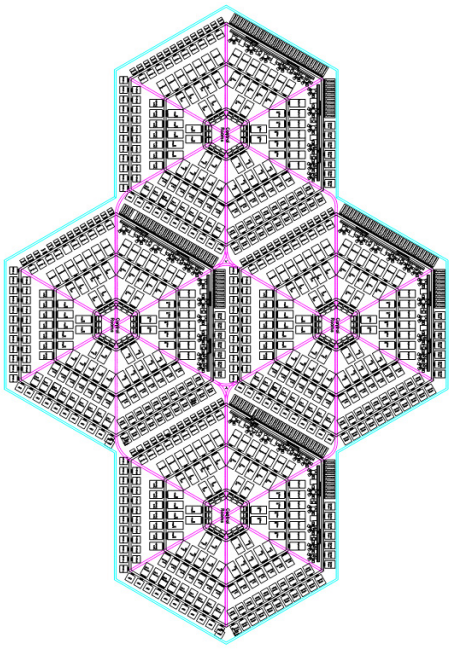

Figure 3. Connected semiconductor hexagonal layout

4. Simulation Analysis

In this section, the hexagonal semiconductor layout is compared with the existing unified layout using a commercial simulation package, FACTOR/AIM 8.0. First, the unified layout is introduced briefly and then the simulation model including input data and assumptions is explained in details. The simulation experiments were conducted with two main factors, different product mix, and arrival rate. Two observed performance metrics to compare the two layout alternatives from the experiments are vehicle utilization and total transportation time. Under the same arrival rates given to the two layout alternatives, the alternative having less vehicle utilization and total transportation time is regarded as the better alternative.

4.1 Unified Layout

The unified layout consists of many bays under a typical spine type material flow pattern. Recently, the unified layout became one of the most popular alternatives used by the industry due to the high tool-to-tool direct transportation rate (Fischmann, 2008, Montoya-Torres, 2007, Montoya-Torres *et al*., 2006). When developing the unified layout, the farm layout configuration presented in the study of International SEMATECH (Quinn and Bass, 1999) was referred. The farm layout proposed by SEMATECH also has a spine configuration as to the unified layout but there is no path on the right and left perimeters of the layout. The difference is that bays on the sides of the center spine are connected by OHT or OHS loops in the unified layout while they are connected through the center spine only in the farm layout. The authors noted that this unified layout alternative has been used by main semiconductor makers to develop the most recent several fab facilities substituting the farm layout. Although it has been popular in practice, the unified layout has not been officially announced in the literature partly because of the confidential issues across the semiconductor makers.

In <Figure 4>, the same toolsets in <Figure 2> were placed in the unified layout using the same principles. The rectangular floor plan in <Figure 4> is 70 m×96 m, of which area is also about 6,500 m^2. It turned out that the total track length of the OHT system used by the unified layout is about

1642 m while that of the hexagonal layout is 1692 m. There is about a 3% difference.

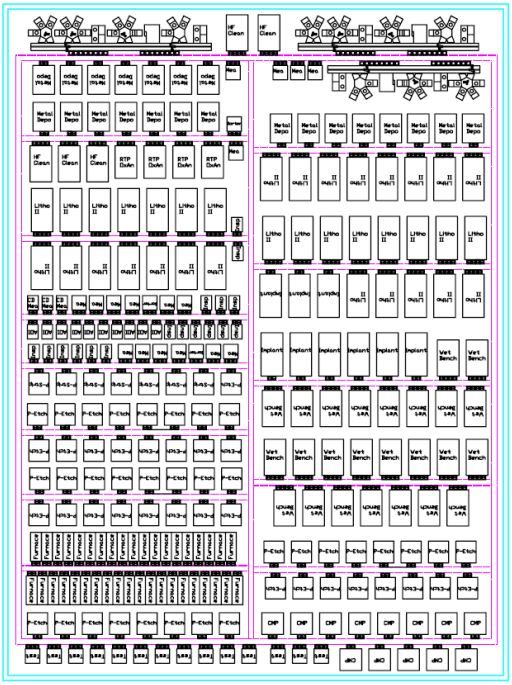

Figure 4. Unified machine layout.

4.2 Simulation Input Models

In this section, we identify important input data and assumptions for simulation experiments. Especially, creating material flows in complicated wafer fabrication lines has been an important issue in practice. This research introduces a new method of creating the material flows based on process sequences of independent layers. This method readily considers product mix in fabrication lines.

(1) Input Data and Assumptions

<Table 2> summarizes the simulation input data and assumptions. First, this simulation model considers three different product mix scenarios. In the industry, changes in product mix often make the design principles of the layout obsolete even before the fab line is fully ramped up. Hence, a good layout design should create good performance undera certain product mix environment. More details on how to create the product mix scenario will be discussed below. To observe behaviors of the performance; i.e., not the static performance measurement, the simulation model considers three different levels of the Transportation arrival rates. Consequently, the two factors create 9 different simulation scenarios based on different levels of them, each of which was simulated for one month. Also each scenario was replicated 5 times to obtain unbiased results; however, it turned out that the one month simulation period is long enough that differences by the repetitions are negligible. In the table, details of the OHT system are explained.

(2) Identification of Material Flows

Two methods were conventionally used to consider material flows of the wafer fab in simulation experiments. First, material flows are created based on the process plans of only one or two product types (Kong, 2007; Quinn and Bass, 1999). This method considers not only material handling factors but also process factors such as processing time and toolset breakdown time to evaluate overall fab efficiency. One advantage of this method is that its model closely follows the real world fab operation. However, in practice, there are many issues related to product mix; hence, considering only one or two product types in the simulation hardly creates an unbiased result. Also using this method, it is sometimes difficult to evaluate the performance of the material handling efficiency because it is mixed with the operational efficiency of the process toolsets.

To evaluate material handling efficiency, researchers (Lin *et al*., 2003b) and practitioners use a material flow matrix created from process plans of several product types. Arrival requests in the simulation are created based on the matrix using a probability distribution function. An advantage of this method is its simplicity in using the matrix. However, it is not easy to create a reasonable matrix reflecting real world material flows.

Table 2. Simulation input data and assumptions

Item		Input
Product mix		3 types of product mix scenarios
Arrive rate level		3 levels
Number of simulation replications		5 times (with 9 alternatives)
Simulation periods		1 month
OHT system	Speed	30 m/hr
	Load/unload time	30 sec
	Empty vehicle selection policy	Closest idle
	Order selection policy	Closest
	Idle parking policy	Idle stop
	AGV vehicle clearance	0.5 m

To overcome these drawbacks, this paper proposes a new method based on process plans of layers, which follows process sequences of layers. It is noted that a process plan con-

sists of layers in a wafer fab. There are layer types used repeatedly for different product types as well as in a product type. In <Table 3>, these layer types are identified based on the process plan given by the International SEMATECH (Quinn and Bass, 1999). Note that there are 8 layer types in the table. It is assumed that a product type consists of a combination of these layers, each of which can be used more than one time. Using these layer types, a product mix scenario is created in <Table 4>. Three product types were created out of the eight layer types in the table. Product type A was created based on Quinn and Bass (1999). To create product types B and C, the author consulted a process engineer who worked for more than 10 years in the semiconductor industry. Using this modular method, much more product mix scenarios are readily created.

In the simulation, wafer lots in the FOUP (front opening unified pod) are independently released and they follow process sequences of these layers. Arrivals of lots for each layer were created by the exponential distribution and the total amount of lots released in average was 25 K WSPM. Using the three different product types and three different arrival rates, <Table 5> shows the nine cases tested.

Table 3. Layer types and their process sequence

Layer ID.	Process sequence
L1	WB-FR-LH-DE
L2	DE-DS-HF-WB-FR-LH-IM
L3	IM-DS-WB-LH-IM
L4	DE-DS-WB-CV-CM-MD-LH-DE
L5	DE-WB-FR-OX-TS-WB-LH-DE
L6	DE-WB-CV-CM-MD-LH-DE
L7	IM-DS-WB-FR-DE-WB-OX-LH-IM
L8	IM-DS-WB-OX-DE-DS-WB-HF-MD-LH-DE

Note) CM : CMP CV : CVD
DE : Dry etch DS : Dry strip
FR : Furnace HF : HF cleaning
IM : Implant LH : Photolithography
MD : Metal deposition OX : Oxidation
TS : Test WB : Wet bench

Table 4. Product mix scenario number of layer types

Product mix	L1	L2	L3	L4	L5	L6	L7	L8	Sum
A	2	2	3	2	4	2	1	2	18
B	2	3	2	1	2	3	2	3	18
C	1	2	1	3	3	4	3	1	19

Table 5. Simulation cases under different product mix and inter-arrival rate

Alternative #	Product mix	Inter-arrival rate
1	A	Low
2	A	Medium
3	A	High
4	B	Low
5	B	Medium
6	B	High
7	C	Low
8	C	Medium
9	C	High

4.3 Simulation Output Analysis

Two criteria, total transportation time and vehicle busy rate, are observed in analyzing simulation outputs, both of which center on evaluating the material handling performance of the two layout alternatives. Space efficiency, initial investment and toolset utilization are also important in comparing fab layout alternatives (Quinn and Bass, 1999). First, related to the space efficiency, it will be mentioned in section 5. Next, the initial investment is assumed to be about the same because both the alternatives use the same number of the toolsets. Note that the initial investment highly depends on the toolset count in the layout. Finally, the impact of the hexagonal layout on the toolset utilization will be discussed at the end of this section.

As seen in figures 5 to 8, the hexagonal semiconductor layout outperforms the unified layout in all the test cases. <Figure 5> shows the average total transportation times under three different arrival rates, low, medium, and high. The hexagonal semiconductor layout yields less total transportation times for all three different cases. In addition, as the arrival rate increases the gap of the total transportation time between the hexagonal and unified semiconductor layout tend to be larger as observed by the line in the figure. The highest gap in percentage is about an hour that is 16% less transportation time in the hexagonal semiconductor layout. <Figure 6> shows the average total transportation times under different product mix scenarios, A, B, and C, as shown in <Tables 4> and <Table 5>. It is clearly shown that the hexagonal layout performs better than the unified layout under different product mix scenarios as well.

Similar observations are obtained with the OHT vehicle utilization metric. <Figure 7> shows the OHT busy rates under different arrival rates and <Figure 8>. presents the busy rates under different product mix scenarios. All the results

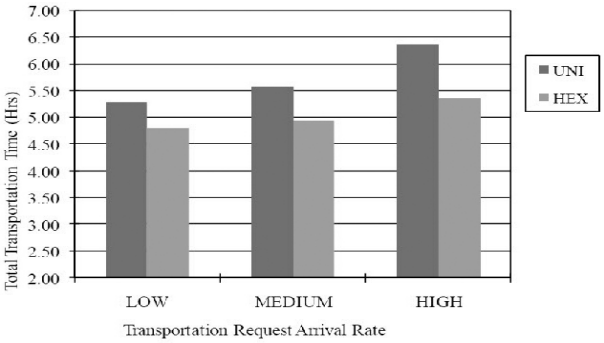

Figure 5. Total transportation time under different request arrival rates

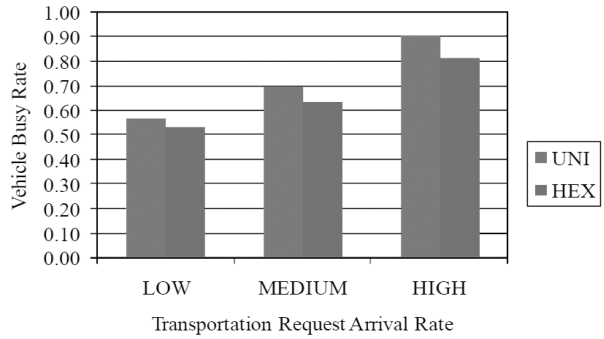

Figure 6. OHT busy rate under different request arrival rates

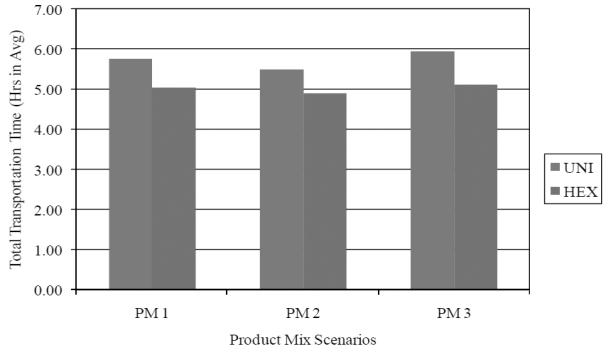

Figure 7. Total transportation time under different product mix scenarios

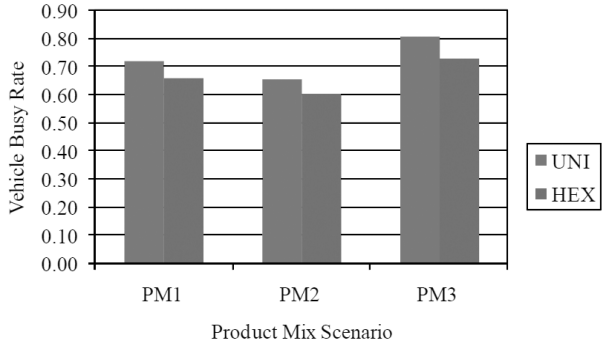

Figure 8. OHT busy rate under different product mix scenarios

consistently indicate the better performance of the hexagonal layout compare to the unified layout. These results show about 4% to 8% better performance in percentages. <Figure 9> shows the simulation screen by FACTOR/AIM.

A consistent result is presented in <Table 6> that compares the hexagonal layout with the unified layout in various statistics under different product mix scenarios. The statistics include transportation times in average, standard deviation, minimum, and maximum. Note that the average transportation times in <Table 6> are the same as ones in <Figure 7>. As observed in the table, the hexagonal layout performs better than the unified layout in all the statistics. A similar result was obtained in the analysis under different arrival rates that presented in <Figure 5> and we skip the detail.

Table 6. Performance of hexagonal and unified layouts under different product mix scenarios

(unit : hours)

Product mix	Criteria	Hex	Uni
PM 1	Average	5.05	5.76
	Std Dev	0.28	0.52
	Min	4.79	5.27
	Max	5.43	6.48
PM 2	Average	4.91	5.50
	Std Dev	0.10	0.19
	Min	4.78	5.27
	Max	5.03	5.74
PM 3	Average	5.12	5.96
	Std Dev	0.34	0.65
	Min	4.80	5.32
	Max	5.59	6.86

It is known that a good layout reduces bottlenecks; as a consequence, increases toolset utilization. For enhancing the toolset utilization, the hexagonal semiconductor layout takes the advantage of the central pooling effect (Eppen, 1979) by placing the bottleneck (litho) toolsets in the core area. As seen in <Figure 4>, litho toolsets are located in three bays in the unified layout. Consequently, WIP(work-in-process)s in each bay tends to be dedicated to the toolsets located in the bay. However, WIPs in the hexagonal layout could be moved to any toolsets in the core area using the streamlined OHS/OHT loops. As a result, it is expected that the unforced idle time of the litho toolsets by lacking available WIPs would be reduced in the hexagonal layout. The authors noted that more precise analysis on the central pooling effect would enrich this study; however, we leave this task for a future study due to the limited boundary of this research.

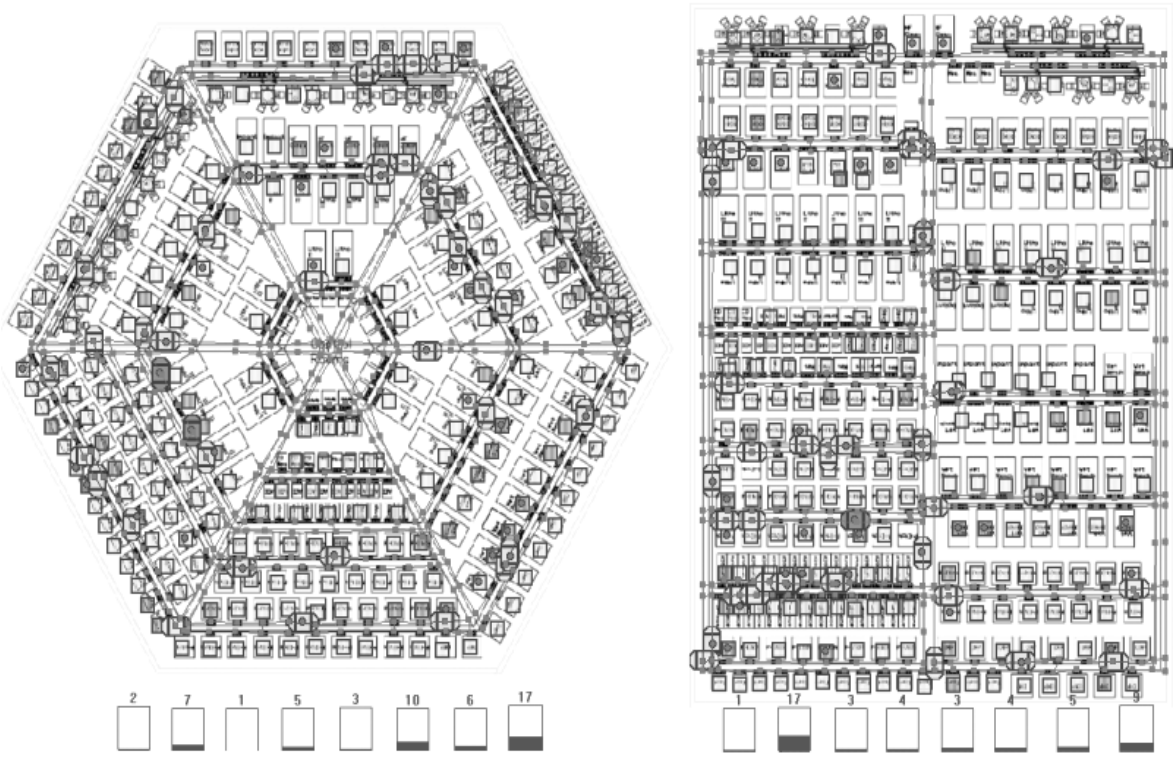

Figure 9. Simulation screen

5. Conclusions

This paper has applied the hexagonal layout for developing a semiconductor fab layout that could be used in practice after slight modification. The industry recently launched project teams to prepare the 450 mm transition, which requires a new type of the fab layout. Based on the two important metrics, the total transportation time and vehicle utilization, this paper showed that the hexagonal semiconductor layout would be a good alternative for the project. One issue raised by practitioners is the space efficiency of the hexagonal semiconductor layout compared to the rectangular unified layout. However, as shown in the drawings above, the same number of toolsets was placed in the same area of the hexagonal layout as the unified layout. The empty spaces in the corners of the hexagonal layout can be used for auxiliary toolsets, storage spaces, and control panels. Another interesting point is that, with the same area, the perimeter of the floor plan is less with the hexagonal layout compared to the conventional rectangular semiconductor layout. This may contribute to saving construction cost of the building. In future study, an economic analysis might be explored to convince that the proposed alternative can be implemented in practice. For this analysis, the two cost factors (i.e., material handling and space usage) might be measured quantitatively.

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