A Gate-Leakage Insensitive 0.7-V 233-nW ECG Amplifier using Non-Feedback PMOS Pseudo-Resistors in 0.13-μm N-well CMOS

Ji-Yong Um, Jae-Yoon Sim, and Hong-June Park

Abstract—**A fully-differential low-voltage low-power electrocardiogram (ECG) amplifier by using the non-feedback PMOS pseudo-resistors is proposed. It consists of two operational-transconductance amplifiers (OTA) in series (a preamplifier and a variable-gain amplifier). To make it insensitive to the gate leakage current of the OTA input transistor, the feedback pseudo-resistor of the conventional ECG amplifier is moved to input branch between the OP amp summing node and the DC reference voltage. Also, an OTA circuit with a *Gm* boosting block without reducing the output resistance (*Ro*) is proposed to maximize the OTA DC gain. The measurements shows the frequency bandwidth from 7 Hz to 480 Hz, the midband gain programmable from 48.7 dB to 59.5 dB, the total harmonic distortion (THD) less than 1.21% with a full voltage swing, and the power consumption of 233 nW in a 0.13 μm CMOS process at the supply voltage of 0.7 V.**

Index Terms—**Electrocardiogram amplifier, pseudo-resistor, gate leakage, low-voltage OTA**

I. INTRODUCTION

Recently, as the interest for U-health increases, the remote patient-monitoring technology has been developed. Among those technologies, the portable heart rate monitors are widely used. In such portable devices, the low power consumption and the small physical size are very important [1-3]. In order to measure the heart rate without disturbing the normal life, the portable device should have a small size and a light weight. Therefore, it uses a small size battery and so it requires a low-voltage and low-power operation.

A crucial building block of the portable heart rate monitor is an ECG amplifier of analog front-end. To measure the heart rate, the amplification and capturing of ECG signal's R-wave is essential. The R-wave has a frequency range between 10 Hz and 15 Hz, and the amplitude between 100 μV and 2 mV [3-5]. In the practical ECG signal acquisition systems, the extracted R-wave can be degraded by disturbances such as motion artifact, dc-offset due to the skin-electrode contact resistance, and the 60 Hz AC power interference. Especially in the portable heart rate monitor, the motion artifacts can cause the largest disturbance, with the frequency components in the range of 1 ~ 5 Hz [5]. Therefore, the motion artifact should be filtered by ECG amplifier. In addition, when the differential electrode offset (DEO) due to the skin-electrode contact resistance is applied to the DC-coupled ECG amplifier, the amplifier output can be saturated. To avoid the output saturation due to DEO, the AC coupling must be used to connect the input signal to the ECG amplifier. Moreover, the human body can easily pick up the 60 Hz common-mode interference signals from the AC power, which are applied to the ECG amplifier as the common-mode signal. Therefore, the ECG amplifier requires the high CMRR.

The conventional ECG amplifier for ECG recorder or heart rate monitor usually utilizes the MOS-bipolar pseudo-resistors or the chopping techniques [6-8].

Among these techniques, the pseudo-resistor based approach gives a small chip area and low-power consumption. However, it has a drawback of the input DC operating-point drift due to the gate leakage current in the sub-0.1-micron CMOS process. Therefore, the design which is insensitive to the gate leakage current is very important in sub-0.1-micron CMOS process.

In the proposed ECG amplifier, the pseudo-resistor in the feedback path of conventional amplifier is removed, so the drift of the input DC operating-point due to the gate leakage current is eliminated. This enables the proposed circuit be used in the sub-0.1-micron CMOS process. Furthermore, the proposed circuit is dedicated to amplify and filter the R-wave of ECG signal, and the DEO due to the skin-electrode contact resistance was removed by the ac-coupling of input signal. The ECG amplifier has a fully differential topology to enhance CMRR.

The paper is organized as follows. Section II describes the architecture of the proposed ECG amplifier. The detailed circuit design and description are presented in Section III. Section IV shows the measurement results. Section V concludes the paper.

II. ECG AMPLIFIER ARCHITECTURE

A simplified architecture of the ECG amplifier is shown in Fig. 1. To reduce the power consumption, the number of stages is minimized to two (preamplifier, variable-gain amplifier). The first stage is a preamplifier which has a band-pass filter characteristic. The second stage is a variable-gain amplifier (VGA) which is able to control the midband gain. The preamplifier has a -3 dB low cut-off frequency between 5 Hz and 10 Hz, and the midband gain of 34 dB. Furthermore, DEO and DC voltage of human body are not applied to the amplifier
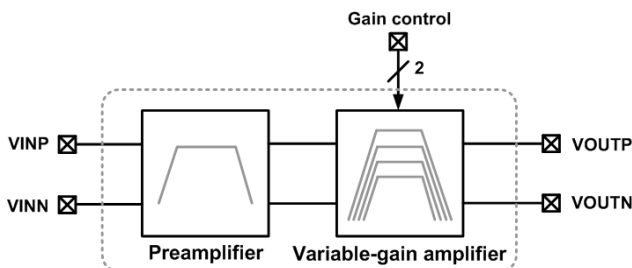

Fig. 1. Architecture of ECG amplifier.

because the input signal is applied to the amplifier through ac-coupling. The VGA also has a band-pass filter characteristic with four selectable midband gains. The ECG amplifier of Fig. 1 operates at the supply voltage below 1 V. The VGA gain is adjusted not to saturate the ECG amplifier output even for the largest input signals.

III. CIRCUIT DESCRIPTION

1. Band-pass Filter Amplifier

Each amplifier of Fig. 1 is designed as a band-pass filter amplifier (BPFA), which uses pseudo-resistors. Fig. 2(a) shows a conventional BPFA [7, 8]. The -3 dB low cut-off frequency is determined by a pseudo-resistor R_1 and a capacitor C_2 in the feedback path. A pseudo-resistor consists of a series connection of two turned-off PMOSFETs ($V_{GS} = 0$). It has a resistance value in the order of 10^{12} Ω. The very large resistance of pseudo-resistor enables the use of moderate valued capacitors to generate a very low frequency pole. In the process with the minimum feature size larger than 0.13 μm, the gate leakage current of the OTA input transistor has a value in the order of 10^{-15} A. The gate leakage current of the OTA input transistor generates the voltage drop of around 1 mV across the pseudo-resistor R_1 in a feedback path. However, in the process with the minimum feature size less than 0.13 μm, a gate leakage in the order of 10^{-13} A flows from the gate of the OTA input transistor to the output node of OTA, and the leakage current generates a voltage drop between 0.1 V and 0.4 V across pseudo-resistor R_1. As a result, the DC voltage of the OTA input node is different from that of the OTA output, and the difference in DC voltage is determined by the un-deterministic leakage current independent of the input signal level. In the worst case, the DC voltage of the OTA input can be located outside the input common-mode range (ICMR) of OTA. Since OTAs should have a high DC gain, the DC voltage drift of the OTA input can decrease a DC gain, and finally degrade the midband gain of BPFA.

Fig. 2(b) shows the circuit diagram of the proposed BPFA. The pseudo-resistor in the feedback path of the conventional BPFA (Fig. 2(a)) is moved to an input path
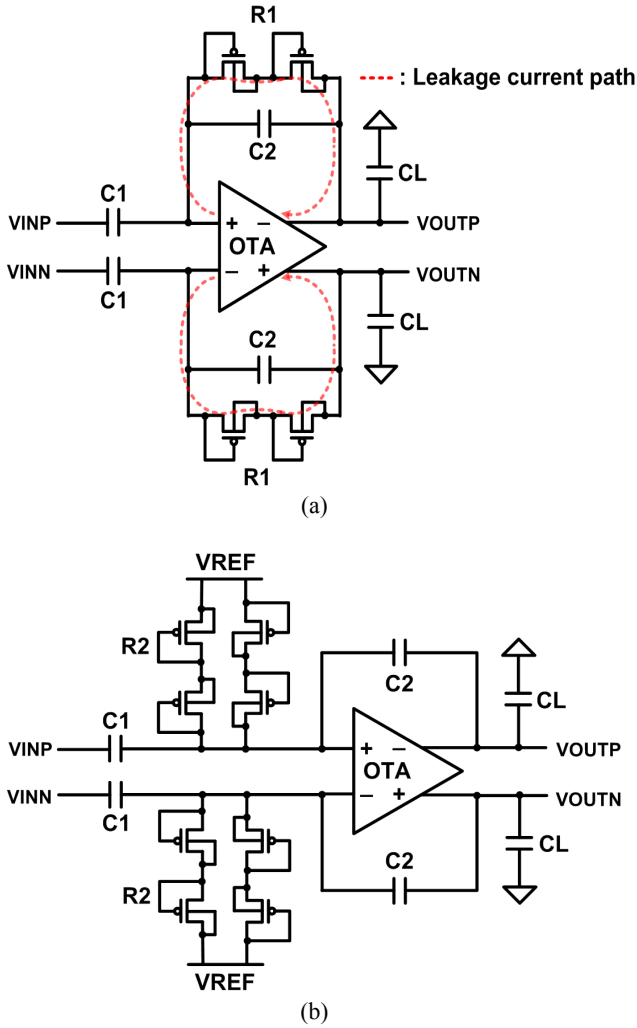
(a)

(b)

Fig. 2. Band-pass filter amplifier circuit. (a) Conventional, (b) Proposed.

between the Op amp summing node and the *VREF* node. Thus, the gate leakage current of the OTA input transistor flows through the pseudo-resistor R_2. However, the resistance value of the pseudo-resistor R_2 in Fig. 2(b) is smaller than R_1 in Fig. 2(a) by the OTA DC gain A, that is $R_2 = R_1/A$. This gives the same low frequency pole ω_L in both Fig. 2(a) and (b). Table 1 shows the comparison of the midband gain, poles, and zero between Fig. 2(a) and (b) where, *Gm* is the differential-mode transconductance of OTA. In this design, the OTA DC gain A is about 73 dB (4000 V/V) according to the SPICE simulation.

Table 1. Comparison of midband gain, pole, and zero between Fig. 2(a) and (b)

	A_M	*zero*	ω_L	ω_H
Fig. 2(a)	C_1/C_2	0	$1/(R_1C_2)$	$Gm/(A_MC_L)$
Fig. 2(b)	C_1/C_2	0	$1/(AR_2C_2)$	$Gm/(A_MC_L)$

Therefore, R_2 has a value (R_1/A), while R_1 has a value in the order of 10^{12} Ω. Thus, the DC voltage drop across R_2 due to the gate leakage current of the OTA input transistor can be neglected in the proposed circuit.

Fig. 3(a) shows the I-V characteristic of the pseudo-resistor R_1 in the conventional circuit (Fig. 2(a)). With a large negative V, R_1 works as a diode-connected PMOS transistor. With a large positive V, R_1 works as a parasitic p-n-p bipolar junction transistor [6]. This makes the I-V characteristic of R_1 very asymmetric for the signal range of V (± 0.25 V). The voltage drop across R_2 is ± 0.25 V/A = ± 62.5 μV for the same output signal level of ± 0.25 V. Also, the symmetric property of R_2 gives a much smaller THD of 0.0142% compared to that of 4.761% for R_1, for the same output signal level of ± 0.25 V. The I-V characteristic of a diode-connected PMOS transistor (W/L = 0.5 μm/10 μm) and a parasitic p-n-p BJT depends on the layout. Thus, R_2 is less sensitive to process variation than R_1.
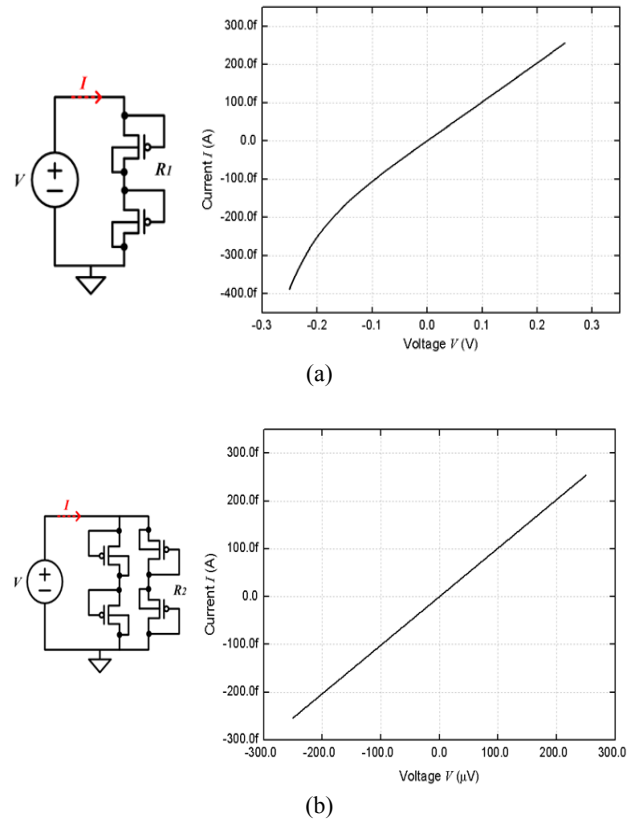

(a)

(b)

Fig. 3. Test circuit and I-V characteristic of pseudo-resistor. (a) Conventional, (b) Proposed.

2. Top-block Circuit Diagram

Fig. 4 shows the top-block circuit diagram. As shown in Fig. 1, the ECG amplifier consists of two stages, a preamplifier and a variable-gain amplifier. The same BPFA circuit as shown in Fig. 2(b) is used at each stage.

The values of C_1 and C_2 are 5 pF and 0.1 pF, respectively. The midband gain of the VGA can be selected by the switch configurations [7]. As shown in the Table 2, there are four levels of selectable midband gain. The capacitance values of C_3, C_4, C_5, C_6, C_{L1}, and C_{L2} are 2 pF, 0.1 pF, 0.1 pF, 0.2 pF, 45 pF, and 50 pF, respectively.

Table 2. Switches configuration for midband gain setting

S1	S2	VGA gain [V/V]
off	off	5
off	on	7
on	off	11
on	on	23

3. Low-voltage Single-stage High-gain OTA

The most important building block of each stage is OTA. The OTA determines the power consumption and the supply voltage of ECG amplifier. The DC gain of OTA determines the -3 dB low cut-off frequency (ω_L) and the midband gain (A_M) of ECG amplifier, as shown in Table 1. When the DC gain (A) of OTA is high, the resistance of pseudo-resistor R_2 which determines the -3 dB low cut-off frequency ω_L can be reduced, since $\omega_L = 1/(AR_2C_2)$. Besides, the DC gain of OTA must be high enough to make the midband gain be insensitive to the OTA DC gain. To reduce the power consumption of ECG amplifier, the number of amplifier stages of an OTA is reduced to a single-stage.

The proposed single-stage OTA circuit is shown in Fig. 5(a). The differential-mode transconductance (Gm) of OTA is increased without reducing the output resistance (Ro). This is achieved by adding a transconductance-boosting block (dotted) between the input and output branches of OTA [9]. The DC gain (A) of the proposed OTA is X/Y times larger than that of the conventional OTA. The values of X and Y are 1.9 and 1/20, respectively, which increases the DC gain (A) by about 30 dB. A differential-amplifier-type CMFB circuit is used in this work (Fig. 5(b)). The power spectral density of the input-referred thermal noise $\overline{v_{in.OTA}^2}$ of the OTA can be derived as
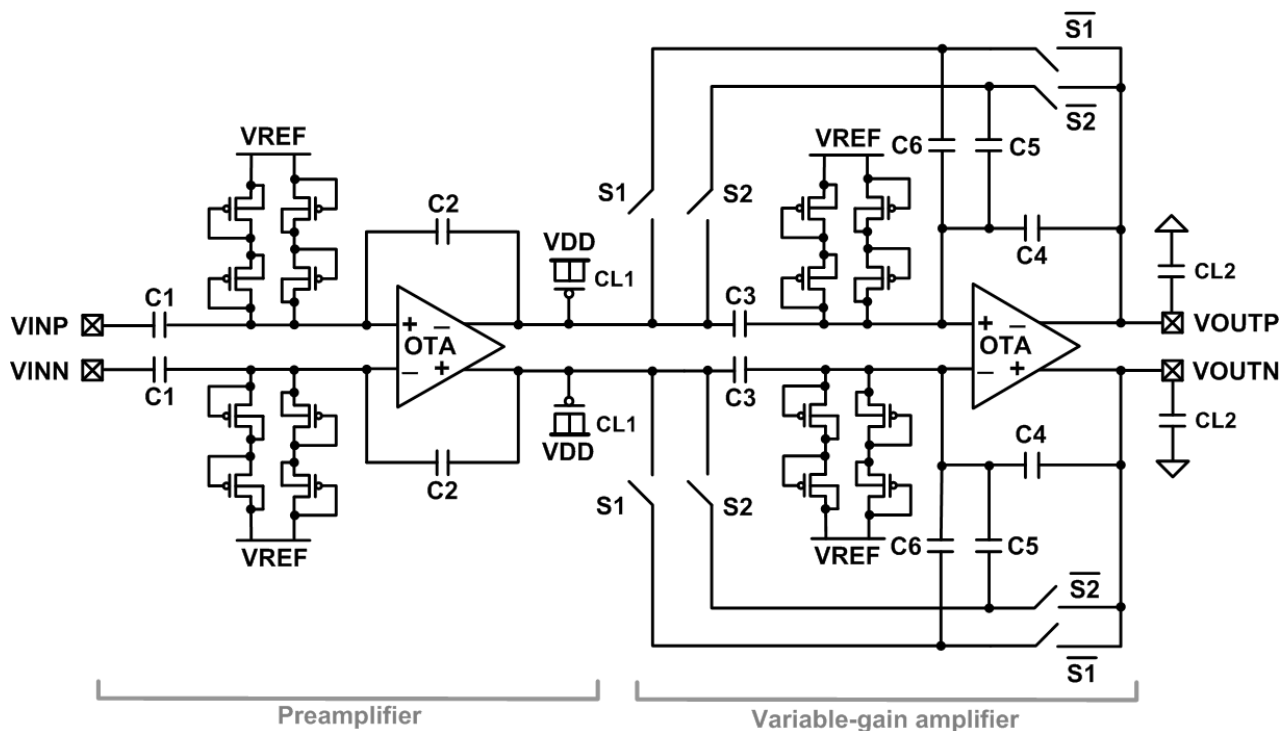

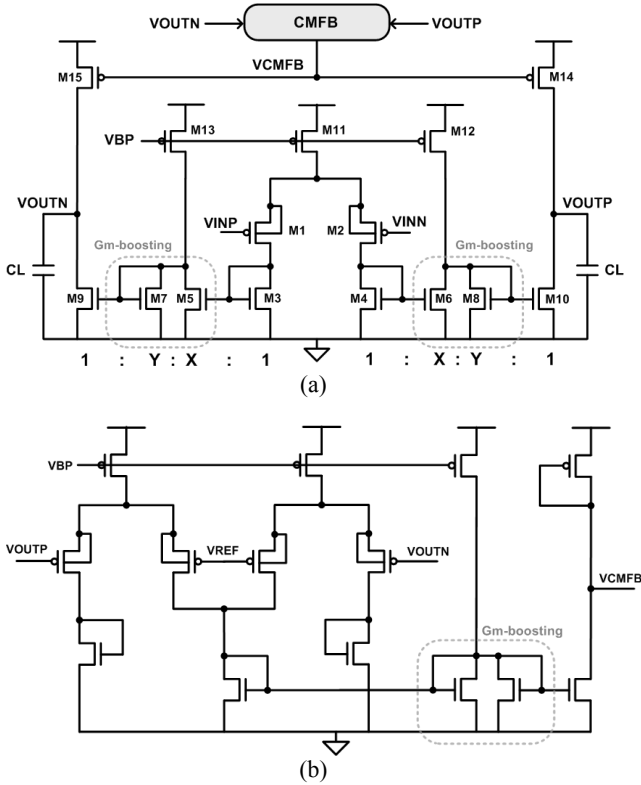**Fig. 4.** Top-block circuit diagram.

Fig. 5. (a) Proposed low-voltage single-stage high-gain OTA, (b) CMFB circuit of the OTA.

$$\overline{v_{in.OTA}^2} \approx \frac{8kT\gamma}{g_{m1}}(1+\frac{g_{m3}}{g_{m1}}+\frac{g_{m5}}{g_{m1}}\frac{1}{X}+\frac{g_{m11}}{2g_{m1}})\frac{Y}{X}. \quad (1)$$

To minimize $\overline{v_{in.OTA}^2}$, the transconductance of the input transistor (g_{m1}) should be maximized. By making the input transistors M1 and M2 to operate in the sub-threshold region, g_{m1} is maximized at a given current consumption. As shown in Eq. (1), the noise contribution of the transistor M5 of the transconductance-boosting block is not negligible. (The simulated input-referred total noise voltage of the ECG amplifier is 42 μV_{rms} with the amplifier bandwidth of 300 Hz)

IV. MEASUREMENT RESULTS

The proposed design was fabricated in a 0.13 μm standard CMOS process. The chip is tested at the supply voltage 0.7 V. Fig. 6 shows the measured frequency response of the fabricated chip. The midband gain is controlled by the switches ($S1$ and $S2$) of VGA, and the values are 48.7, 50.1, 54.1, and 59.6 dB. The measured -

3 dB low cut-off frequency ($\omega_L/2\pi$) ranges from 7 Hz to 8 Hz, which can filter the motion artifact sufficiently. The -3 dB high cut-off frequency ($\omega_H/2\pi$) ranges from 280 Hz to 475 Hz.

Fig. 7 shows the measured total harmonic distortion (THD) for the differential output voltage. Both THD and the midband gain (A_M) increases as the differential output voltage increases. THD is measured to be 1.21% when the differential output voltage is 0.5 V_{PP} (amplitude 0.25 V).

Fig. 8(a) shows the artificial ECG signal which is generated by an arbitrary waveform generator (AP, SYS-2722) from the MATLAB generated data [10]. Fig. 8(b) is the measured output voltage waveform. The measured amplitude of output waveform is 380 mV, and the R-wave which is the peak signal of ECG signal is well-detected.

Fig. 9 shows the chip layout and die micrograph of ECG amplifier. The area of the designed ECG amplifier is 800 × 490 μm^2. Table 3 shows the summary of measured performance of the proposed ECG amplifier. The
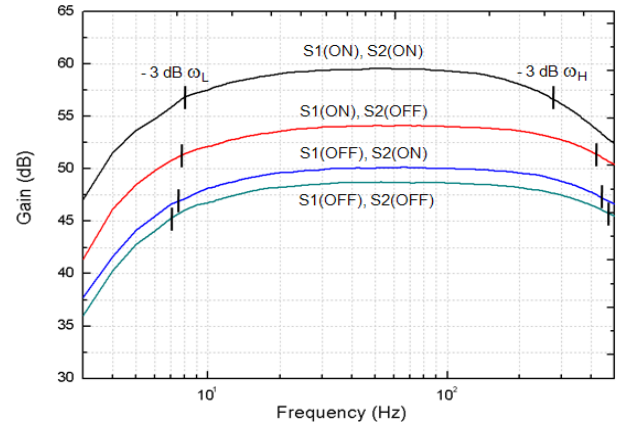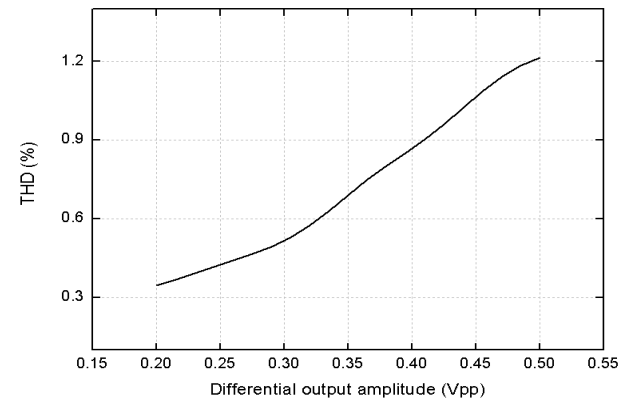

Fig. 6. Frequency response.
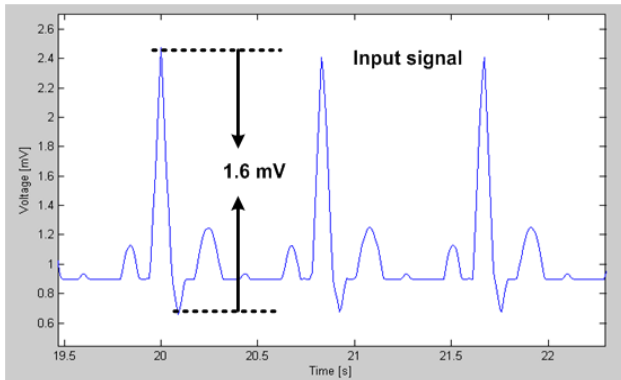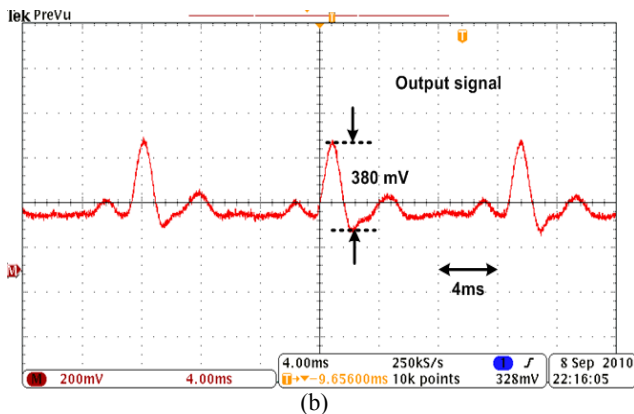

Fig. 7. Total harmonic distortion.

(a)

(b)

Fig. 8. (a) ECG input signal, (b) Measured output signal.
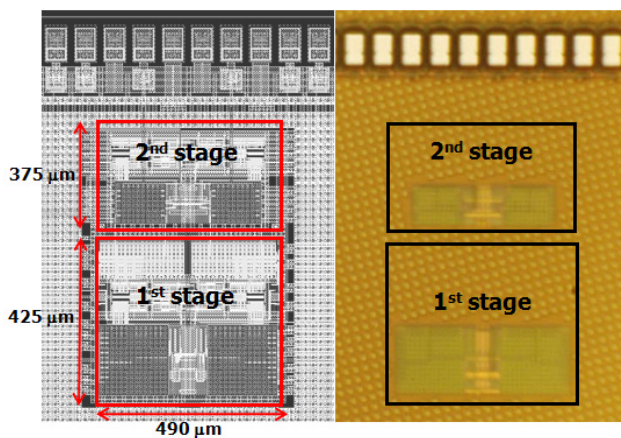

Fig. 9. Layout and die micrograph.

designed ECG amplifier has the lowest supply voltage of 0.7 V compared to the published ECG amplifiers [4, 6-8]. Although the simulated CMRR is 110 dB, the measured CMRR is 80 dB. This discrepancy is considered to be due to the mismatch of pseudo-resistors and OTA circuits in the two differential branches. The power consumption is 233 nW. The current consumption of preamplifier and VGA is 258 nA and 75 nA, respectively.

Table 3. Measurement summary

Process	1P 6M 0.13 μm CMOS
Supply voltage	0.7 V
Midband gain (A_M)	48.7 / 50 / 54 / 59.5 dB
Low cut-off frequency ($\omega_L/2\pi$)	7 ~ 8 Hz
High cut-off frequency ($\omega_H/2\pi$)	280 ~ 480 Hz
CMRR @ min. midband gain	> 80 dB (below 240 Hz)
THD @ max. A_M & output swing	1.21%
Active area	0.392 mm^2
Power consumption	233 nW
Max. output swing	$\pm$ 0.5 V$_{PP}$ (differential)

V. CONCLUSIONS

The low-voltage low-power ECG amplifier using the non-feedback PMOS pseudo-resistor is presented. The proposed circuit is designed and fabricated using a 0.13 μm standard CMOS process. In order to reduce power consumption, the number of stages is reduced as possible, and a simple band-pass filter amplifier is utilized as a basic scheme. A conventional band-pass filter amplifier can be affected by a gate leakage current in sub-0.1-micron CMOS process. The scheme which can overcome the performance degradation due to a gate leakage current is proposed. To support low supply operation of the ECG amplifier, low-voltage high DC gain single-stage OTA is proposed. The ECG amplifier operates at the supply voltage of 0.7 V. The power consumption of the fabricated chip is 233 nW. The ECG amplifier has a sufficient frequency response for extracting R-wave from ECG signals.

ACKNOWLEDGMENTS

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