A 67.5 dB SFDR Full-CMOS VDSL2 CPE Transmitter and Receiver with Multi-Band Low-Pass Filter

Joon-Sung Park, Hyung-Gu Park, YoungGun Pu, and Kang-Yoon Lee

***Abstract*—This paper presents a full-CMOS transmitter and receiver for VDSL2 systems. The transmitter part consists of the low-pass filter, programmable gain amplifier (PGA) and 14-bit DAC. The receiver part consists of the low-pass filter, variable gain amplifier (VGA), and 13-bit ADC. The low pass filter and PGA are designed to support the variable data rate. The RC bank sharing architecture for the low pass filter has reduced the chip size significantly. And, the 80 Msps, high resolution DAC and ADC are integrated to guarantee the SNR. Also, the transmitter and receiver are designed to have a wide dynamic range and gain control range because the signal from the VDSL2 line is variable depending on the distance. The chip is implemented in 0.25 μm CMOS technology and the die area is 5 mm × 5 mm. The spurious free dynamic range (SFDR) and SNR of the transmitter and receiver are 67.5 dB and 41 dB, respectively. The power consumption of the transmitter and receiver are 160 mW and 250 mW from the supply voltage of 2.5 V, respectively.**

***Index Terms*—Transmitter, receiver, VDSL2, ADC, DAC, SFDR, SNR**

I. INTRODUCTION

The VDSL2 (Very High Speed Digital Subscriber Line 2) is an access technology that exploits the existing infrastructure of copper wires that were originally deployed for POTS services. The VDSL2 is the newest and most advanced standard of DSL broadband wireline communications. In order to support the wide deployment of Triple Play services such as voice, video, data, high definition television (HDTV) and interactive gaming, the VDSL2 enables operators and carriers to upgrade existing xDSL-infrastructure in a flexible and cost efficient way [1].

It has been standardized as ITU G.993.2. ITU-T G.993.2 (VDSL2) is an enhancement to G.993.1 (VDSL1) that permits the transmission of asymmetric and symmetric (Full-Duplex) aggregate data rates up to 200 Mbps on twisted pairs using a bandwidth up to 30 MHz. While the VDSL1 standard uses the band plan that defines the spectrum up to 12 MHz, the VDSL2 standard defines the band plan and spectrum up to 30 MHz. Fig. 1 shows the band plan of the DSL.

Thanks to the increasing bandwidth, the VDSL2 can provide the total data rate (including up-link and down-link) over 200 Mbps at a short loop. The VDSL2 has a superior performance than the VDSL1 in terms of the data-rate, improved function such as impulse noise protection and circuit diagnostics.

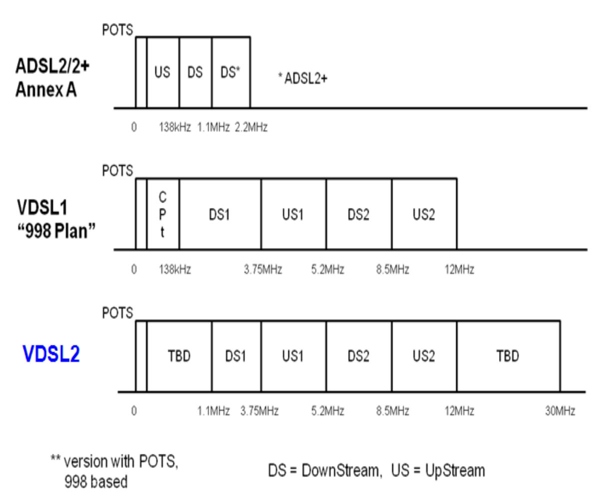

Fig. 1. Band plan of DSL.

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Thus, there are some design issues to implement the VDSL2 system [2].

First, the programmable low-pass filter is required because the data rate is variable from 138 kHz to 30 MHz. The efficient filter architecture to share the capacitance between different data-rates is proposed in the paper to reduce the die area.

Second, high-speed ADC and DAC are designed to support the maximum data rate of 30 MHz. Also, in order to guarantee the SNR, the resolution of ADC and DAC is designed as 13 bits and 14 bits, respectively.

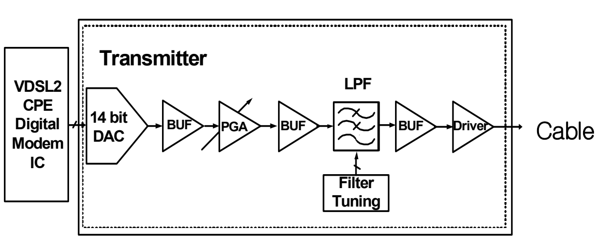
Third, the bandwidth of the operational amplifier is designed to be large enough to process the data rate of 30 MHz.

In this paper, system architecture and building blocks to meet the requirements of VDSL2 system are presented.

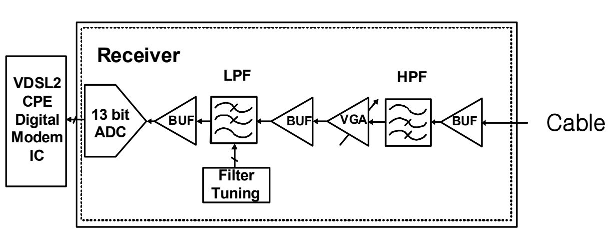
The paper is organized as follows. In Section II, the proposed VDSL2 AFE (Analog Front-End) architecture is shown and its problems and proposed solutions are discussed. Section III describes various building blocks and circuits for use in building the chip. Section IV shows experimental results from 0.25 μm CMOS implementation and Section V concludes the paper.

II. System Architecture

Fig. 2(a) and (b) show the block diagram of the transmitter and receiver part of the VDSL2 AFE (Analog Front-End), respectively.



(a)



(b)

Fig. 2. Block diagram of (a) Transmitter, (b) Receiver.

The transmitter is composed of a 14-bit DAC, a PGA, a low-pass filter with a tuning circuit, a driver and buffers [3, 4]. The 14-bit DAC receives data from VDSL2 CPE (customer premises equipment) Digital IC and operates at 80 Msps. The PGA is controlled digitally by CPE Digital IC. And, its gain control range is -24 dB ~ 0 dB and the gain control step is 1 dB. The low-pass filter supports the programmable cut-off frequency (138 kHz, 276 kHz, 12 MHz, 30 MHz). The filter is automatically tuned to the cut-off frequency by the tuning circuit.

The receiver is composed of a 13-bit ADC, a VGA, a high-pass filter, and a low-pass filter with tuning circuit [5]. The ADC operates at the sampling rate of 80 Msps and is designed to have the resolution of 13-bits to guarantee the SNR. The high-pass filter (HPF) cancels the DC-offset in the input signal. The low-pass filter is implemented in active-RC, third-order Chebyshev type and has four cut-off frequencies (3.75 MHz, 12 MHz, 18.1 MHz, 30 MHz). To compensate the RC time constant variation, the automatic tuning circuit is used. And, the capacitance arrays and resistor arrays in active-RC filter are shared among the four bandwidth tuning circuits to reduce the area.

III. Building Blocks

1. Programmable Low-pass Filter of Transmitter

The channel selection low-pass filter in the transmitter has programmable bandwidth (138 kHz, 276 kHz, 12 MHz and 30 MHz) and can attenuate the adjacent channel interferer based on the four cut-off frequencies.

When the low-pass filter is implemented in Chebyshev type, the size of the minimum capacitance is very small (less than 100 fF) for the cut-off frequency of 30 MHz. Thus, 7^{th}-order Butterworth filter is adopted to increase the minimum capacitance above 100 fF [6]. Fig. 3(a) shows the 7^{th}-order active-RC Butterworth filter. In order to have a sufficient attenuation characteristics, superior performance folded cascade operational amplifier is designed. It has the DC gain of 60 dB and unity gain frequency of 1 GHz at the current consumption of 6 mA to cover the wide bandwidth.

The noise level of the filter is optimized to guarantee

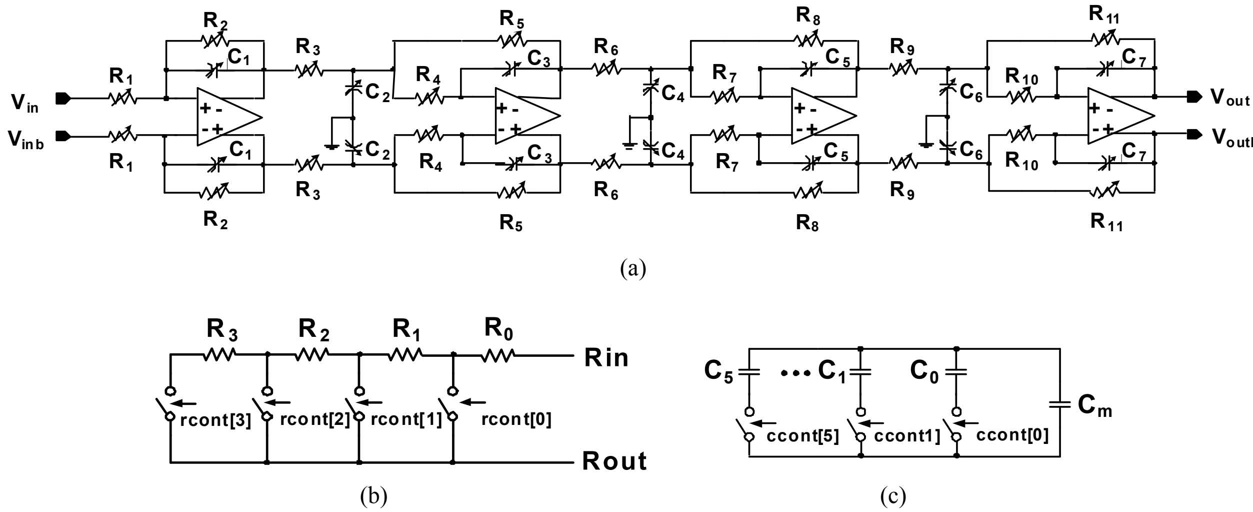


Fig. 3. (a) Block diagram, (b) Resistor bank and (c) Capacitor bank of Active-RC 7th-order Butterworth filter.

the minimum SNR of the transmitted signal and the linearity of the filter is also maximized to suppress the non-linearity components when the signal level is high [7]. Thus, the operational amplifier in the filter is designed to have low input-referred noise for the SNR and high DC gain for better linearity. Effective resistances in the active-RC filter depend on the cut-off frequency (138 kHz, 276 kHz, 12 MHz and 30 MHz). As shown in Fig. 3(b), resistor banks with four resistors and transmission gate type switches are used to implement the multi-band filter. Capacitance varies by about 15% due to the process variation and leads to the fluctuation of the cut-off frequency. To tune the cut-off frequency, variable capacitors, C_{t0} ~ C_{t5}, are used and controlled by the tuning block. Cut-off frequencies are tuned with capacitor arrays composed of capacitors and switches. As shown in Fig. 3(c), variable capacitor consists of a main capacitor C_{tm} and tuning capacitors, C_{t0} ~ C_{t5} [8, 9]. When cut-off frequency is too high, the total capacitance value is increased. On the other hand, if the cut-off frequency is too low, the total capacitance value should be increased.

Proposed tuning circuit for active-RC transmitter and receiver filter are shown in Fig. 4(a). It is composed of reference voltage generator, integrator, comparator, and counter & algorithm block. The reference clock for the tuning circuit comes from the accurate external clock.

Fig. 4(b) and (c) show the timing diagram and the block diagram of the integrator, respectively. The integrator operates when Q1 is HIGH and amplifies the

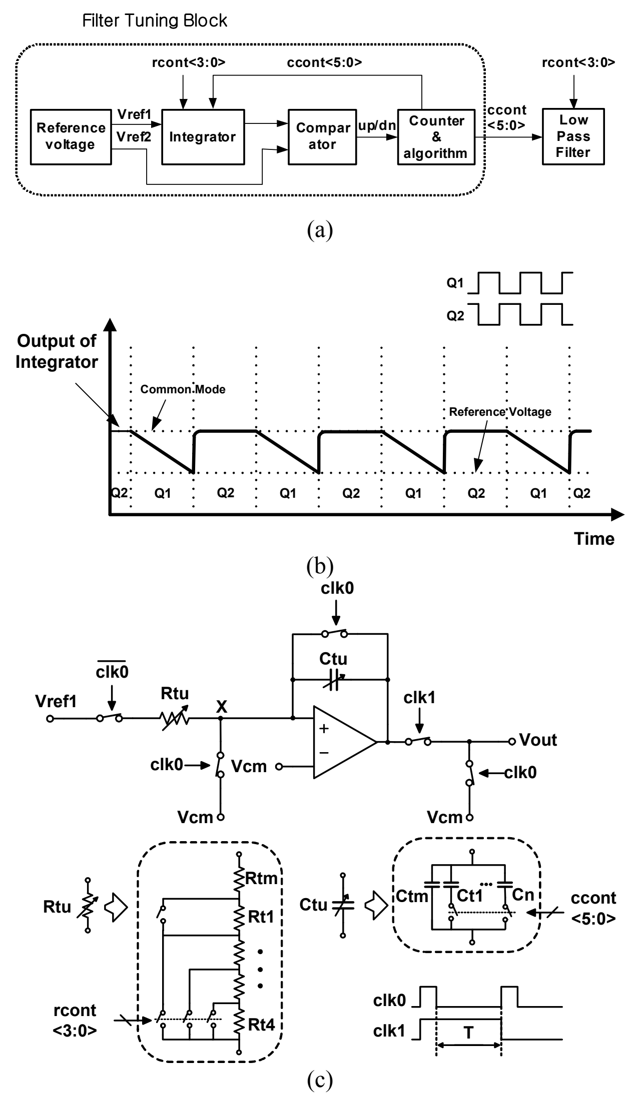


Fig. 4. (a) Block diagram, (b) Timing diagram and (c) Integrator of filter tuning circuit.

signal linearly as determined by the RC slope. When Q2 is HIGH, the comparator compares output voltage of the integrator with the reference voltage.

If the output of the integrator is less than the reference voltage, "dn" signal is applied to the counter. Then the counter decreases the digital code that controls the capacitor array resulting in increasing the RC slope. In Fig. 4(c), op-amp of integrator is equal to that of low-pass filter. And, C_{tu} is the same capacitor array as that of the low-pass filter for matching characteristics. As can be seen in Fig. 4(c), when clk0 and clk1 are both high, X node and V_{out} are equal to V_{com}. When clk0 is changed to low and clk1 is high, V_{out} changes as Eq. (1)

$$V_{out} = V_{com} - \frac{1}{RC_{tu}}\left(V_{ref} - V_{com}\right)T \qquad (1)$$

In Eq. (1), T is determined from exact external reference clock. If C_{tu} is too large, V_{out} becomes too low causing C_{tu} to be decreased. On the other hand, if C_{tu} is too small, V_{out} is too high causing C_{tu} to be increased. R_{tu} in Fig. 4(c) is selected by rcont<3:0> to tune the channel bandwidth.

2. Programmable Gain Amplifier of Transmitter

The PGA of the transmitter is shown in Fig. 5(a). It is composed of Op-amp, gain control switch, voltage divider using resistor.

In order to adjust the output level of the DAC to the input range of the low-pass filter, the PGA in the transmitter can provide the positive or negative gain. The gain control range of 24 dB can be adjusted digitally in 1 dB step. The baseband modem adjusts the gain of PGA automatically.

The negative gain of PGA can be implemented through the voltage division with R_4 and R_5 as shown in Fig. 5(a).

Accurate gain step of 1 dB can be achieved using resistors and switches. The values of resistors are selected carefully to minimize the gain error and thermal noise. The gain of PGA can be represented as Eq. (2),

$$A_V = \frac{R_2 + R_3}{R_1} \times \frac{R_5}{R_4 + R_5} \qquad (2)$$

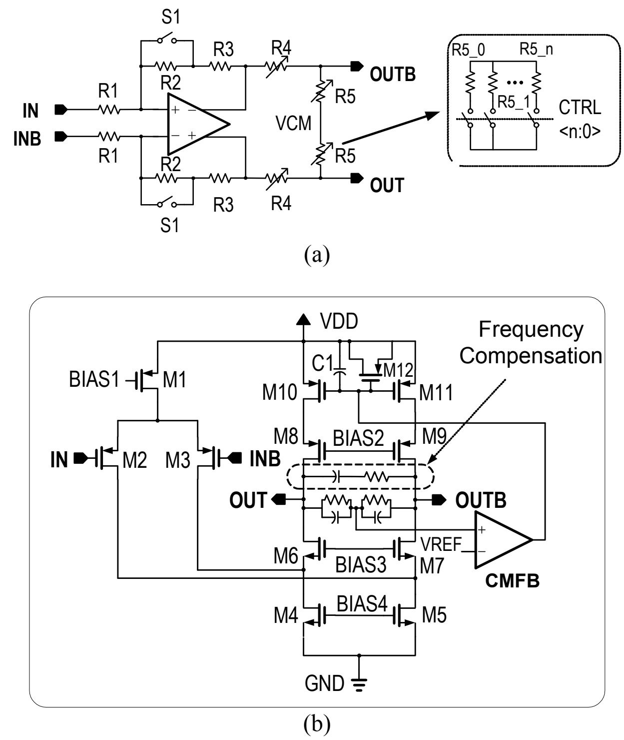


Fig. 5. (a) Block diagram, (b) Op-amp of PGA of transmitter.

Op-amp in Fig. 5(b) is folded cascode type. Due to its high gain characteristics, the frequency compensation and CMFB (Common Mode Feedback) circuit is added [10]. In order to alleviate the common mode oscillation due to the CMFB, the gain of op-amp and current of CMFB are optimized. For the case of the high voltage swing condition of the VDSL2 transmitter, the linearity is one of the most important issues. Thus, in order to obtain the good linearity and guarantee the wide bandwidth of 30 MHz, the PGA is designed with the feedback topology and the current of the Op-amp is designed to be 24 mA.

3. Low-pass Filter of Receiver

The dynamic range of the signal and high frequency noise from the cable are too large. Thus, the received signal should be amplified adaptively and the high frequency and low frequency noise should be rejected through the low pass filter. Also, its DC offset should be cancelled [11].

Fig. 6(a) shows the circuit diagram of low pass filter with resistor array, which is the 3^{rd}-order, Chebyshev active-RC filter. This type has somewhat large pass-band ripple, but has sharp attenuation characteristic. In this

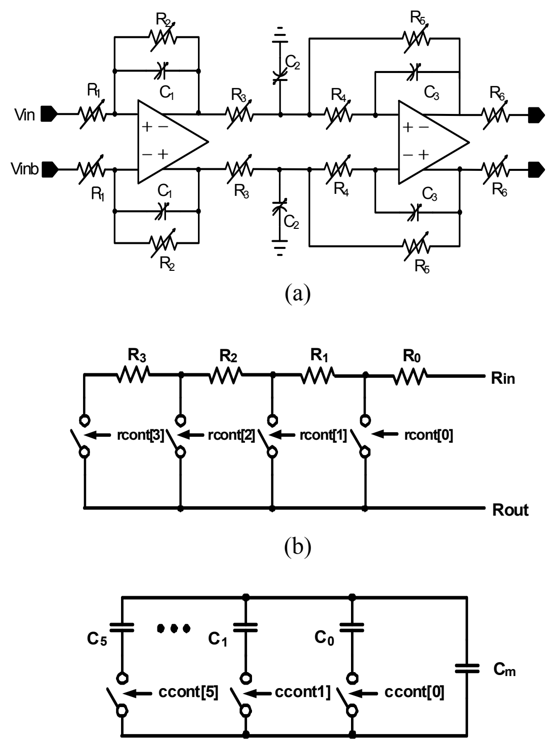


Fig. 6. (a) Block diagram, (b) Resistor bank and (c) Capacitor bank of Active-RC 3rd order Chebyshev filter.

work, to minimize the pass-band ripple, the amplifier characteristic and capacitor and resistor value are optimized. Resistor banks and capacitor banks are used for the multi-band low pass filter.

The low pass filter has four cut-off frequencies (3.75 MHz, 12 MHz, 18.1 MHz and 30 MHz). Multiband cut-off frequencies could be realized by employing the resistor banks and capacitor banks. The resistor banks shown in Fig. 6(b) consist of resistors and control switches. And, the capacitor banks shown in Fig. 6(c) consist of capacitors and control switches. The control switches of capacitor banks are controlled by the control bits from the automatic filter tuning block. If the cut-off frequency is too high, the effective capacitance of the capacitor banks should be decreased to adjust the cut-off frequency to higher frequency. On the other hand, if the cut-off frequency is too low, the effective capacitance should be increased.

Die area is one of the important issues of the transceiver. Since capacitors in the low pass filter occupy large area, we proposed the efficient architecture to share them among four cut-off frequencies. Resistor bank consisting of resistor array and switches, and capacitor bank consisting of capacitor array and switches are shared to implement the four cut-off frequencies by the control bit from the serial peripheral interface (SPI). This sharing scheme has reduced the die area drastically.

4. Variable Gain Amplifier of Receiver

Because of the very large dynamic range of the signal from the VDSL2 line, the VGA is designed to operate at rail-to-rail and its noise should be minimized. The input range is about 0.1 V to 2.5 V and its noise level is designed to be about 10 nV/√Hz [12].

Fig. 7 shows the schematic of the VGA architecture and resistor array. The VGA is designed to have the wide dynamic range and its gain is controllable by 6 bits from decoder controlled by the modem system.

The gain control scheme using the resistor bank is used in this design. The gain of VGA is controlled digitally by the digital modem. The gain range is from 0 dB to 40 dB and the gain step is 2 dB. The gain, A_v, is determined by the ratio of R_1 and R_2, so R_2 is composed of programmable resistors and switches.

$$A_V = \frac{V_{out} - V_{outb}}{V_{in} - V_{inb}} = -\frac{R_2}{R_1} \quad (3)$$

Because the gain is controlled by the relative ratio of R_1 and R_2, the variation of the gain is small. Because the gain is controlled digitally by CTRL<5:0>, it is easy to design the gain range and steps. The switch control signals CTRL<5:0> are controlled by the VDSL2 modem. The number of switch and resistor sets is determined by the gain control step and total gain.

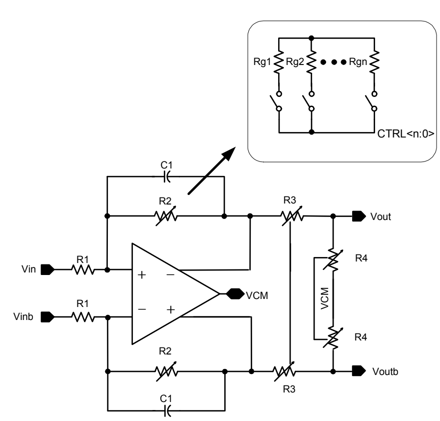


Fig. 7. Variable gain amplifier of receiver.

The cut-off frequency of the DC-offset cancellation block is 10 kHz and the DC component is attenuated by 100 dB.

5. Digital-to-Analog Converter

The 14-bit, 80 Msps DAC structure is shown in Fig. 8. Thermometer current steering array architecture has a good linearity, but it needs large area. On the other hand, binary current steering array needs a small area, but it has a large non-linearity due to mismatches. In this work, partially segmented current steering DAC architecture is used for small area and good linearity [13]. The 4-bit LLSB (Lower Least Significant Bit) array is implemented with binary-weighted current steering array and the 5-bit ULSB (Upper Least Significant Bit) array is implemented with thermometer-weighted current steering arrays. As a result, the overall resolution of DAC is 14 bits.

The clock generator generates 3 phase clocks from single clock input. The clock generator supplies timing for Buffer and Register and 4-bit LLSB array, 5-bit ULSB array, 5-bit MSB array. The voltage bias block supplies bias voltages to current steering circuit of each array. Each bias voltage is adjustable from control signals, IB<1:0>. The current folder & output driver block converts the DAC current proportional to the digital input into the output voltage. Output voltages of the current folder & output driver, Vout and Voutb, are tunable through the control signals, IF<1:0>, to compensate for the temperature and process variation.

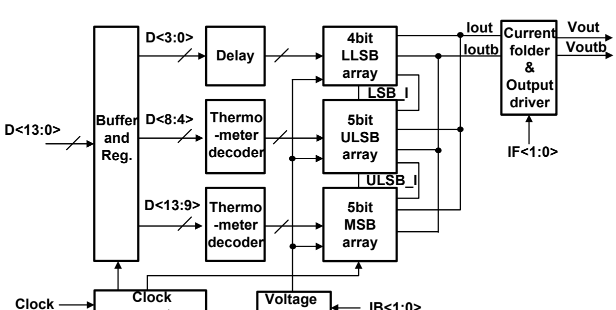


Fig. 8. Block diagram of DAC.

6. Analog-to-Digital Converter

For VDSL2 application, high SFDR, high sampling rate and high resolution are required for ADC. Thus, ADC should have the resolution of 13-bits, sampling rate of 80 Msps, SFDR of 75 dBc and input range of 2 Vpp. In this work, the pipeline architecture is used for high speed and low power consumption.

Fig. 9 shows the 13-bit, five stage pipeline ADC structure. Each stage is composed of 3-bit MDAC (Multiplying DAC) and Flash ADC [13].

Voltage reference1 and voltage reference2 generate reference voltages for MDACs and Flashes. The clock generator provides the clocks to S&H, MDACs and Flashes from one clock source. The current bias provides the bias currents to S&H, MDACs and Flashes. It can be controlled by external SPI bits, ICONS<3:0> and ICON<3:0>.

When analog signal is applied to the input of ADC, S&H circuit samples and holds it. Since the sampling rate is 80 Msps and resolution is 13 bits, the gain and bandwidth of the op-amp should be large enough. Flash ADC in each stage converts the input signal into 3-bit digital code. MDACs evaluate the residue and multiply it to the range of Flash ADC. The DCL(Digital Correction Logic) takes 3-bit digital code from Flash ADC and performs the error correction.

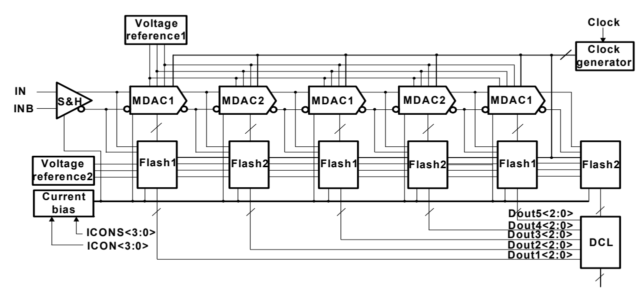


Fig. 9. Block diagram of ADC.

IV. EXPERIMENTAL RESULTS

This chip is fabricated in CMOS process with a feature size of 0.25 μm technology, a single poly layer, five layers of metal. The die area is 5 mm × 5 mm. Fig. 10 shows the chip layout pattern.

Fig. 11 shows the simulation result of the 7th-order active-RC Butterworth filter in transmitter. It has four cut-off frequencies (138 kHz, 276 kHz, and 12 MHz. 30 MHz). Thus, the capacitance arrays and resistor arrays in active-RC filter are shared among the four bandwidths to reduce the area.

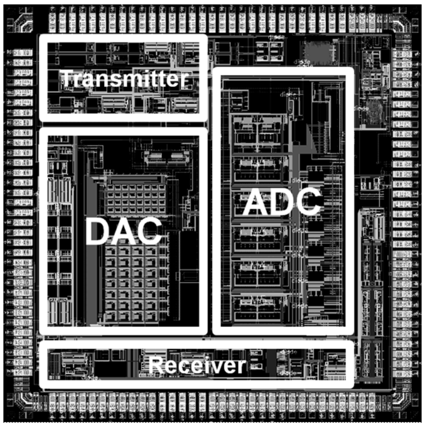


Fig. 10. Chip layout pattern.

Fig. 12 shows the simulation result of PGA in the transmitter. Maximum gain of PGA is 0 dB and can be boosted to 6 dB with switch, S1 in Fig. 5(a). The gain control range is 24 dB and gain step is 3 dB.

Fig. 13 shows the simulation result of the 3rd-order active-RC Chebyshev filter in the receiver. It has four cut-off frequencies (3.5 MHz, 12 MHz, 18.1 MHz, and 30 MHz).

Fig. 14 shows the simulation result of the VGA in the receiver.

The gain control range is 40 dB and the cut-off frequency for the DC-offset cancellation is 10 kHz.

Fig. 15 shows the measured spectrum at the output of the receiver. The output of the receiver is connected to the input of the transmitter and SNR of the DAC output is measured. As can be seen in Fig. 15, the SNR of the pass band is 41 dB. The result shows the spectrum of the output of the receiver when the cut-off frequency of the low-pass filter is 30 MHz.

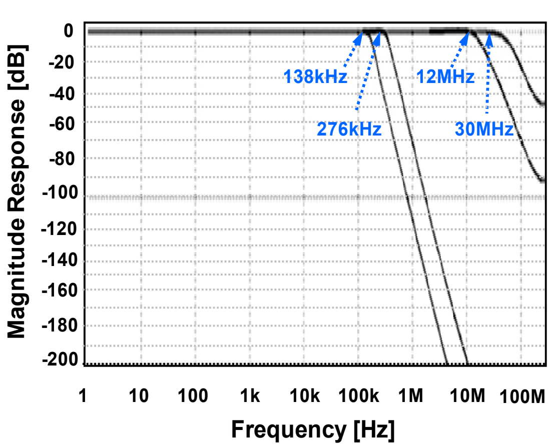


Fig. 11. Simulated frequency response of low-pass filter in transmitter.

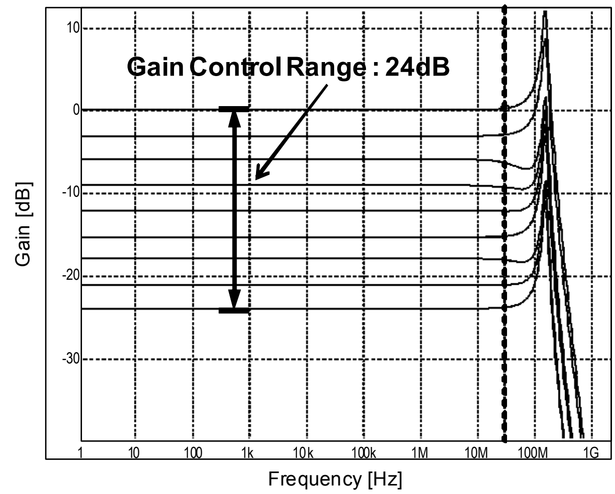


Fig. 12. Frequency response of PGA in transmitter.

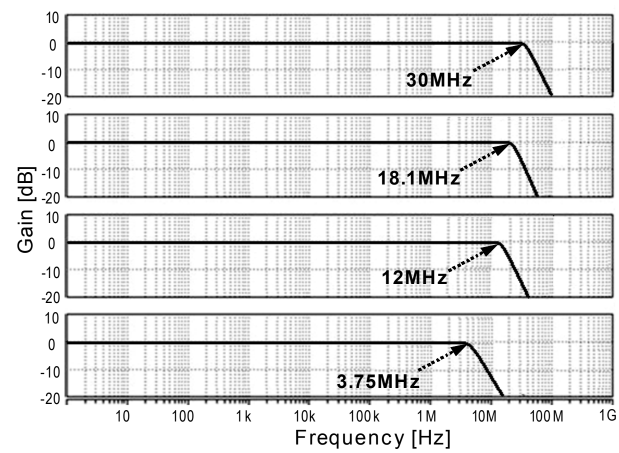


Fig. 13. Frequency response of low-pass filter in receiver.

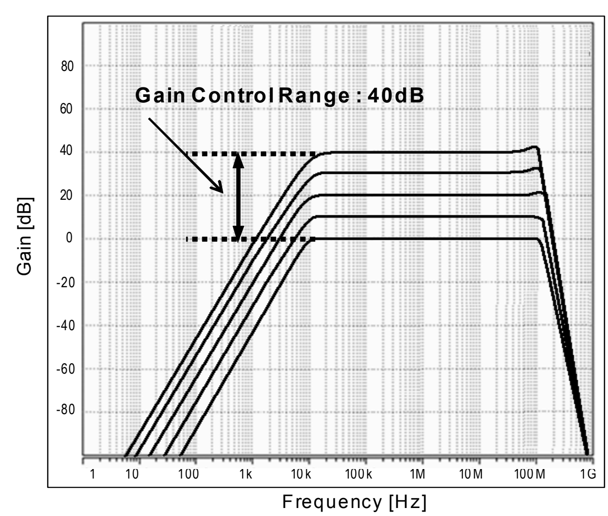


Fig. 14. Frequency response of VGA in receiver.

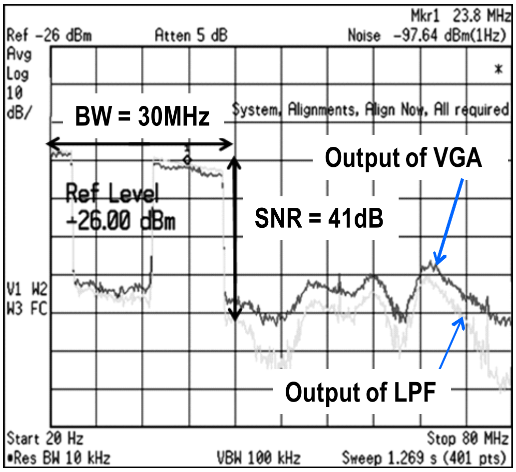


Fig. 15. Measured output spectrum of the receiver.

Fig. 16 shows the measurement spectrum at the output of the transmitter.

As can be seen in Fig. 16, the SNR of the pass band is 41 dB and bandwidth is 30 MHz when the modulated input is applied. Output of low-pass filter at the transmitter is also shown in Fig. 16. The measured result satisfies the specification of VDSL2 system.

To measure the characteristics of the transmitter and receiver, the output of transmitter is connected to the input of the receiver in loop-back. Fig. 17 shows the measurement result of the SFDR at the output of the receiver in loop-back.

SFDR is measured at the output of the receiver when 256 tones are applied to the input of transmitter.

As can be seen in Fig. 17, the measured SFDR is 67.5 dB. It shows that the measured SFDR satisfies the specification of VDSL2 system.

The measured performance is summarized in Table 1.

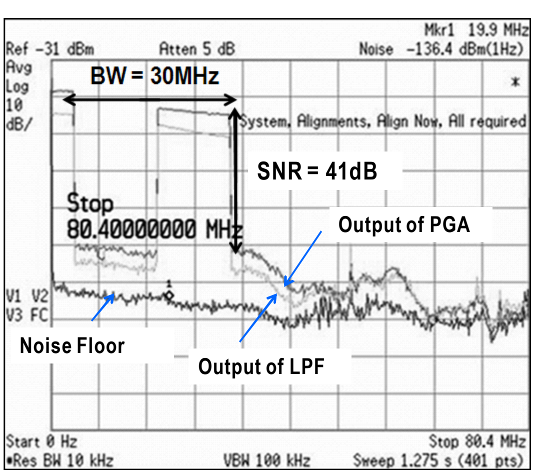


Fig. 16. Measured output spectrum of the transmitter.

Table 1. Summary of measured performance

Technology		0.25 μm CMOS
Die Area		5 mm x 5 mm
SFDR		67.5 dB
SNR (Transmitter/Receiver)		41 dB
Bandwidth	Transmitter	138 KHz ~ 30 MHz
	Receiver	3.75 MHz ~ 30 MHz
Dynamic Range	Transmitter	24 dB
	Receiver	40 dB
Power Consumption	Transmitter	160 mW @ 2.5 V
	Receiver	250 mW @ 2.5 V

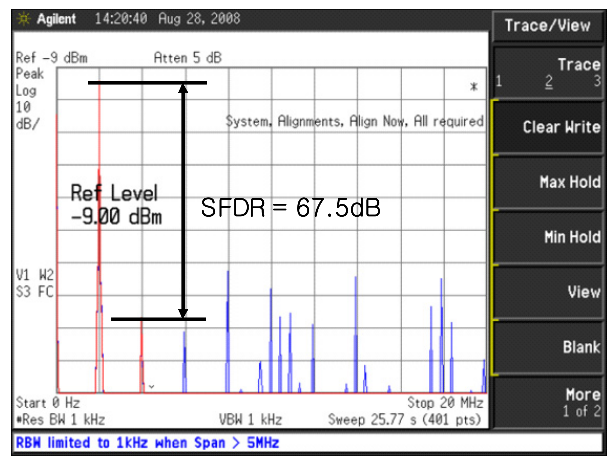


Fig. 17. Measured output spectrum at the output of the receiver in loop-back.

V. CONCLUSIONS

In this paper, we presented a full-CMOS transmitter and receiver for VDSL2 system.

The transmitter consists of the low-pass filter, programmable gain amplifier (PGA) and 14-bit DAC. The receiver consists of the low-pass filter, variable gain amplifier (VGA), and 13-bit ADC. The RC bank sharing architecture for the low pass filter has reduced the chip size significantly. The transmitter and receiver are designed to have a wide dynamic range and gain control range because the signal from the VDSL2 line is variable depending on the distance.

This chip is fabricated in CMOS process with a feature size of 0.25 μm technology, a single poly layer, five layers of metal. The die area is 5 mm × 5 mm. The measured SNR is 41 dB when the modulated input is applied, and can meet the specification of VDSL2. The power consumption is 160 mW in transmitter mode and

250 mW in receiver mode at the supply voltage of 2.5 V.

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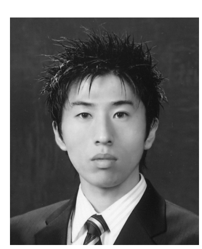

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