A 2.5 V 109 dB DR ΔΣ ADC for Audio Application

Gwangyol Noh and Gil-Cho Ahn

Abstract—**A 2.5 V feed-forward second-order delta-sigma modulator for audio application is presented. A 9-level quantizer with a tree-structured dynamic element matching (DEM) was employed to improve the linearity by shaping the distortion resulted from the capacitor mismatch of the feedback digital-to-analog converter (DAC). A chopper stabilization technique (CHS) is used to reduce the flicker noise in the first integrator. The prototype delta-sigma analog-to-digital converter (ADC) implemented in a 65 nm 1P8M CMOS process occupies 0.747 mm^2 and achieves 109.1 dB dynamic range (DR), 85.4 dB signal-to-noise ratio (SNR) in a 24 kHz audio signal bandwidth, while consuming 14.75 mW from a 2.5 V supply.**

Index Terms—**Delta-sigma modulator, feed-forward, dynamic element matching, chopper stabilization**

I. INTRODUCTION

Recent advances of CMOS technology have enabled the high quality signal processing in the multi-media and communication systems and have resulted in a great demand for the high resolution analog-to-digital converters (ADCs). Among various ADC architectures, the delta-sigma ADC offers high dynamic range by using oversampling and noise shaping properties. Moreover, as it requires only simple and relatively high-tolerance analog components with fast and complex digital signal processing to achieve high resolution, it is very well-suited for the digital CMOS process.

The theoretical signal-to-quantization noise ratio (SQNR) of the delta-sigma ADC is given by Eq. (1)

$$SQNR_{MAX} = 6.02N + (20L+10)\log_{10} OSR - 10\log_{10}\left(\frac{\pi^{2L}}{2L+1}\right) \quad (1)$$

where, N is the number of quantizer bit resolution, L is the modulator order, and OSR is the oversampling ratio [1]. However, since this equation is based on many assumptions, the actual achievable maximum SQNR from the behavioral simulation with all possible non-idealities is much lower than the theoretical maximum SQNR. Even more, though the maximum SQNR satisfies the target specification, the overall performance is typically limited by the circuit noise such as the kT/C noise and the op-amp noise. Therefore, the careful consideration of the noise budget is necessary for the optimum design. The kT/C noise is easily controlled by sizing the capacitors in the integrators and the OSR of the modulator at the expense of area and power. The sampling capacitor size and OSR need to be increased to reduce the kT/C noise in the delta-sigma modulator. The op-amp has two major noise sources, thermal noise and flicker noise. Among these, the flicker noise is dominant at low frequency and critical in a low-pass delta-sigma modulator. To achieve the high dynamic range, the flicker noise must be suppressed. The flicker noise of the op-amps can be attenuated by simply increasing the device size. However, the overall cost of the ADC will be increased due to its larger size. There are several techniques to reduce the flicker noise such as correlated double sampling and chopper stabilization techniques [2]. Even though theses techniques require additional switches and/or capacitors, overall size of the ADC can be reduced.

In this paper, a feed-forward single-loop second-order delta-sigma modulator is presented. A 9-level quantizer

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is employed with the dynamic element matching technique for the feedback DAC to improve the signal-to-noise ratio (SNR) and the linearity of the modulator. The rest of this paper is organized as follows. Section II describes the proposed delta-sigma modulator architecture. The circuit level design details of the modulator are discussed in Section III. In Section IV, measurement results are presented. The overall conclusion is drawn in Section V.

II. PROPOSED ARCHITECTURE

As discussed in Section I, there are three main variables which decide the theoretical SQNR, N, L, and OSR. For the targeted performance of 100 dB dynamic range (17 ENOBs), a second-order modulator with 9-level quantizer and OSR of 512 is selected as shown in Fig. 1. A single-loop second-order modulator is employed, as it relaxes the gain requirement of the op-amps in the integrators and allows the stable operation than the higher order modulators. An internal 9-level quantizer increases the stable input signal range and the modulator stability as well as reduces the quantization noise. However, the multi-bit quantization introduces the non-linearity due to the mismatch of the DAC capacitors which limits the overall modulator performance. To relax the matching requirement of the DAC capacitors and improve the linearity, a tree-structured dynamic element matching (DEM) which spectrally shape the distortion arising from the analog components mismatches of the DAC is used as illustrated in Fig. 2 [3]. A 25 MHz clock is used for the signal bandwidth of 24 kHz with OSR of 512. With the selected high OSR, the design requirements of the anti-aliasing filter (AAF) as well as the thermal noise of the analog circuits and the sampling capacitors in the integrators are relaxed.

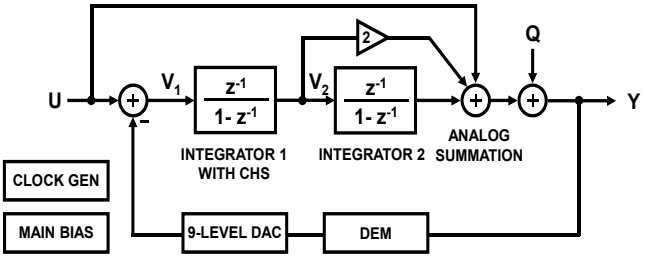


Fig. 1. The linear model of the proposed delta-sigma modulator.

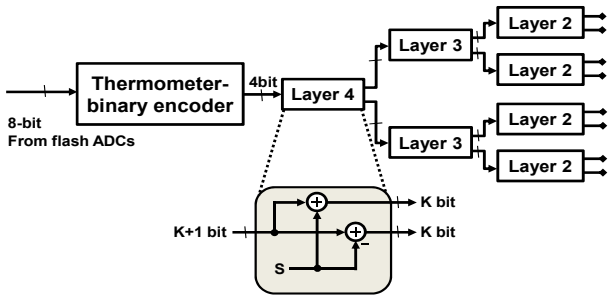


Fig. 2. Block diagram of the tree-structred DEM.

The z-domain output, Y(z), of the proposed delta-sigma modulator is derived as Eq. (2)

$$Y(z) = U(z) + \left(1 - z^{-1}\right)^2 Q(z) \tag{2}$$

where, U(z) is the input signal of the modulator, Q(z) is the quantization noise. In this feed-forward topology, each input of the integrators, $V_1(z)$ and $V_2(z)$, is

$$V_1(z) = -\left(1 - z^{-1}\right)^2 Q(z) \tag{3}$$

$$V_2(z) = -z^{-1}\left(1 - z^{-1}\right) Q(z) \tag{4}$$

As shown in Eqs. (3, 4), each integrator processes only the shaped quantization noise which is independent to the input signal, so it relaxes the signal swing range and the linearity requirements of the op-amps in the integrators [4]. Fig. 3 shows the behavioral model simulation result of the proposed modulator with op-amp DC gain variation. A key observation in this result is that an op-amp DC gain above 50 dB suffices to the design aim. This is due to the input feed-forward single-loop topology of the modulator. Fig. 4 shows the simulation result with the various capacitor mismatches. This result indicates that less than 0.05% DAC capacitor mismatch is enough to satisfy the design target which is available in the modern CMOS technology.

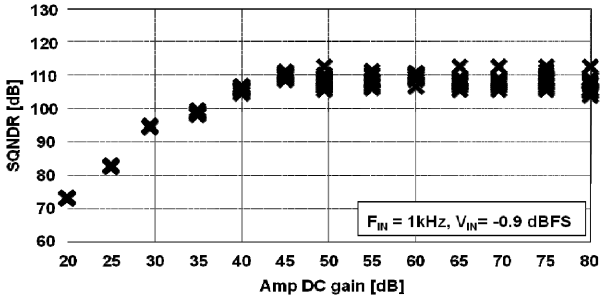


Fig. 3. SQNDR dependence on op-amp DC gain of the integrators.

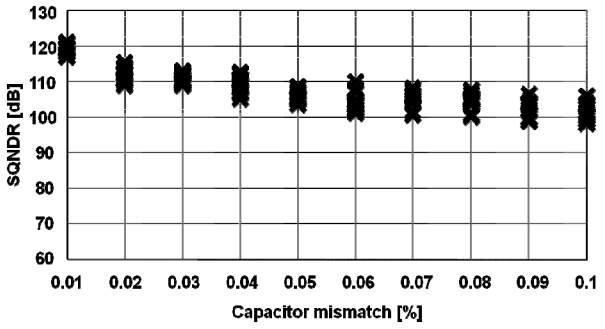


Fig. 4. SQNDR dependence on capacitor mismatch.

III. CIRCUIT IMPLEMENTATION

The switched-capacitor (SC) implementation of the proposed delta-sigma modulator and its timing diagram are shown in Fig. 5. It consists of two SC integrators and a summing amplifier followed by a 9-level flash ADC. The operation of the first integrator is as follows. During the ϕ_1 phase, the input signal is sampled at the sampling capacitor C_{S1X}. Then, during the following ϕ_2 phase, reference signal ($\pm V_{REF}$) is subtracted from the sampled input by the output of the quantizer and the residual signal is integrated into the feedback capacitor C_{F1}. The second integrator only processes the output signal of the first integrator with same clock phases as first integrator; therefore, it is simply implemented with conventional SC integrator topology without DAC function. The SC summing amplifier is used to add signals from the input of the modulator and outputs of both integrators. During ϕ_1 phase, all the inputs of the summing amplifier are connected to the V_{CMO} to reset the sampling capacitors. And during the following ϕ_2 phase, each input signal is connected to the sampling capacitors. At this phase, the sum of the three input signals is transferred to the quantizer with no delay.

To achieve the high performance delta-sigma modulator, the noise analysis of the various noise sources has to be fulfilled. Each noise source must be optimized to achieve a target performance efficiently.

In the audio applications, the flicker noise of the first integrator limits the achievable performance of the modulator because they are referred directly to the input signal and have the same signal transfer function (STF) as input. To suppress the flicker noise in the low frequency, the chopper stabilization (CHS) technique is employed in the first integrator [5]. The input signal of the amplifier is chopped with ϕ_A and ϕ_B which is half of the sampling frequency, $F_S/2$. With this modulation, the flicker noise moves to the high frequency centered at $F_S/2$ and filtered out, therefore, the SNR of the modulator in signal bandwidth is improved.

The thermal noise of the amplifier of the first integrator also has to be optimized. The input referred noise of the first integrator resulted from the op-amp thermal noise is derived as

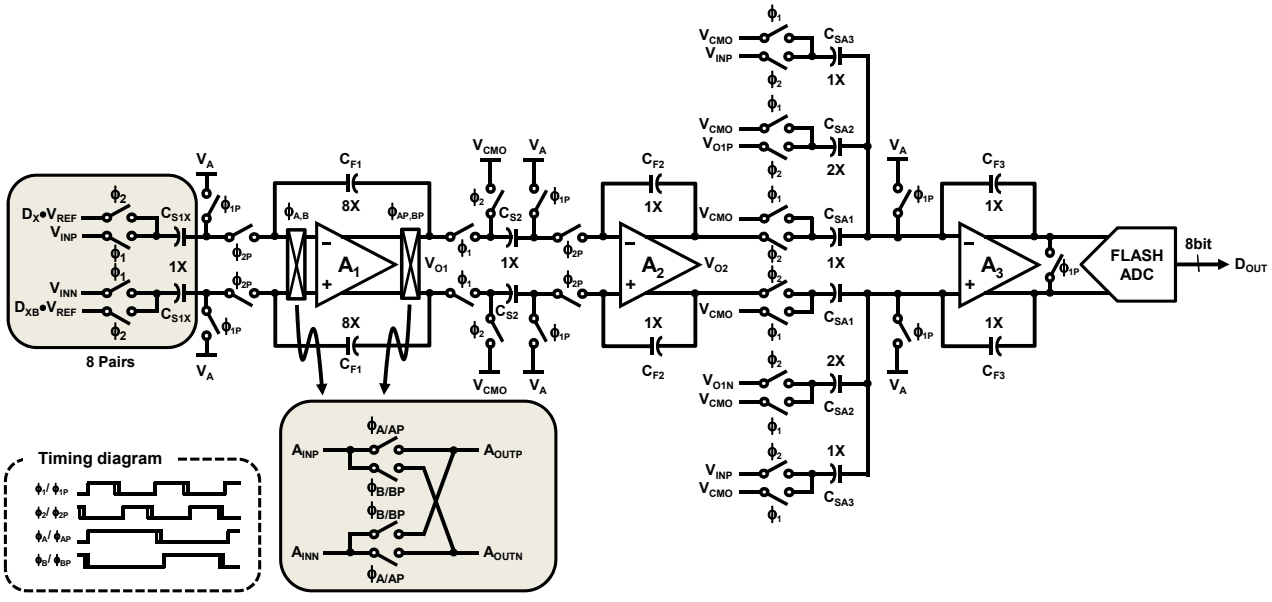


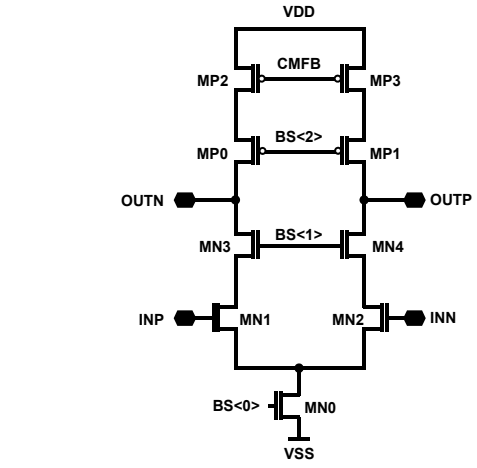
Fig. 5. The SC implementation of the proposed modulator.

$$V_{N,IN}(z) = V_{N1}(z) \cdot \frac{\sum_{X=1}^{8} C_{S1X} + \left(1 - z^{-1}\right) C_{F1}}{\sum_{X=1}^{8} C_{S1X}} \quad (5)$$

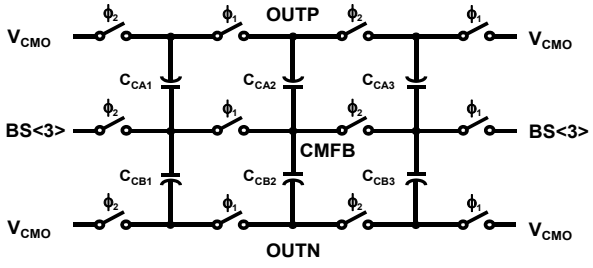
where, V_{N1} is the input referred op-amp noise of the first integrator, C_{S1X} is the sampling capacitance of the first integrator, and C_{F1} is the feedback capacitance of the first integrator. The op-amp noise V_{N1} is decided by the circuit implementation, and the input referred noise of the first integrator for a given V_{N1} is determined by the ratio of the C_{F1} to the C_{S1_TOT} as shown in Eq. (5). Due to the advantages of the conventional low-distortion input feed-forward architecture and the multi-bit quantizer, it is possible to set the gain of the first integrator to one resulting in the same value of the sampling capacitance as the feedback capacitance. It reduces the gain of noise from op-amp input to integrator input compared to the integrator which has gain of less than one. The kT/C noise is in inverse proportion to the input sampling capacitance. To achieve 16 bits resolution with the OSR of 512, 4 pF capacitors are used for the sampling and the feedback in the first integrator. In the second integrator and the summing amp, 100 fF capacitors are used for the sampling by considering the noise shaping of each kT/C noise and matching requirement.

The conventional telescopic op-amps shown in Fig. 6(a) are employed in the both integrators and the summing amplifier. Because the both integrators only process shaped quantization noise, the output swing range and the linearity requirements of the op-amps are significantly relaxed. The DC gains of the op-amps in both integrators are above 56 dB at the worst case corner which is above 6 dB compared to the minimum requirement from the behavioral simulation results. The switched capacitor (SC) type common-mode feedback (CMFB) circuit shown in Fig. 6(b) is used to stabilize the op-amp differential output common-mode level. By applying alternative SC-CMFB, it maitains the same total loading capacitance at the differential output during both clock phases [6]. The power consumption of the amplifier is scaled by considering the settling time and the linearity requirements of each stage.

A 9-level flash ADC with 8 comparators is used for the quantization. Each comparator consists of the pre-amplifier and latched comparator as shown in Fig. 7. The pre-amplifier amplifies the signal difference of the input



(a)



(b)

Fig. 6. A schematic of (a) Telescopic op-amp, (b) SC common-mode feedback.

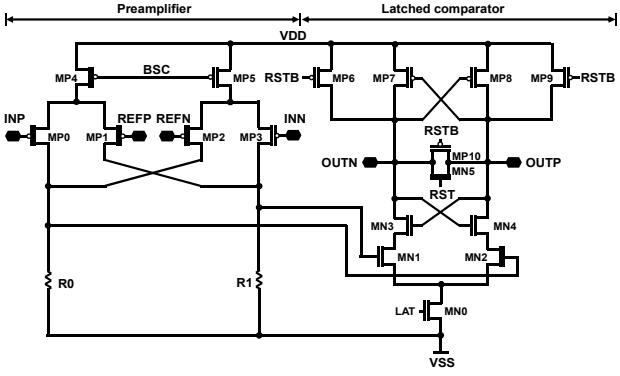


Fig. 7. A schematic of comparator.

pairs and adjusts the output common-mode level for the latched comparator by the bias current from MP4 and MP5 with the load resistors R0 and R1.

IV. EXPERIMENTAL RESULTS

The prototype chip is designed and fabricated in a 65 nm 1P8M CMOS process, and occupies 0.747 mm^2 (830 μm × 900 μm) active die area. The photograph of the

prototype chip is shown in Fig. 8. The measured power spectrum of the prototype ADC output is shown in Fig. 9(a). The measured signal-to-noise ratio (SNR) for 15 kHz, -6 dBFS sine wave input signal is 85.4 dB. The measured power spectrum with shorted input signal is shown in Fig. 9(b). It achieves a dynamic range of 109.1 dB. The total power consumption of the prototype ADC is 14.75 mW including digital blocks. The overall performance of the ADC is summarized in Table 1.

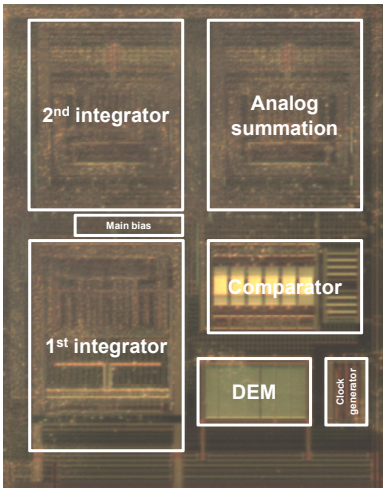
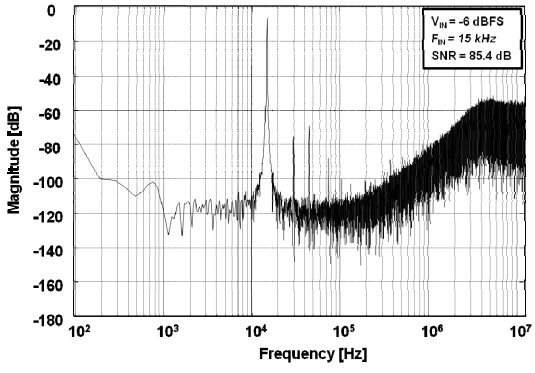
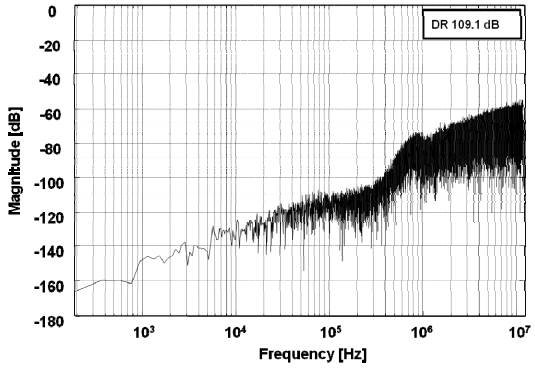


Fig. 8. Chip photograph.



(a)



(b)

Fig. 9. Measured output spectrum for: (a) 15 kHz, -6 dBFS sinusoidal input signal, (b) Shorted input signal.

Table 1. Measured Performance summary

Process	65 nm CMOS
Power supply	2.5 V
Signal bandwidth	24 kHz
Sampling frequency	25 MHz
OSR	512
Peak SNR Peak DR	85.4 dB 109.1 dB
Power Consumption	8.75 mW @ 2.5 V (Analog) 6 mW @ 2.5 (Digital)
Chip Area	0.747 mm^2 (830 μm x 900 μm)

V. Conclusions

In this paper, a delta-sigma modulator for high performance audio application is proposed. A feed-forward single-loop second-order architecture with 9-level quantizer is employed to relax the op-amp requirements and reduce the quantization noise level. A DEM technique is used to spectrally shape the DAC noise arising from analog component mismatches. The flicker noise is suppressed with CHS technique in the signal bandwidth effectively. The measured results verify the operation of the proposed modulator.

Acknowledgments

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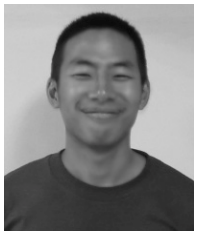

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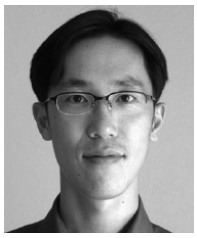

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