Rigorous Design of 22-nm Node 4-Terminal SOI FinFETs for Reliable Low Standby Power Operation with Semi-empirical Parameters

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Abstract—In this work, reliable methodology for device design is presented. Based on this method, the underlap length has been optimized for minimizing the gate-induced drain leakage (GIDL) in a 22-nm node 4-terminal (4-T) silicon-on-insulator (SOI) fin-shaped field effect transistor (FinFET) by TCAD simulation. In order to examine the effects of underlap length on GIDL more realistically, doping profile of the source and drain (S/D) junctions, carrier lifetimes, and the parameters for a band-to-band tunneling (BTBT) model have been experimentally extracted from the devices of 90-nm channel length as well as pn-junction test element groups (TEGs). It was confirmed that the underlap length should be near 15 nm to suppress GIDL effectively for reliable low standby power (LSTP) operation.

Index Terms—Device design, gate-induced drain leakage (GIDL), fin-shaped field-effect transistor (FinFET), TCAD simulation, carrier lifetime, band-to-band tunneling (BTBT), underlap length

I. INTRODUCTION

Recently, managing the standby power is considered as one of the most critical reliability issues in CMOS technologies including SRAM and high-density mobile electronic appliance. One of the major leakage current sources in ultra-small metal-oxide-semiconductor field-effect transistors (MOSFETs) is the gate-induced drain leakage (GIDL) current mainly caused by band-to-band tunneling (BTBT) near the drain end [1]. The devices on silicon-on-insulator (SOI) are known to have low intra-junction leakage and punch-through leakage [2, 3]. In a device structure view, fin-shaped FET (FinFET) have merits of better controllability on threshold voltage (V_{th}) and higher drivability of on-current [4, 5]. In this work, a rigorous design of 22-nm node 4-terminal (4-T) SOI FinFET aiming low standby power (LSTP) operation is carried out for suppressing GIDL by controlling the gate underlap length by TCAD simulation [6]. We used the parameters extracted from the fabricated devices of 90-nm technology node and junction-engineered pn-diode. This semi-empirical approach makes the design of the ultra-small CMOS devices more realistic and reliable.

II. DEVICE STRUCTURE AND DESIGN STRATEGY

The schematic views with circuit symbols for 3-T and 4-T SOI FinFETs and a cross-sectional image by scanning electron microscope (SEM) are shown in Fig. 1(a), (b) and (c).
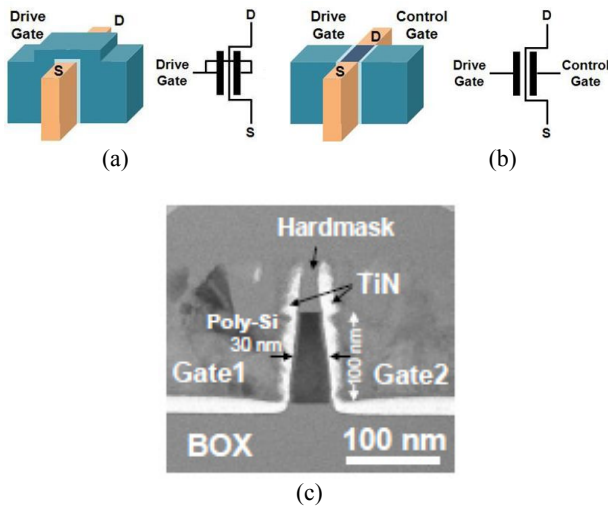
(a)　　　　　　　　　　　　　　　(b)

(c)

Fig. 1. Schematic views with circuit symbols for (a) 3-T and (b) 4-T SOI FinFETs, (c) Cross-sectional SEM image of the fabricated 4-T SOI FinFET following the 90-nm technology node [7].

Fig. 2 demonstrates the flow chart for the design of SOI FinFET on 22-nm technology node. As shown in the figure, three different initial approaches were made simultaneously toward the design purpose in order to collect the crucial ingredients that will be embedded in the device design by TCAD simulation.
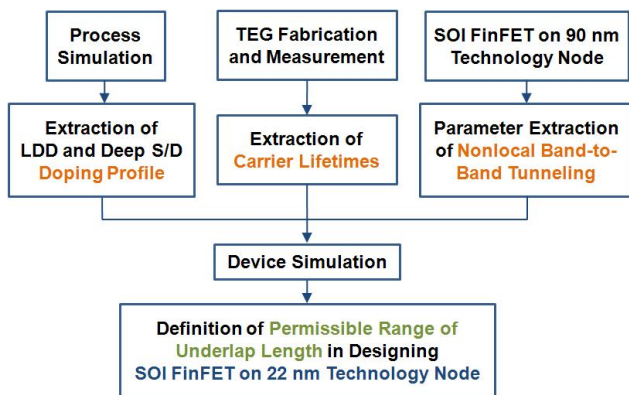

Fig. 2. Flow chart for the design of LSTP 4-T SOI FinFET on 22-nm node.

III. MEASUREMENT AND COMPACT MODELING

1. Doping Profile Extraction from Process Simulation

In order to identify the doping profile near the drain end of the fabricated device, process simulations were performed by fully following the process steps taken in

the fabrication [7]. As$^+$ ions of 5×10^{13} /cm^2 dose were implanted at 5 keV with 60° tilt for the source/drain (S/D) extensions. After the formation of sidewall spacer made of plasma oxide, P$^+$ ions of 1×10^{15} /cm^2 dose were implanted at 10 keV with 7° tilt for deep S/D implantation. The activation was performed by spike rapid thermal annealing (RTA) for 4 sec at 830 °C. In the fabrication, low thermal budget was pursued in the RTA process to minimize the unwanted movements of boron atoms in consideration of the applications for static random access memory (SRAM) architectures where p-type MOSFET should be implemented simultaneously [7-10]. Fig. 3 shows that the distances from the n$^+$ doping peaks of the extensions and deep S/D regions to the metallurgical junctions are 17 nm and 50 nm, respectively, by the process simulations. In this figure, the nominal distances are only meaningful since two curves reflect the results from two times of independent ion implantations on different Si wafers so that the relative locations are meaningless. Thus, these doping gradients of the LDD and S/D regions will be used in the design works regardless of the thicknesses of sidewall spacers, i.e, the underlap lengths.
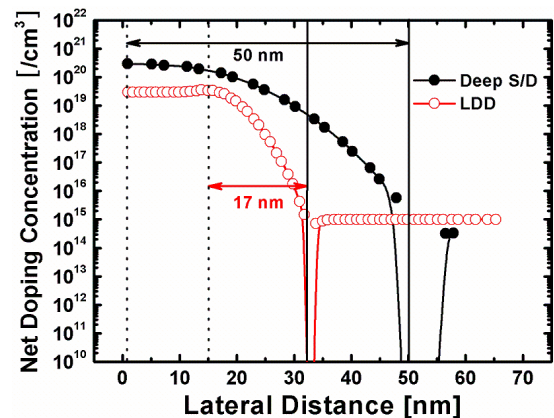
Fig. 3. Doping profiles near the junctions at the extension and deep S/D ends. The dotted lines and solid lines indicate n$^+$ peak doping locations and the metallurgical junctions, respectively.

2. Extraction of Carrier Lifetimes from Calibration Devices

For extracting more accurate carrier lifetimes, a test element group (TEG) containing pn-junctions of various dimensions was fabricated on the 6" SOI wafer following the actual process conditions for S/D junctions. A 6" p-type (100) SOI wafer with body doping concentration of

5×10^{15} /cm³ was prepared. The thickness of SOI is 1000 Å, which is the height of silicon fin, and the active region is isolated in a mesa structure by dry etch. A TEOS dummy pattern of 1000 Å thickness is constructed for distinguishing p- and n-type regions and the S/D extension is implanted by the previous condition, As⁺ 5×10^{13} /cm² dose at 5 keV with a changed tilting angle of 30°. In other words, the polysilicon gate and gate oxide in an SOI FinFET were simply replaced by TEOS hard mask in a pn-junction. The incident angle is switched from 60° to 30° to obtain the same doping profile in a pn-junction where the current flows along the wafer surface. The simple rotational conversion is demonstrated in Fig. 4. Sidewall spacers are formed by consecutive deposition and anisotropic dry etch of Si_3N_4 after the S/D extensions are formed. Likewise, S/D ion implantation is performed at a converted tilt of 83°. All the doses and acceleration energy conditions are same with those adopted in the fabrication of 4-T SOI FinFET. By this condition, extremely shallow S/D junctions on the Si fin sides are formed. After an activation by spike RTA, inter-layer dielectric (ILD) is deposited and contact holes are made, which are followed by metallization and alloy at 450 °C for 30 min in an N_2/H_2 ambient.

Fig. 5(a) and (b) show the fabricated pn-junction and the definition of the effective junction length (L_{eff}), respectively. The junction width was varied from 0.6 μm to 41.2 μm in the masks. On the other hand, L_{eff} is kept invariable since all the devices were fabricated by the same implantation and RTA conditions. Fig. 6 shows the junction capacitances measured by Agilent 4284A. The junction capacitances were measured from the capacitors with long junction widths and two capacitors are connected in parallel so that C_j is mainly composed of the surface component. Thus, the x-axis in Fig. 6 indicates
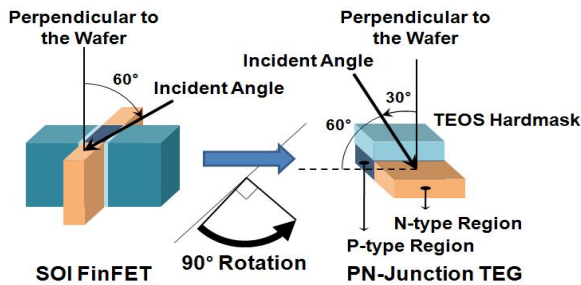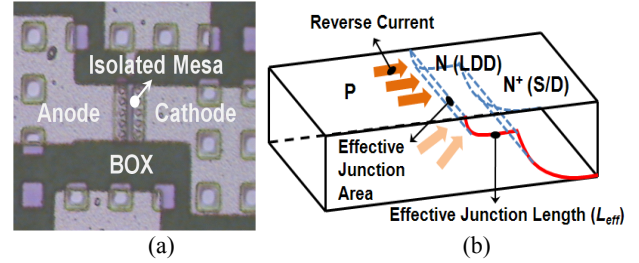

Fig. 5. Junction-engineered pn-diode in the TEG. (a) Microscopic view on top, (b) Schematic view of the mesa-structured pn-diode and effective junction area.
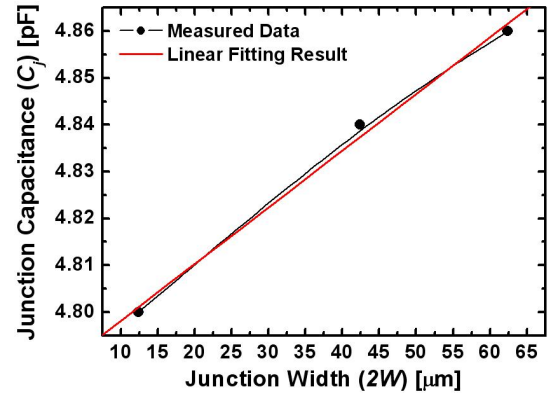

Fig. 6. Junction capacitance (C_j) as a function of junction width (2W).

the doubled junction width. Based on the slope of the fitting line, 1.21×10^{-11} F/cm, built-in potential values, and the depletion width at a reverse bias of 0.5 V, L_{eff} was extracted to be 6.4×10^{-4} cm. The carrier and generation lifetimes were calculated by following equations [11].

$$J_R = I_R / A_{eff} = I_R / WL_{eff} = q\sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A} + \frac{qn_iW_{dep}}{\tau_g} \quad (1)$$

$$\tau_g = \tau_p e^{(E_T - E_i)/kT} + \tau_n e^{-(E_T - E_i)/kT} \quad (2)$$

The effective junction area to calculate the reverse current density (J_R) is the multiplication of the junction width as a design variable and the extracted junction length. Since there are two unknowns in Eq. (1), τ_n and τ_g, J_R's under two reverse bias conditions at a fixed junction width were considered to set up two equations. Assuming the trap level is near the midgap ($E_T \sim E_i$) as the usual CMOS processes, τ_g is simply expressed as the sum of τ_p and τ_n from Eq. (2). The effective junction area in Eq. (1) is the multiplication of junction width as the design variable and the extracted effective junction length. The reverse currents were measured at reverse voltages of -

Fig. 4. Rotational conversion relation between tilt angles in ion implantations for the S/D regions of SOI FinFET and pn-junction.

0.2 V and -0.35 V by Agilent 4156C. Assuming $E_T \sim E_i$, the carrier lifetimes are calculated as $\tau_n = 5.430 \times 10^{-5}$ s and $\tau_p = 5.752 \times 10^{-6}$ s, which are reasonable values in the devices fabricated by conventional CMOS processes [12].

3. Modeling of Band-to-Band Tunneling

Fig. 7 shows the transfer characteristics curve from the measurement of a fabricated 4-T SOI FinFET under 3-T operation and its modeling results in which the newly extracted carrier lifetimes are reflected. Although there are a number of BTBT models [13-15], nonlocal BTBT calculations were carried out in consideration of quantum effects, which shows a very good agreement with the measured data as confirmed in the figure. For more elaborate fitting, the contact resistance and the electron mobility parameters were recursively figured out and equipped in the TCAD simulation. The channel length was 90 nm and the drive drain voltage (V_{DD}) was 1.0 V. Since GIDL is independent of device channel length [16, 17], the determined coefficients from the modeling results could be persistently utilized in designing the SOI FinFET device with 20-nm channel length.
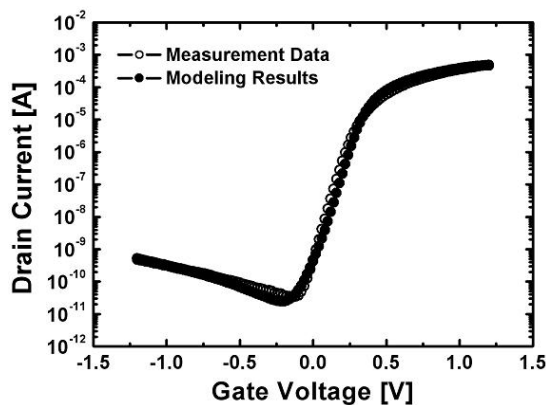

Fig. 7. I_D-V_{GS} curves from measurement data and modeling result.

IV. DESIGN OF LOW STANDBY POWER (LSTP) SOI FINFET

Based on the parameters extracted from the measurement and the compact modeling in the previous sections, a design of SOI FinFET device on 22-nm technology node for LSTP operation has been performed. The design variable was underlap length which substantially affects

the GIDL in the off-state of device. The underlap length can be easily modulated by the bottom width of the sidewall spacer [18-20]. For more reliable design, a number of realistic models were included in the simulation works: field and concentration-mobility models, Shockley-Read-Hall (SRH) recombination model, bandgap narrowing model, quantum model, gate current model, nonlocal BTBT model, and nonlocal trap-assisted tunneling (TAT) model [21-27].

Fig. 8(a) shows the simulation results of I_D-$V_{G,Drv}$ ($V_{G,Drv}$: drive gate voltage) curves of an SOI FinFET with a channel length of 20 nm. The drive and control gates (Fig. 1) are connected in common to investigate the transfer characteristics for the basic 3-T operation. The thicknesses of silicon fin and gate oxide were 10 nm and 1.4 nm, respectively. The underlap length was varied from 0 to 50 nm by 5 nm spacing. Fig. 8(b) depicts the V_{th} as a function of underlap length. They were extracted by a constant current method ($V_{th} = V_{G,Drv} @(I_D = 1$ $\mu A/\mu m))$. It was confirmed that the V_{th} values are in a
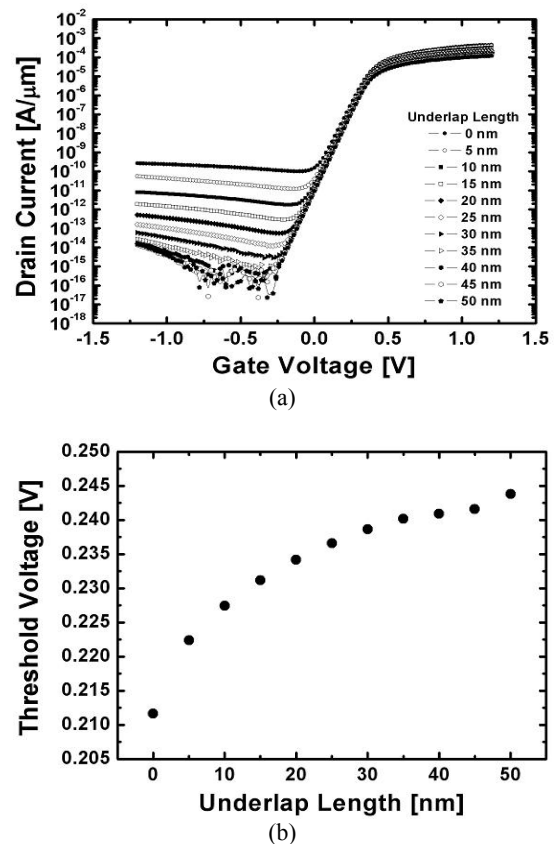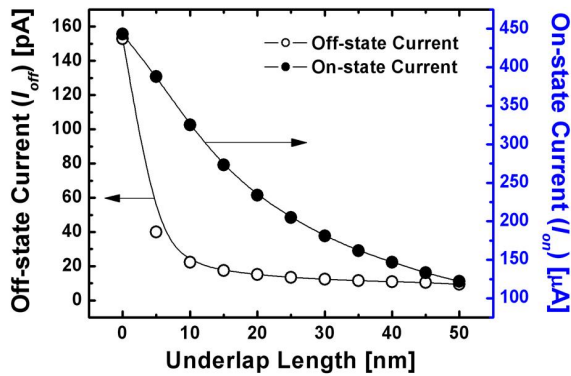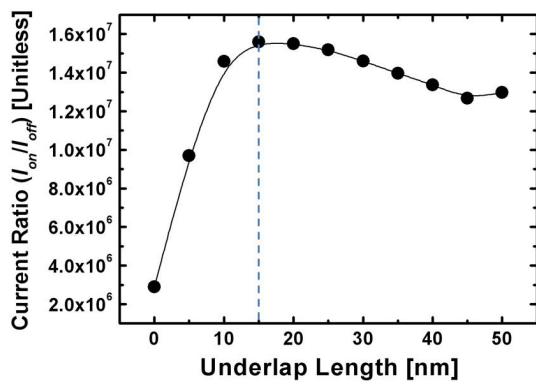

(a)

(b)

Fig. 8. Effects of the underlap lengths. (a) I_D-V_{GS} curves for the SOI FinFET devices, (b) corresponding threshold voltages (V_{GS} at a constant current of $I_D = 10^{-7}$ A/μm) with variation on the underlap lengths.

permissible range to meet the requirements on multiple-gate (MG) MOSFETs designated by the most recent technology roadmap [28]. In Fig. 8(a) and (b), V_{DD} was set to be 1.0 V in accordance with the near-term predictions for the LSTP technology by roadmap. Fig. 9(a) shows on-state (I_{on}) and off-state (I_{off}) currents with variation on underlap length. Both I_{on} and I_{off} decrease monotonically as the underlap elongates. Especially, I_{off} rolls off more prominently than I_{on} by controlling the underlap length. I_{off} is effectively suppressed below 20 pA/μm and saturated with an underlap longer than 10 nm.

Fig. 9(b) demonstrates the current ratio (I_{on} / I_{off}) as a function of underlap length. The current ratio increases drastically from non-underlap condition to underlap length of 15 nm due to the sharp decline in I_{off} up to this length. However, the ratio begins to roll off above the underlap length of 15 nm, where it is determined dominantly by continuous decrease of I_{on}. The drive current (I_D @(V_{GS} = V_{DD} = 1.0 V)) is monotonically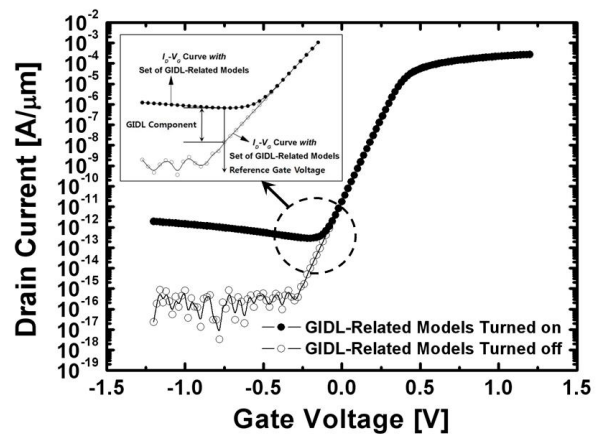 degraded with a large slope as the underlap elongates due to the incre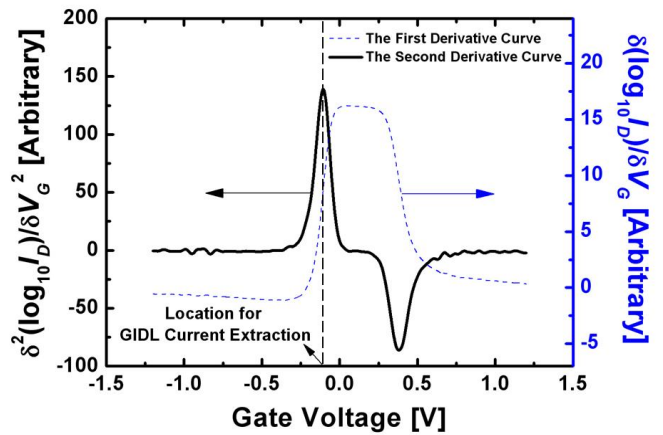ase of series resistance across the graded doping region. Assuming the S/D dopants are activated by RTA, the simulation results show that non-zero underlap is indispensable for suppressing the off-state leakage current below the reference value guided for reliable LSTP devices in the near future by the technology roadmap, 50 pA/μm [28]. If we consider the effects of the underlap length collectively, although the non-zero underlap is essential in order to minimize the leakage current, there should be an upper limit in designing the underlap length for operating by lower V_{DD} as well as reducing the device area. These are not the most important factors in LSTP design but should be working as the boundaries.

Fig. 10(a) and (b) demonstrates an analytical method of extracting GIDL. In this method, GIDL current is defined as the difference in drain current induced by

(a)

(b)

Fig. 9. Current characteristics as a function of underlap length. (a) I_{on} and I_{off} (I_{off} = I_D @(($V_{G,Drv}$, V_D) = (0 V, 1 V))), (b) On/off-current ratio (I_{on}/I_{off}). A local maximum is observed at an underlap length of 15 nm.

(a)

(b)

Fig. 10. Quantitative extraction of GIDL component. (a) Definition of GIDL by TCAD simulations: the drain current difference by switching on and off the set of all the GIDL-related models, (b) Extracting V_G location.

switching the full set of GIDL-related models at a specific gate voltage as shown in Fig. 10(a). The code names of GIDL-related models activated in the TCAD simulation were srh (Shockley-Read-Hall model), bbt.std (standard BTBT model), trap.tunnel (TAT model), bbt.nonlocal (nonlocal BTBT model), bbt.nlderivs (a BTBT model considering the derivatives of the tunneling current with respect to the values of the band edges), bbt. forward (a BTBT model for more accurate calculation in forward tunneling current), bbt.reverse (same purpose for in reverse one), and tat.nonlocal (a TAT model enabling the nonlocal tunneling model in the calculation of the field effect enhancement factors). There is no feasible way to extract GIDL from the measured I_D-V_G curve in reality. However, in simulation works, GIDL can be quantitatively evaluated by switching on and off the set of GIDL-related models. In a previous research, only BTBT model was switched but it is more realistic to deal with all the related models simultaneously [29-31]. In Fig. 10(a), GIDL is defined as the current difference generated by switching the model set. Fig. 10(b) shows the positioning V_G value for GIDL extraction.

The switching operations were performed at a gate voltage where the second derivative of I_D-V_G curve has a local maximum. It can trace the point where the curvature most rapidly changes. At this point, drastic enhancement in GIDL begins to occur [31]. In a physical sense, this is more reliable than the conventional method [29]. Since it is almost impossible to extract GIDL solely from other current components by measurement from an already fabricated device, establishing a reliable method of quantitative extraction of GIDL based on device simulation will be useful. Fig. 11 depicts the extracted
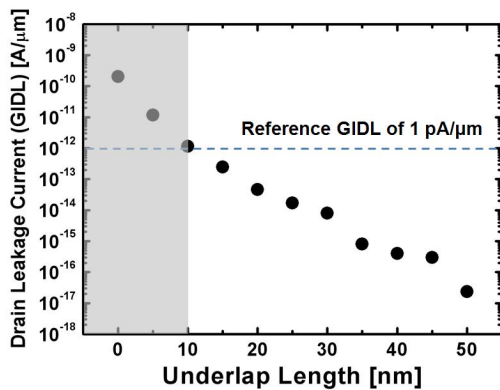

Fig. 11. GIDL current as a function of underlap length. The tentative reference line indicates GIDL of 1 pA/μm.
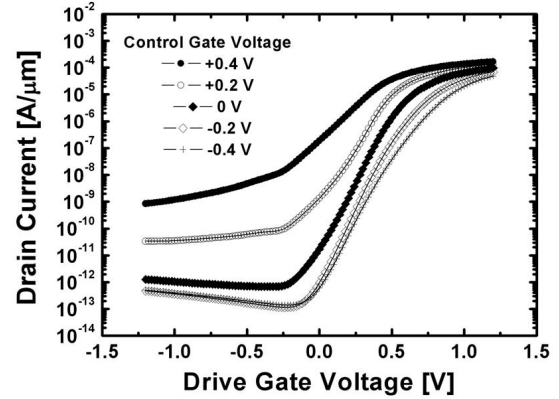

Fig. 12. I_D-$V_{G,Drv}$ curves for 4-T operations with $V_{G,Ctr}$ control ($V_{DD} = 1.0$ V).

GIDL components as a function of underlap length. If a permissible GIDL current is presumed to be 1 pA/μm, the underlap length should be longer than 10 nm. Thus, for the sake of stable V_{th} window, maximum I_{on}/I_{off} ratio, and effective repression of I_{off} in terms of GIDL, the underlap should be at least 15 nm but limited for efficiency in operation and area. Fig. 12 shows I_D-$V_{G,Drv}$ curves at different control gate voltages ($V_{G,Ctr}$). The designed channel length and underlap were 20 nm and 15 nm, respectively, as optimized. The results confirm the 4-T operation and threshold V_{GDrv} is adjustable by V_{GCtr}. In order to suppress I_{off} below a reference value by roadmap, 50 pA/μm, while keeping the subthreshold slope steep for the LSTP logic application, nonpositive $V_{G,Ctr}$ biasing is desirable.

V. CONCLUSIONS

In this work, a rigorous design of 4-T SOI FinFET device on 22-nm technology node for LSTP operation has been performed. For higher reliability, parameters were extracted and calculated semi-empirically from the fabricated 90-nm SOI FinFET and TEGs. The doping profiles obtained by the process simulations abiding by actual fabrication conditions, majority and minority carrier lifetimes, and recursive fitting, the accuracy of device design was made highly reliable. Based on these results, a 22-nm node 4-T SOI FinFET has been designed focusing on the underlap length for LSTP application by TCAD simulations. In order to achieve reliable LSTP operation with marginal performance and area-effectiveness, the underlap should be precisely controlled

around 15 nm in a process architecture using the RTA system.

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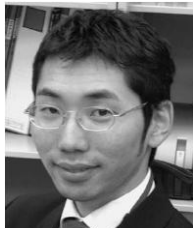
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