

# Improvement of Thermal Stability of Ni-Silicide Using Vacuum Annealing on Boron Cluster Implanted Ultra Shallow Source/Drain for Nano-Scale CMOSFETs

Hong-Sik Shin, Se-Kyung Oh, Min-Ho Kang, Ga-Won Lee, and Hi-Deok Lee

**Abstract**—In this paper, Ni silicide is formed on boron cluster ( $B_{18}H_{22}$ ) implanted source/drains for shallow junctions of nano-scale CMOSFETs and its thermal stability is improved, using vacuum annealing. Although Ni silicide on  $B_{18}H_{22}$  implanted Si substrate exhibited greater sheet resistance than on the  $BF_2$  implanted one, its thermal stability was greatly improved using vacuum annealing. Moreover, the boron depth profile, using vacuum post-silicidation annealing, showed a shallower junction than that using  $N_2$  annealing.

**Index Terms**—Boron Cluster ( $B_{18}H_{22}$ ), shallow junction, Ni silicide, nano-scale CMOSFETs, vacuum annealing

## I. INTRODUCTION

For more than 20 years, metal–oxide–semiconductor field-effect transistors (MOSFETs) have been scaled down to improve device performance and to increase integration density. However, when the gate length of the device is scaled down to 22 nm or less, fundamentally, new junction technologies are required to suppress the short channel effect (SCE) by producing ultra shallow junctions with super abrupt doping profiles, above equilibrium dopant activation and contact resistivity [1, 2]. Novel silicide technology is also required to form a uniform and stable silicide on the ultra shallow junction. Recently, boron cluster ( $B_{18}H_{22}$ ) implantation was proposed to form the ultra shallow junction. It can reduce boron channeling, due to its 20 times higher mass,

relative to boron [3]. Simultaneously, low energy boron implantation exhibits low throughput due to low beam current [4]. Moreover, boron cluster implantation could reduce the boron penetration that  $BF_2$  implantation may induce due to the fluorine [5]. It can also reduce the fluctuation of MOSFET parameters, compared with boron implantation [6, 7]. This approach offers various advantages, such as high throughput, low beam divergence, and high dose implantation. However, conventional  $B_{11}$ ,  $BF_2$ , and boron cluster ion implantations show transient enhanced diffusion during the rapid thermal annealing process, which increases the junction depth [8].

Although cobalt silicide ( $CoSi_2$ ), from 0.35  $\mu m$  CMOS technology, has been used widely, it is no longer suitable for nano-scale MOSFETs with a gate length less than 50 nm because its main shortcoming is high silicon consumption, which is detrimental to ultra shallow junctions. At present, it is believed that Ni silicide (NiSi) will replace current  $CoSi_2$  for nano scale MOSFETs because Ni silicide has several advantages over  $CoSi_2$ . However, poor thermal stability is a main obstacle in the nano scale CMOSFET. Therefore, forming a NiSi film, with a uniform orientation in ultra shallow junctions, is still a big challenge [6, 9].

In this paper, we discuss the application of vacuum annealing to boron cluster implanted samples and the thermal stability of the Ni silicide source/drain junction is analyzed in depth.

## II. EXPERIMENTAL DETAILS

The process flow for the experiments is summarized in Fig. 1. An ultra shallow junction was formed by a boron cluster ( $B_{18}H_{22}$ ) ion implantation (Energy: 20 keV / Dose:  $3 \times 10^{15} \text{ cm}^{-2}$ ). A  $BF_2$  (5 keV /  $3 \times 10^{15} \text{ cm}^{-2}$ ) implanted junction was also prepared for comparison. After removing the native oxide in diluted hydrofluoric acid (1 : 100), a 15 nm thick pure Ni layer was deposited, using a radio frequency magnetron sputter system, followed by an in situ deposition of a 10 nm-thick titanium nitride (TiN) layer. The TiN capping layer is commonly used to prevent oxygen contamination during silicide formation. After the formation of Ni silicide, using a one-step rapid thermal process (RTP) at various temperatures from 400 ~ 700 °C for 30 sec, the unreacted metal and TiN layers were selectively removed using a sulfuric acid solution ( $H_2SO_4 : H_2O_2 = 4 : 1$ ). Finally, high temperature furnace annealing (post-silicidation annealing) was carried out at 550 ~ 650 °C for 30 min in  $N_2$  (99.99%) or vacuum ( $3 \times 10^{-2}$  Torr) ambient annealing to check the thermal stability of the formed Ni-silicide.

Sheet resistance was measured by the four-point probing method. Cross-sectional field emission scanning electron microscopy (FE-SEM), field emission transmission electron microscopy (FE-TEM), and scanning probe microscopy (SPM) were employed to study the interfacial structure and surface micrograph of the Ni silicide and annealed films. The phase of Ni silicide was investigated using X-ray diffraction (XRD). A secondary ion mass spectrometer (SIMS) was used to verify the depth profiles of boron and nickel elements.

## III. MEASUREMENT RESULTS

Fig. 2(a) and (b) show the sheet resistance of NiSi as a

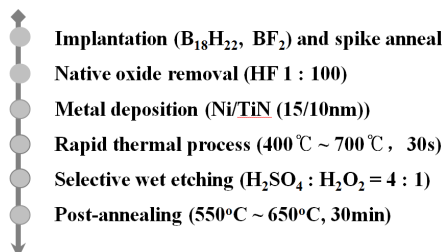


Fig. 1. Process flow for the experiments.

function of RTP and annealing temperatures, respectively.

It can be seen, in Fig. 2(a), that sheet resistance drops sharply at 400 °C indicating the formation of NiSi at this temperature. Fig. 2(a) also exhibits a stable RTP window at 400 °C ~ 650 °C, and an increase of sheet resistance at 700 °C. NiSi on  $BF_2$  exhibits lower sheet resistance than that on  $B_{18}H_{22}$ . However, the sheet resistance of  $BF_2$  begins to increase by with post-silicidation annealing from 650 °C, for both  $N_2$  and vacuum annealing as shown in Fig. 2(b). The purpose of post-silicidation annealing is to check the thermal immunity of the NiSi formed using RTP. Although NiSi on  $B_{18}H_{22}$  also exhibits a great increase of sheet resistance with by post-silicidation,  $N_2$  annealing at 650 °C, vacuum annealing does not exhibit an increase of sheet resistance at all. It was reported that fluorine could enhance the boron diffusion in oxides, causing fluctuations in threshold-voltage ( $V_T$ ) and an increase of off leakage current [10]. On the contrary, the boron cluster implantation could

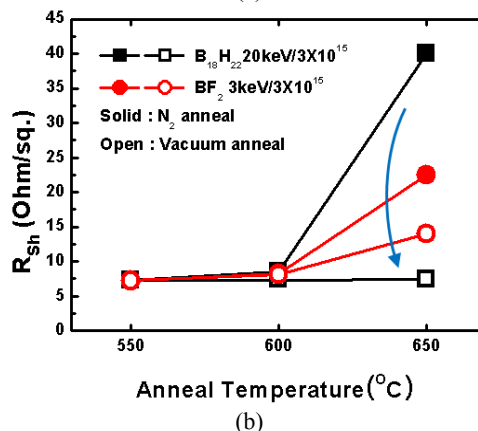
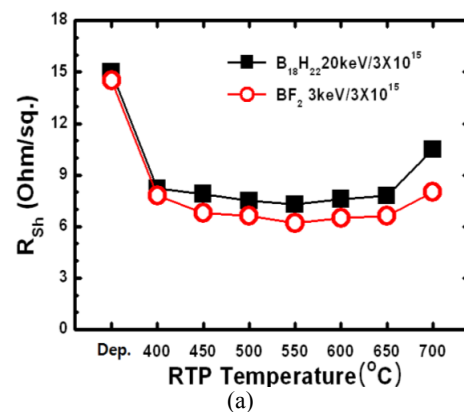
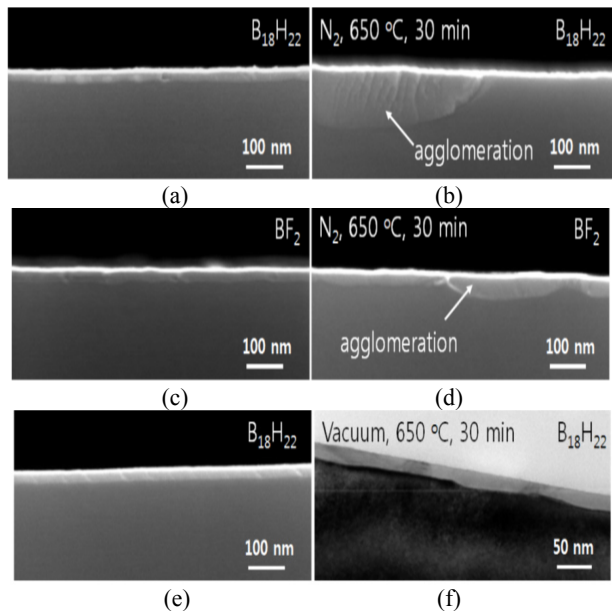
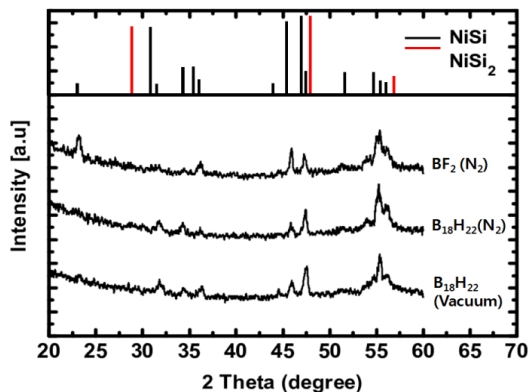


Fig. 2. Sheet resistance of Ni silicide as a function of (a) RTP, and (b) post-silicidation temperature of  $N_2$  and vacuum annealing on  $BF_2$ , and  $B_{18}H_{22}$  implanted substrate. RTP temperature for the formation of NiSi is 600 °C for post-silicidation experiment.

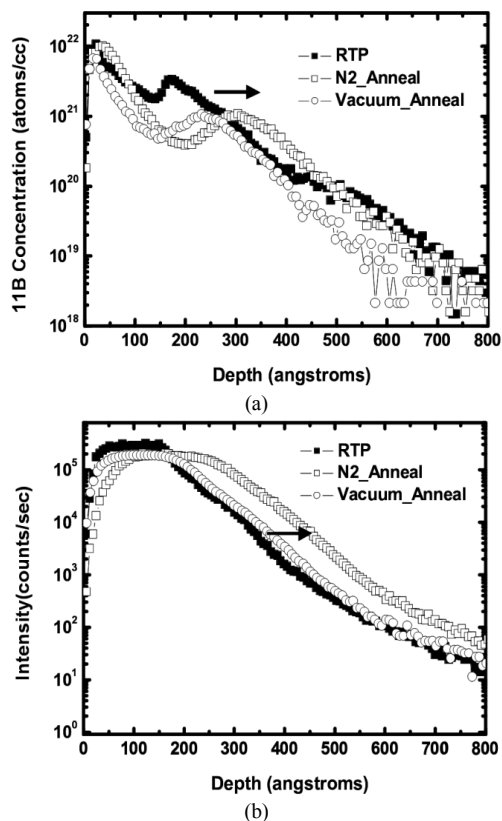


**Fig. 3.** Cross-sectional FE-SEM and FE-TEM image of Ni-silicide on  $\text{BF}_2$  and  $\text{B}_{18}\text{H}_{22}$  implanted Si substrates. (a)  $\text{B}_{18}\text{H}_{22}$  after RTP, (b)  $\text{B}_{18}\text{H}_{22}$  -  $\text{N}_2$  Annealing, (c)  $\text{BF}_2$  after RTP, (d)  $\text{BF}_2$  -  $\text{N}_2$  Annealing, and (e, f)  $\text{B}_{18}\text{H}_{22}$  - Vacuum Annealing.

reduce the boron penetration because there is no fluorine component in it [5]. Fig. 3 shows cross-sectional FE-SEM and FE-TEM images of Ni silicide on  $\text{BF}_2$  and  $\text{B}_{18}\text{H}_{22}$  implanted substrates. The FE-SEM images exhibit a uniform profile just after RTP (600 °C, 30 sec), as shown in Fig. 3(a) and (c); however, agglomeration appeared after  $\text{N}_2$  annealing (650 °C, 30 min) for both  $\text{BF}_2$  and  $\text{B}_{18}\text{H}_{22}$  implanted substrates (Fig. 3(b) and (d)). A uniform profile, however, was maintained after vacuum annealing (650 °C, 30 min), as shown in Fig. 3(e) and (f). The uniform NiSi layer leads to a lower sheet resistance at a low annealing temperature and NiSi agglomeration, as indicated in the figures, results in the abrupt increase of sheet resistance at high temperature. To analyze further the origin of the increase of the sheet resistance in of post-silicidation annealing at 650 °C, XRD phase analysis was performed, as shown in Fig. 4. It is quite notable that there is no  $\text{NiSi}_2$  peak, even after post silicidation annealing at 650 °C, for either  $\text{N}_2$  or vacuum annealing for  $\text{B}_{18}\text{H}_{22}$ , nor for  $\text{N}_2$  annealing for  $\text{BF}_2$ . Therefore, it can be concluded that the abrupt increase of sheet resistance is due to the agglomeration rather than to the formation of high resistive  $\text{NiSi}_2$ . Fig. 5 shows SIMS depth profiles of boron and Ni for the  $\text{B}_{18}\text{H}_{22}$  implanted substrate, after post-silicidation annealing using  $\text{N}_2$  and vacuum annealing. Although



**Fig. 4.** XRD phase analysis of Ni silicide on  $\text{BF}_2$  and  $\text{B}_{18}\text{H}_{22}$  implanted Si substrate after  $\text{N}_2$  and Vacuum post-silicidation annealing at 650 °C.



**Fig. 5.** Depth profile of (a) boron and (b) Ni on  $\text{B}_{18}\text{H}_{22}$  implanted wafer before and after post-silicidation  $\text{N}_2$  and vacuum annealing.

both annealing induces boron diffusion, boron diffusion becomes less in the vacuum annealing than in  $\text{N}_2$  annealing, as shown in Fig. 5(a).

However, the depth profile of Ni for vacuum annealing is similar to that without annealing (RTP); that is, there is no diffusion of Ni during post silicidation annealing. In the case of  $\text{N}_2$  annealing, Ni shows deeper

distribution than in the vacuum annealing case, which implies the agglomeration of NiSi, in agreement with Fig. 3(b).

#### IV. CONCLUSIONS

In this study, the thermal stability of Ni silicide on  $B_{18}H_{22}$  implanted junctions is improved using vacuum post-silicidation annealing. Low sheet resistance and little degradation of the cross-sectional profile, even after vacuum post-silicidation annealing at 650 °C for 30 min., are mainly attributed to the retardation of agglomeration and penetration of Ni silicide. Moreover, almost the same NiSi peaks appeared after  $N_2$ , and vacuum post-silicidation annealing on  $BF_2$  and  $B_{18}H_{22}$  implanted substrates. Boron and Ni diffusion, with vacuum annealing, is less than with  $N_2$  annealing, maybe due to the suppressed agglomeration and/or penetration of NiSi.

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#### REFERENCES

- [1] C.Y. Lu, J.M. Sung, "Reverse short-channel effects on threshold voltage in submicrometer silicide devices," *Electron Device Lett.*, IEEE Vol.10, p.446, 1989.
- [2] D.-X. Xu, S. R. Das, C. J. Peters, and L. E. Erickson, "Material aspects of nickel silicide for ULSI applications," *Thin Solid Films* 326, p.143, 1998.
- [3] X. Lu, L. Shao, X. Wang, J. Liu, W. Chu, J. Bennet, L. Larson, and P.Ling, "Cluster-ion implantation: An approach to fabricate ultrashallow junctions in silicon," *J. Vac. Sci. Technol. B* 20, 992, 2002.
- [4] Y. Kawasaki, T. Kuroi, T. Yamashita, K. Horita, T. Hayashi, M. Ishibashi, M. Togawa, Y. Ohno, M. Yoneda, T. Horsky, D. Jacobson, and W. Krull, "Ultra-shallow junction formation by  $B_{18}H_{22}$  ion implantation," *Nucl. Instrum. Methods Phys. Res. B* 237, 25, 2005.
- [5] M. Ishibashi, Y. Kawasaki, K. Horita, T. Kuroi, T. Yamashita, K. Shiga, T. Hayashi, and M. Togawa, "Advantages of  $B_{18}H_{22}$  Ion Implantation and Influence on PMOS Reliability," *International Workshop on Junction Technology'05*, p.31, 2005.
- [6] C. Lavoie, F. M. d'Heurle, C. Detavernier, and C. Cabral Jr., "Towards implementation of a nickel silicide process for CMOS technologies," *Microelectron. Eng.* 70, p.144, 2003.
- [7] W.J. Lee, S.Y. Oh, Y.J. Kim, Y.Y. Zhang, Z. Zhong, S.Y. Jung, H.H. Ji, K.J. Hwang, Y.C. Kim, H.T. Cho, W.A. Knull, J.S. Wang, and H.D. Lee, "Formation and Thermal Stability Characteristics of Ni Silicide on Boron Cluster ( $B_{18}H_{22}$ ) Implanted Source/Drain," *International Workshop on Junction Technology'06*, p.184, 2006.
- [8] A. Agarwal, H.-J. Gossmann, D. C. Jacobson, D. J. Eaglesham, M.Sosnowski, J. M. Poate, I. Yamada, J. Matsuo, and T. E. Haynes, "Transient enhanced diffusion from decaborane molecular ion implantation," *Appl.Phys. Lett.* 73, 2015, 1998.
- [9] H.I. Iwai, T.Ohguro, and S.I. Ohmi, "NiSi silicide technology for scaled CMOS," *Microelectron. Eng.*, Vol.60, p.157, 2000.
- [10] T. Aoyama, K. Suzuki, H. Tashiro, Y. Toda, T. Yamazaki, K. Takasaki, and T. Ito, "Effect of fluorine on boron diffusion in thin silicon dioxides and oxynitride," *J. Appl. Phys.* 77, p.417, 1995.



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