A Semi-analytical Model for Depletion-mode N-type Nanowire Field-effect Transistor (NWFET) with Top-gate Structure

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Abstract—**We propose a semi-analytical current conduction model for depletion-mode n-type nanowire field-effect transistors (NWFETs) with top-gate structure. The NWFET model is based on an equivalent circuit consisting of two back-to-back Schottky diodes for the metal-semiconductor (MS) contacts and the intrinsic top-gate NWFET. The intrinsic top-gate NWFET model is derived from the current conduction mechanisms due to bulk charges through the center neutral region as well as of accumulation charges through the surface accumulation region, based on the electrostatic method, and thus it includes all current conduction mechanisms of the NWFET operating at various top-gate bias conditions. Our previously developed Schottky diode model is used for the MS contacts. The newly developed model is integrated into ADS, in which the intrinsic part of the NWFET is developed by utilizing the Symbolically Defined Device (SDD) for an equation-based nonlinear model. The results simulated from the newly developed NWFET model reproduce considerably well the reported experimental results.**

Index Terms—**Nanowire field-effect transistor (NWFET), depletion-mode, accumulation charge, pinch-off, Schottky diode, equivalent circuit**

I. INTRODUCTION

Semiconducting nanowires have recently attracted considerable attention. The nanowire circuits defined by assembly of the nanowire devices such as the semiconducting nanowire field-effect transistor (NWFETs) have been demonstrated already by the bottom-up paradigm [1-5]. Especially, NWFETs among the nanowire devices have demonstrated promising field-effect transistor (FET) characteristics in top-gate [6-10], bottom-gate [9-13], and surround-gate [14] FET geometries. Most of NWFETS have operated in accumulation or depletion mode [6-11]. The NWFETs have generally a metal-semiconductor-metal (MSM) structure [1-14], and the metal-semiconductor (MS) contacts in the NWFET can classify with Schottky contact and ohmic contact [15]. The NWFETs mostly composed of two Schottky contacts connected back to back, in series with a semiconducting nanowire operating as the intrinsic NWFET [15, 16].

To design and simulate the nanowire circuits, a few compact models of depletion-mode NWFETs with bottom-gate structure have been reported so far [9, 15-18]. Recently, we have developed a depletion-mode NWFET model including the surface depletion effect and the accumulated charges [17]. However, because the NWFET have only a bottom-gate structure and the NWFET model has not considered the nonlinear characteristics for the MS Schottky contacts yet, a new NWFET model with top-gate structure, including the nonlinear contact model, is required.

In this paper, we will present a new compact model of a depletion-mode n-type NWFET with top-gate structure for efficient circuit simulation. The NWFET model will be based on an equivalent circuit consisting of two back-to-back Schottky diodes for the MS contacts and one depletion-mode NWFET for the intrinsic top-gate NWFET. The intrinsic top-gate NWFET model will be

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derived from the current conduction mechanisms due to bulk charges through the center neutral region as well as of accumulation charges through the surface accumulation region, based on the electrostatic method used in [17]. The Schottky diode model for the MS contacts will include the thermionic field emission (TFE) and the thermionic emission (TE) mechanisms for reverse bias and forward bias, respectively. To verify a validity of our model, the results simulated by our model will be compared with the experimental results of the NWFET.

II. MODEL FORMATION

Fig. 1(a) and Fig. 1(b) show a schematic cross-sectional view of a n-type NWFET channel with top-gate structure used in this work and a schematic cross-sectional view along the NWFET channel, respectively. It is assumed that the cross-section of the nanowire used in this work is a square shape rather than a circular or hexagonal one, because a complicated computing tool would be necessary to simulate the NWFET structures with a circular or hexagonal cross-section [17]. The nanowire is a semiconductor doped with n-type impurities. The metals for ohmic contacts of the drain and source are used, the metal of the top-gate contacts to modulate the nanowire channel are used and the metal of the bottom-gate contacts to control the depletion width of bottom-side in the naowire. Here, W_{nw}, L_{nw}, t_{nw}, N_d, and ε_{nw} are the width, the length, the thickness, the n-type doping concentration, and the dielectric permittivity of the nanowire, respectively, t_{iT} and t_{iB} are the thickness of the top-gate insulator and the bottom-gate insulator, and ε_i is the dielectric permittivity of the insulator. The source in the device is grounded, and the voltages, V_D, V_{TG}, and V_{BG}, are applied to the drain, the top-gate, and the bottom-gate, respectively.

1. Gate Insulator Capacitance

The dielectric capacitance of a top-gate NWFET is difficult to determine precisely because of the curved gate geometry and the dependence of the curvature on the oxide thickness, and the wire-to-plate capacitance model used for bottom-gate NWFETs may be not applicable. For bottom-gate NWFETs, the general

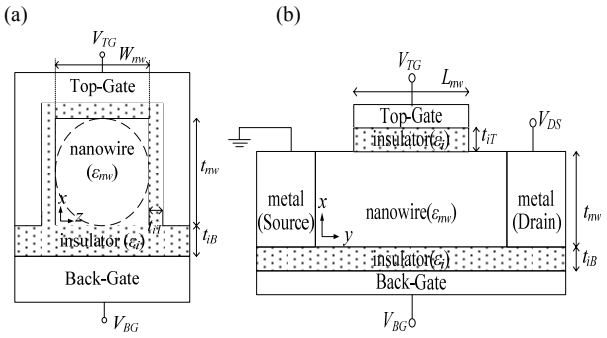

Fig. 1. (a) Schematic cross-sectional view along a NWFET channel with a top-gate structure and (b) schematic cross-sectional view of the NWFET channel.

form of capacitance per unit length can be represented as [17]

$$C_i' = \frac{C_i}{L_{nw}} = \frac{2\pi\varepsilon_i}{\ln\left[\dfrac{2t_{iT} + t_{nw}/2}{t_{nw}/2}\right]}, \quad (1)$$

where C_i is the gate insulator capacitance and t_{iT} is the thickness of a gate insulator. 2D device simulator was used to compute the capacitance between the top-gate and the NW, and it was found that the capacitance calculated by using (1) is underestimated by approximately 10~14 % when compared to the numerically computed capacitance for an oxide thickness of 100 nm [8]. Therefore, for the top-gate NWFET, the capacitance per unit length can be represented as $C'_{iT} = \alpha C'_i$ in this work, where α is a fitting parameter obtained from the 2D device simulator.

2. Mobile Carriers

Fig. 2(a) shows the cross-section in the substrate direction at a location y in the nanowire channel as the NWFET is biased at $V_{TG} - V(y) < V_{FBT}$, where $V(y)$ is the channel potential at location y in the channel and V_{FBT} is the flat-band voltage of top-gate. Solving the Poisson's equation in the vertical and lateral directions of the channel, the depletion widths of x-direction and z-direction due to the top-gate in the nanowire, x_{dT} and x_{dS}, are expressed as [18]

$$x_{dT}(y) = \frac{W_{nw}\varepsilon_{nw}}{C'_{iT}}\left\{-1+\sqrt{1-\frac{2C'^2_{iT}}{qN_d\varepsilon_{nw}W^2_{nw}}\left[V_{TG}-V_{FBT}-V(y)\right]}\right\}, \quad (2)$$

$$x_{dS}(y)=\frac{t_{nw}\varepsilon_{nw}}{C'_{iT}}\left\{-1+\sqrt{1-\frac{2C'^{2}_{iT}}{qN_d\varepsilon_{nw}t_{nw}^2}\left[V_{TG}-V_{FBT}-V(y)\right]}\right\}. \quad (3)$$

The depletion widths of x-direction due to the bottom-gate in the nanowire, x_{dB}, is expressed as

$$x_{dB}(y)=\frac{W_{nw}\varepsilon_{nw}}{C'_{iB}}\left\{-1+\sqrt{1-\frac{2C'^{2}_{iB}}{qN_d\varepsilon_{nw}W_{nw}^2}\left[V_{BG}-V_{FBB}-V(y)\right]}\right\}, \quad (4)$$

where C'_{iB} is the bottom-gate insulator capacitance per unit length and V_{FBB} is the flat-band voltage of bottom-gate. Under this condition, the conducting channel is in the center neutral portion (non-depleted region) of the nanowire, and the amount of the total mobile carriers per unit length in the center channel is given by

$$Q'_n=-qN_d(W_{nw}-2x_{dS})(t_{nw}-x_{dT}-x_{dB}). \quad (5)$$

As $V_{TG} - V(y) > V_{FBT}$, as shown in Fig. 2(b), the depletion region in the nanowire due to the top-gate disappears and electrons are accumulated at the nanowire surface below the top-gate. Under this situation, the amount of total mobile carriers per unit length in the channel, which includes the total electrons per unit length in the neutral region (Q'_n) and in the accumulated region (Q'_{acc}), are given by

$$\begin{aligned} Q'_n &= -qN_dW_{nw}\left(t_{nw}-x_{dB}\right), \\ Q'_{acc} &= -C'_{iT}\left[V_{TG}-V_{FBT}-V(y)\right]. \end{aligned} \quad (6)$$

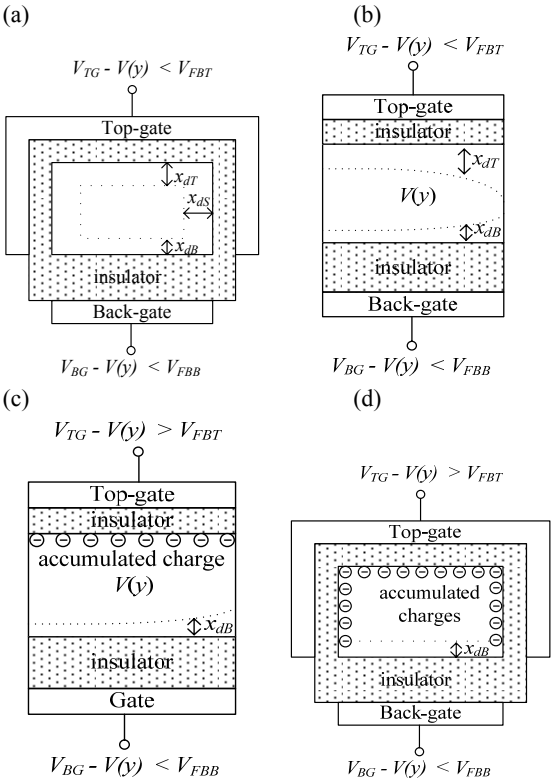

Fig. 2. (a) Cross-section of x-y plane and (b) cross-section of x-z plane in the NWFET channel when the top-gate side in the nanowire is depleted, and (c) cross-section of x-y plane and (d) cross-section of x-z plane in the NWFET channel when the top-gate surface in the nanowire is accumulated.

3. Mobility

The electron mobility for the mobile carriers in the neutral region and accumulation region of the nanowire are given by [17, 18]

$$\mu_n=\frac{\mu_{n0}}{1+\frac{\mu_{n0}}{v_{sat}}E}, \quad (7)$$

$$\begin{aligned} \mu_s &= \frac{\mu_{s0}}{1+\frac{\mu_{s0}}{v_{sat}}E}, \\ \mu_{s0} &= \frac{k_1\cdot\mu_{n0}}{1+\theta\left(V_{TG}-V_{FBT}\right)}, \end{aligned} \quad (8)$$

where μ_{no} is the low field bulk mobility, v_{sat} is the electron saturated velocity, E is the lateral electric field, and k_1 and θ are fitting parameters to account for the surface scattering effect.

4. Intrinsic Drain-Source Current

Depending on the top-gate bias-conditions, the mechanism of the current conduction in a depletion-mode NWFET can be complicated. The depletion-mode NWFET consists of two current components. One is the body current, I_{body}, occurring in the center neutral region of the device when the carriers in the nanowire are not fully depleted. The other is the accumulation current, I_{acc}, due to the accumulated electrons when the carriers at the nanowire surface below the top-gate are accumulated. Depending on the top-gate bias-conditions, there are six cases for the current conduction condition in the depletion-mode NWFET due to the top-gate as shown in Fig. 3. The left and right figures show the

cross-sections of the *x*-*y* plane and the *x*-*z* plane in the NWFET channel, respectively.

Case 1: It is the case when $V_{TG} < V_{TH}$, i.e., when the nanowire is fully depleted. The threshold voltage V_{TH} is defined as the gate voltage when the source end in the nanowire fully depleted, and it is given by $V_{TH} = V_{FBT} - V_{dep}$. Here V_{dep} is the change in the top-gate voltage with respect to top-gate flat-band necessary to obtain the threshold condition near the source. There are two cases of the threshold condition and the threshold voltage as follows

1. Fully-depleted condition 1 of the vertical direction at the source end in the nanowire: $t_{nw} = x_{dT}(0) + x_{dB}(0)$, and by applying the fully-depleted condition 1, V_{dep1} is given by

$$V_{dep1} = \frac{qN_d W_{nw}}{C_{iT}^{'}}\left[t_{nw} - x_{dB}(0)\right]\left\{1 + \frac{C_{iT}^{'}}{2\varepsilon_{nw} W_{nw}}\left[t_{nw} - x_{dB}(0)\right]\right\}. \quad (9)$$

2. Fully-depleted condition 2 of the lateral direction at the source end in the nanowire: $W_{nw} = 2x_{dS}(0)$, and by applying the fully-depleted condition 2, V_{dep2} is given by

$$V_{dep2} = \frac{qN_d t_{nw} W_{nw}}{2C_{iT}^{'}}\left(1 + \frac{C_{iT}^{'} W_{nw}}{4\varepsilon_{nw} t_{nw}}\right). \quad (10)$$

The effective V_{dep} is given by $V_{dep} = \min(V_{dep1}, V_{dep2})$. Here $\min(a,b)$ function returns the minimum value of a and b. In this case, the NWFET operates in the subthreshold region. Because diffusion current dominates in the subthreshold region, the drain current is given by [17, 18]

$$I_{DS} = \frac{W_{nw}}{L_{nw}} I_o \cdot \left[1 - \exp\left(\frac{V_{DS}}{V_t}\right)\right] \cdot \frac{\exp\left[-\frac{V_{GS} - V_{TH}}{nV_t}\right]}{1 + \exp\left[-\frac{V_{GS} - V_{TH}}{nV_t}\right]}, \quad (11)$$

where I_0 is the fitting parameter, n is non-ideality factor, and V_t is the thermal voltage.

Case 2: When $V_{TH} < V_{TG} < V_{FBT}$ and V_{TG} - V_{FBT} + $V_{dep} > V_{DS}$, only the center portion in the nanowire is neutral and there are no accumulation channel. Therefore, current conduction occurs through the center neutral region and the device is operating in the linear region. Since the drain end of the center neutral channel is not pinched off, the body current is expressed as

$$I_{body} = -Q_n^{'} \frac{\mu_{n0}}{1 - \frac{\mu_{n0}}{v_{sat}} \frac{\partial V}{\partial y}} \frac{dV}{dy}. \quad (12)$$

In (12), by moving the denominator to the left hand side and integrating from source to drain by using (5), the body current is expressed as

$$I_{body} = \frac{\mu_{n0}}{L_{nw} - \frac{\mu_{n0}}{v_{sat}} V_{DS}} qN_d A,$$
$$A = W_{nw} t_{nw} V_{DS} - W_{nw}\left[F_1(V_{DS}) + F_2(V_{DS}) - F_1(0) - F_2(0)\right] - 2t_{nw}\left[F_3(V_{DS}) - F_3(0)\right] + 2\left[F_4(V_{DS}) - F_4(0)\right], \quad (13)$$

$$F_1(V) = \frac{W_{nw}\varepsilon_{nw}}{C_{iT}^{'}}\left[-V + \frac{qN_d \varepsilon_{nw} W_{nw}^2}{3C_{iT}^{'2}}\left(1 - \frac{2C_{iT}^{'2}}{qN_d \varepsilon_{nw} W_{nw}^2}(V_{TG} - V_{FBT} - V)\right)^{3/2}\right], \quad (14)$$

$$F_2(V) = \frac{W_{nw}\varepsilon_{nw}}{C_{iB}^{'}}\left[-V + \frac{qN_d \varepsilon_{nw} W_{nw}^2}{3C_{iB}^{'2}}\left(1 - \frac{2C_{iB}^{'2}}{qN_d \varepsilon_{nw} W_{nw}^2}(V_{BG} - V_{FBB} - V)\right)^{3/2}\right], \quad (15)$$

$$F_3(V) = \frac{t_{nw}\varepsilon_{nw}}{C_{iT}^{'}}\left[-V + \frac{qN_d \varepsilon_{nw} t_{nw}^2}{3C_{iT}^{'2}}\left(1 - \frac{2C_{iT}^{'2}}{qN_d \varepsilon_{nw} t_{nw}^2}(V_{TG} - V_{FBT} - V)\right)^{3/2}\right], \quad (16)$$

$$F_4(V) = -\frac{t_{nw}\varepsilon_{nw}}{C_{iT}^{'}} F_1(V) - \frac{W_{nw}\varepsilon_{nw}}{C_{iT}^{'}} F_3(V) - \frac{W_{nw} t_{nw} \varepsilon_{nw}^2}{C_{iT}^{'2}}$$
$$\left\{V - \left[\frac{qN_d \varepsilon_{nw}}{8C_{iT}^{'2}}\left(t_{nw}^2 + W_{nw}^2\right) - \frac{1}{2}(V_{TG} - V_{FBT} - V)\right] F_{41}(V)\right.$$
$$- \frac{qN_d \varepsilon_{nw}}{4C_{iT}^{'2}}\left[W_{nw} t_{nw} - \frac{1}{4W_{nw} t_{nw}}\left(t_{nw}^2 + W_{nw}^2\right)^2\right]$$
$$\left.\log\left[\frac{1}{2}\left(\frac{W_{nw}}{t_{nw}} + \frac{t_{nw}}{W_{nw}}\right) - \frac{2C_{iT}^{'2}}{qN_d \varepsilon_{nw} W_{nw} t_{nw}}(V_{TG} - V_{FBT} - V) + F_{41}(V)\right]\right\}, \quad (17)$$

$$F_{41}(V) = \sqrt{1 - \frac{2C_{iT}^{'2}}{qN_d \varepsilon_{nw} W_{nw}^2 t_{nw}^2}\left(t_{nw}^2 + W_{nw}^2\right)(V_{TG} - V_{FBT} - V) + \frac{4C_{iT}^{'4}}{q^2 N_d^2 \varepsilon_{nw}^2 W_{nw}^2 t_{nw}^2}(V_{TG} - V_{FBT} - V)^2}. \quad (18)$$

$$V_{pn1} = \frac{qN_d \varepsilon_{nw} W^2}{8\left(\frac{t_{nw}}{\varepsilon_{nw} W_{nw}} + \frac{1}{C_{iT}^{'}} + \frac{1}{C_{iB}^{'}}\right)^2}$$
$$\left\{\left[\frac{t_{nw}^2}{\varepsilon_{nw}^2 W_{nw}^2} + \frac{2t_{nw}}{\varepsilon_{nw} W_{nw}}\left(\frac{1}{C_{iT}^{'}} + \frac{1}{C_{iB}^{'}}\right) + \frac{2}{C_{iT}^{'} C_{iB}^{'}}\right.\right.$$
$$\left.+ \frac{2}{qN_d \varepsilon_{nw} W_{nw}^2}(V_{TG} + V_{BG} - V_{FBT} - V_{FBB})\right]^2 \quad (19)$$
$$- 4\left[\frac{1}{C_{iT}^{'2} C_{iB}^{'2}} - \frac{2}{qN_d \varepsilon_{nW} W_{nw}^2 C_{iT}^{'2}}(V_{BG} - V_{FBB}) - \frac{2}{qN_d \varepsilon_{nW} W_{nw}^2 C_{iT}^{'2}}(V_{TG} - V_{FBT})\right.$$
$$\left.\left. + \frac{4}{q^2 N_d^2 \varepsilon_{nw} W_{nw}^4}(V_{BG} - V_{FBB})(V_{TG} - V_{FBT})\right]\right\}$$

Case 3: When $V_{TH} < V_{TG} < V_{FBT}$ and V_{TG} - V_{FBT} + $V_{dep} \leq V_{DS}$, the center neutral channel is pinched off but there is neither accumulation channel nor full depletion of the nanowire. Therefore, current conduction occurs through the center neutral region and the device is operating in the saturation region. The channel potential at the pinched-off point (V_{pn}) where the center neutral channel is pinched off can be obtained from the pinched-off condition of a center neutral point. There are two cases of the pinch-off condition and the pinched-off potential as follows

1. Pinched-off condition 1 of the vertical direction in the nanowire: $t_{nw} = x_{dT}(V_{pn1}) + x_{dB}(V_{pn1})$, and by applying the pinched-off condition 1, V_{pn1} is represented as (19).
2. Pinched-off condition 2 of the lateral direction in the nanowire: $W_{nw} = 2x_{dS}(V_{pn2})$, and by applying the pinched-off condition 2, V_{pn2} is represented as

$$V_{pn2} = V_{TG} - V_{FBT} + \frac{qN_d t_{nw} W_{nw}}{2C'_{iT}}\left(1 + \frac{C'_{iT} W_{nw}}{4\varepsilon_{nw} t_{nw}}\right). \quad (20)$$

The effective V_{pn} is given by $V_{pn} = \min(V_{pn1}, V_{pn2})$. Since the drain end of the center neutral channel is pinched off, the drain current is expressed by modifying the body current of Case 2 as

$$\begin{aligned} I_{body} &= \frac{\mu_{n0}}{L_{nw} - \frac{\mu_{n0}}{v_{sat}} V_{DS}} qN_d B, \\ B &= W_{nw} t_{nw} V_{pn} - W_{nw}\left[F_1(V_{pn}) + F_2(V_{pn}) - F_1(0) - F_2(0)\right] \\ &\quad -2t_{nw}\left[F_3(V_{pn}) - F_3(0)\right] + 2\left[F_4(V_{pn}) - F_4(0)\right]. \end{aligned} \quad (21)$$

Case 4: When $V_{TG} \geq V_{FBT}$ and V_{TG} - $V_{FBT} > V_{DS}$, the depletion region due to the top-gate disappears and the nanowire surface below the top-gate is in accumulation from the source to the drain. Therefore, current conduction occurs through the center neutral channel as well as the accumulated surface channel. Since both the center neutral channel and the accumulated surface channel are not pinched off, the body current and the accumulation current are operating in the linear region. In (12), by moving the denominator to the left hand side and integrating from source to drain by using Q'_n in (6), the body current is expressed as

$$I_{body} = \frac{\mu_{n0}}{L_{nw} - \frac{\mu_{n0}}{v_{sat}} V_{DS}} qN_d W_{nw}\left[t_{nw} V_{DS} - F_2(V_{DS}) + F_2(0)\right]. \quad (22)$$

When the accumulated surface channel is not pinched off, the accumulation current is expressed as

$$I_{acc} = -Q'_{acc} \frac{\mu_{s0}}{1 - \frac{\mu_{s0}}{v_{sat}} \frac{\partial V}{\partial y}} \frac{dV}{dy}. \quad (23)$$

In (23), by moving the denominator to the left hand side and integrating from source to drain by using Q'_{acc} in (6), the accumulation current is expressed as

$$I_{acc} = \frac{\mu_{s0} C'_{iT}}{L_{nw} - \frac{\mu_{s0}}{v_{sat}} V_{DS}}\left[\left(V_{TG} - V_{FBT}\right) V_{DS} - \frac{V_{DS}^2}{2}\right]. \quad (24)$$

$$\begin{aligned} I_{body} &= \frac{\mu_{n0}}{L_{nW} - \frac{\mu_{n0}}{v_{sat}} V_{DS}}\left[\int_0^{V_{TG}-V_{FBT}} qN_d W_{nw}(t_{nw} - x_{dB}) dV \right. \\ &\quad \left. + \int_{V_{TG}-V_{FBT}}^{V_{DS}} qN_d (W_{nw} - 2x_{dS})(t_{nw} - x_{dT} - x_{dB})\right] \\ &= \frac{\mu_{n0}}{L_{nw} - \frac{\mu_{n0}}{v_{sat}} V_{DS}} qN_d \{W_{nw}\left[t_{nw}(V_{TG} - V_{FBT})\right. \\ &\quad \left. - F_2(V_{TG} - V_{FBT}) + F_2(0)\right] + C\}, \\ C &= W_{nw} t_{nw}(V_{DS} - V_{TG} + V_{FBT}) \\ &\quad -W_{nw}[F_1(V_{DS}) + F_2(V_{DS}) \\ &\quad -F_1(V_{TG} - V_{FBT}) - F_2(V_{TG} - V_{FBT}) \\ &\quad -2t_{nw}[F_3(V_{DS}) - F_3(V_{TG} - V_{FBT}) \\ &\quad +2[F_4(V_{DS}) - F_4(V_{TG} - V_{FBT}) \end{aligned} \quad (25)$$

Case 5: When $V_{TG} \geq V_{FBT}$, V_{TG} - V_{FBT} + $V_{dep} > V_{DS}$, and V_{TG} - $V_{FBT} \leq V_{DS}$, the center neutral channel is not pinched off and there is accumulation at the source end. In addition, the accumulated surface channel is pinched off. The current conduction occurs through the center neutral channel as well as the accumulated surface channel. Therefore, by using the similar method for Case 4 except for the two-segment approach in which the center neutral region is divided with two segments for the body current, the body current and the accumulation current are

expressed as

$$I_{acc} = \frac{1}{2}\frac{\mu_{s0} C'_{iT}}{L_{nw} - \frac{\mu_{s0}}{v_{sat}} V_{DS}} \left(V_{TG} - V_{FBT}\right)^2 . \quad (26)$$

Case 6: When $V_{TG} \geq V_{FBT}$, V_{TG} - V_{FBT} + $V_{dep} \leq V_{DS}$, and V_{TG} - $V_{FBT} \leq V_{DS}$, both the center neutral channel and the accumulated surface channel are pinched off. However, the accumulated surface channel and the center neutral channel are not pinched off at the same lateral location. The accumulated channel is pinched off earlier. Therefore, by using the similar method for Case 4 except for three-segment approach in which the center neutral region is divided with three segments for the body current, the body current is expressed as

$$I_{body} = \frac{\mu_{n0}}{L_{nw} - \frac{\mu_{n0}}{v_{sat}} V_{DS}} \left[\int_0^{V_{TG}-V_{FBT}} qN_d W_{nw}(t_{nw} - x_{dB}) dV + \int_{V_{TG}-V_{FBT}}^{V_{pn}} qN_d (W_{nw} - 2x_{dS})(t_{nw} - x_{dT} - x_{dB}) DV \right],$$

$$I_{body} = \frac{\mu_{n0}}{L_{nw} - \frac{\mu_{n0}}{v_{sat}} V_{DS}} qN_d \{ W_{nw} [t_{nw}(V_{TG} - V_{FBT}) - F_2(V_{TG} - V_{FBT}) + F_2(0)] + D \}, \quad (27)$$

$$D = W_{nw} t_{nw}(V_{pn} - V_{TG} + V_{FBT}) - W_{nw} [F_1(V_{pn}) + F_2(V_{pn}) - F_1(V_{TG} - V_{FBT}) - F_2(V_{TG} - V_{FBT})] - 2t_{nw} [F_3(V_{pn}) - F_3(V_{TG} - V_{FBT})] + 2 [F_4(V_{pn}) - F_4(V_{TG} - V_{FBT})]$$

The accumulation current is the same to Eq. (26).

The drain-source current is the sum of the body current and the accumulation current.

5. Extrinsic Characteristics

Fig. 4 shows an equivalent circuit of the NWFET, separated the intrinsic part and the extrinsic part. The equivalent circuit of the NWFET consists of two Schottky diodes (for MS contacts) connected back-to-back in series with an intrinsic top-gate depletion-mode NWFET. Here V_{Si} is the voltage of the intrinsic source node and V_{Di} is that of the intrinsic drain node. It has been reported that electron transport mechanism for the MS barrier in NWFETs at the forward bias and the reverse bias are TE and TFE, respectively [15, 16] and the reported Schottky diode model for the MS contacts [16, 20] is used. We simulate the equivalent circuit with the circuit simulator, ADS [21]. To implement the intrinsic part and the extrinsic part (two Schottky diodes) in the NWFET into ADS, each part utilizes a Symbolically Defined Device (SDD) of the equation-based nonlinear model in ADS, based on the above represented equations for the drain-source current and the Schottky diode current [16, 20].

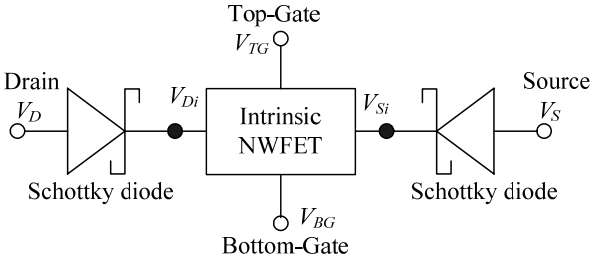

Fig. 4. Equivalent circuit of the NWFET.

III. Model Verifications

Fig. 5 shows the drain current-drain voltage (I_{DS}-V_{DS}) characteristics of an n-type GaN NWFET with top-gate structure as a function of the top-gate voltage (V_{TG}). Symbols and lines denote the experimental data [9] and the data fitted by the newly developed top-gate NWFET model, respectively. Parameters fitted by the newly

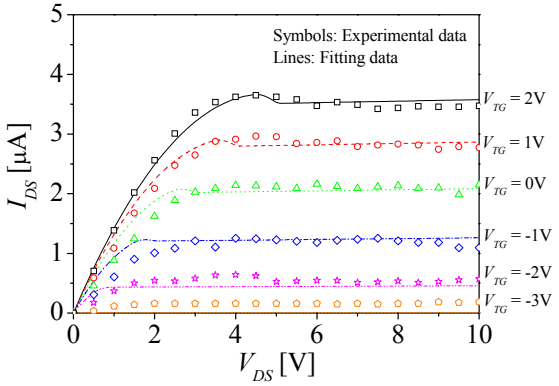

Fig. 5. I_{DS}-V_{DS} characteristics of an n-type GaN NWFET with top-gate structure as a function of V_{TG}.

developed model are t_{iT} = 40 nm, t_{iB} = 1 μm, t_{nw} = W_{nw} = 30 nm, L_{nw} = 3 μm, N_d = 1.0×10^{18} cm^{-3}, V_{FBT} = -2.5 V, V_{FBB} = -0.8 V, μ_{n0} = 95 cm^2/Vs, v_{sat} = 5×10^7 cm/s, k_1 =1.0, θ = 0.5, α = 2, n = 1.5, and I_0 = 2×10^{-8} A. Parameters for the MS contacts, fitted by the newly developed model, the Schottky barrier height ϕ_B = 0.2 eV [16, 20], which means that the MS contacts have nearly ohmic barriers.

Fig. 6 shows I_{DS}-V_{DS} characteristics of an n-type ZnO NWFET with top-gate structure as a function of V_{TG}. Symbols and lines denote the experimental data [7] and the data fitted by the newly developed top-gate NWFET model, respectively. Parameters fitted by the newly developed model are t_{iT} = 50 nm, t_{iB} = 10 μm, t_{nw} = W_{nw} = 150 nm, L_{nw} = 7 μm, N_d = 2.0×10^{16} cm^{-3}, V_{FBT} = -3.0 V, V_{FBB} = -0.8 V, μ_{n0} = 1.3 cm^2/Vs, v_{sat} = 1×10^5 cm/s, k_1 =1.0, θ = 0.01, α = 2, n = 1.5, and I_0 = 2×10^{-8} A. Parameters for the MS contacts, fitted by the newly developed model, ϕ_B = 0.1 eV [16, 20], which means that the MS contacts have nearly ohmic barriers. The mobility estimated from the newly developed model is five times as large as that from the enhancement-mode MOSFET model as shown in [7], which means that our model can give better estimation of device characteristics than the enhancement-mode MOSFET model. Because the mobility extraction used in [7] excludes two MS contacts, the exact intrinsic drain-source voltage is not used, and therefore, the mobility_extraction in [7] can have some error. Fig. 5 and Fig. 6 show that the results simulated from the newly developed top-gate NWFET model reproduce considerably well the experimental results.

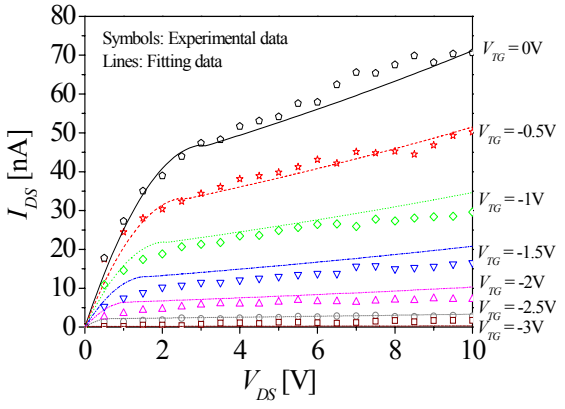

Fig. 6. I_{DS} I_{DS}-V_{DS} characteristics of an n-type ZnO NWFET with top-gate structure as a function of V_{TG}.

IV. CONCLUSIONS

We have proposed a semi-analytical current conduction model for depletion-mode n-type NWFETs with top-gate structure. The NWFET model was based on an equivalent circuit consisting of two back-to-back Schottky diodes for the MS contacts and the intrinsic NWFET. The intrinsic NWFET model was derived from the current conduction mechanisms due to bulk charges through the center neutral region as well as of accumulation charges through the surface accumulation region, and thus it included all current conduction mechanisms of the top-gate NWFET operating at various top-gate bias conditions. Our previously developed Schottky diode model was used for the M-S contacts. The newly developed model was implemented to ADS, in which the extrinsic part (Schottky diode model) and intrinsic part of the NWFET were developed by utilizing the SDD for an equation-based nonlinear model. The results simulated from the newly developed NWFET model reproduced considerably well the reported experimental results.

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