Simulation and Modelling of the Write/Erase Kinetics and the Retention Time of Single Electron Memory at Room Temperature

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Abstract—**In this work, we propose a single electron memory 'SEM' design which consist of two key blocs: A memory bloc, with a voltage source V_{Mem}, a pure capacitor connected to a tunnel junction through a metallic memory node coupled to the second bloc which is a Single Electron Transistor "SET" through a coupling capacitance. The "SET" detects the potential variation of the memory node by the injection of electrons one by one in which the drain-source current is presented during the memory charge and discharge phases. We verify the design of the SET/SEM cell by the SIMON tool. Finally, we have developed a MAPLE code to predict the retention time and nonvolatility of various SEM structures with a wide operating temperature range.**

Index Terms—**Single electron transistor, single electron memory, retention time, SET/SEM, SIMON**

I. INTRODUCTION

Since the pioneering work achieved about a decade ago by Likharev on the possibility of single electronics [1], much research has been done on the modelling and the realization of memory devices based on the single-electron tunnelling phenomena [2-3]. A SEM should work with a reasonable bit error rate, have low power, scalability to the sub-nanometre regime and extremely high charge sensitivity [4].Several single electron memory cells have been proposed in the literature such us the single electron flip-flop, the electron trap proposed by Nakazato and Ahmed [5] based on a dynamic memory cell and the single-electron ring memory which is "similar" to the electron trap memory because it is a trap connected to a ring. However the operation is different.

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In this paper, we explain the operating principle and the electrical model of new SET/SEM device. To have a good idea about capacitances and resistances of tunnel junction, we present SEM simulation results, obtained with SIMON [7], in Write/Read/Erase cycles. Moreover, we have developed a code for the simulation of the kinetic of charge and discharge. Using this code, we are able to compute the retention times with different structures to determine an optimal structure with wide operating temperature range and provide more non-volatility.

II. SINGLE ELECTRON MEMORIES

Various designs have been proposed during the past years to establish a better overview of the state of the single electron memories art. The power consumption of SET memories is usually smaller than that of conventional memories, due to the minuteness of capacitances and the limited umber of electrons concerned in charging and discharging, However, high integration densities and high switching speed may lead to unacceptable power dissipation of 3 kW/cm [3].

One of the most promising applications of single electronics is the single-electron memory. To have a good single electron memory operation, some criteria are necessary [4]. The First criterion is the operation temperature. In fact, the memory cell must operate at room temperature or at least at liquid helium temperature for the time being. Second, its bits error rate must be reasonable, along with low power consumption. Manufacturability is the last but not the least criterion.

III. A NEW SET/SEM DEVICE

1. Design and Electrical Modelling

Each SEM proposed in the literature differs from the other by such properties as the complexity of the architecture, the dependence of background charges, the operating temperature.

In our case, we will expand our current-voltage characteristics study in order to obtain a multi-bit memory structure in which we need at least two islands: one island used in the SET for reading and another for memorization.

This structure is made of two key blocs: a bloc of memory(write/erase), with a voltage source 'V$_{Mem}$', a pure capacitor 'Cgt' connected to a tunnel junction 'Ct' through metallic memory node coupled to the second bloc which is a Single Electron Transistor 'SET' through a coupling capacitance 'Cg'.

We can polarize the drain of SET with a low and constant bias potential 'V$_D$'. In order to simplify the architecture, we put the source in the ground.
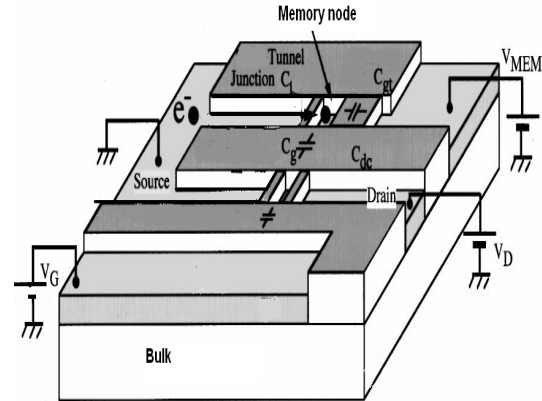

Fig. 1. A new SET/SEM architecture formed of two blocs: the memory bloc (write/erase process) and SET reading bloc are independent due to a thick oxide layer between the memory node and island SET.

The substrate choice can be viewed as the manufacturing technique that varies from one manufacturer to another. However, some studies have proved the benefit of α-Al$_2$O$_3$ .Other substrates can be used including a silicon substrate doped appropriately. In 2007, a Sherbrooke team had used a silicon substrate in their chemical mechanical polishing technique (CMP) to fabricate single electron transistor with the Titanium island based on a nanowire structure [7]. In fact, the SET island is created by patterning a Ti line perpendicular to the oxide trench. The line is oxidized in pure oxygen to grow 2 to 12 nm of TiOx depending on oxidation time and temperature. This TiOx on the Ti line sidewalls constitutes the tunnel junction dielectric layer. In this structure, the Titanium island of SET is embedded in the SiO$_2$. The result of the CMP process is the formation simultaneous of the source, drain and island of the SET with thickness of 2 nm. In SET/SEM structure presented in figure 1, we need 4 electrodes: one for the memory and three for the SET (source, drain and gate). The oxide between memory node and reading SET may be a layer of partially oxidized Titanium 'TiO$_x$' which determines the sensitivity of the SET. The SET/SEM can have one or more islands, in the reading SET, which can be fixed with the possibility of manufacturing and of the dedicated application [8]. In our case, we assume that the SET has only one Titanium island.

To investigate the relation between the device's geometric parameters and the single-charging effects in the electrical characteristics, we present in Fig. 2 a simplified electrical model.
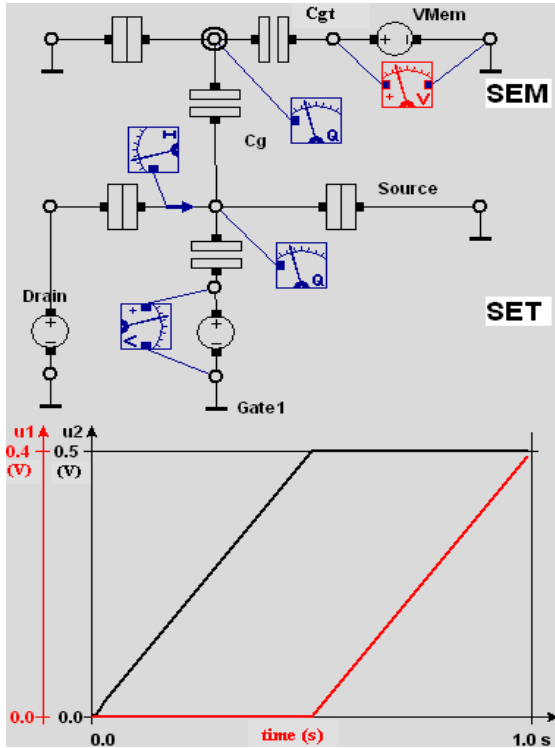
Fig. 2. Electrical model of the physical architecture using SIMON: In the right of the figure, the timing diagram of the write voltage (V_{Mem}=u2 (t)) applied to the programming bloc and the reading voltage u1(t) applied to the gate of the SET.

We neglect the island-substrate capacitance, as the latter has a negative effect on the observation of Coulomb blockade, and we will also ignore the quantum confinement and the island depletion. We have modelled the SET/SEM as a system of two electrical models: the first is the C-SET because of capacitive coupling between the gate and the central island and the second is a vertical single electron box which consists of a single tunnel junction and a capacitor in series.

The shape of control signals (u1(t)=Vg, u2(t)=V_{Mem}) is very important to observe the charge evolution 'Q' versus time. In order to break this lock, different potential signals were applied but it has retained for writing a starting ramp of 0s and for reading a ramp which starts just after writing.

The various coupling capacitances between device elements, such as the capacitance of tunnel junction 'Ct', Cgt, and Cg, are extracted from SIMON simulator after several trials using stationary simulation. In fact, for every such time step all piece-wise-linear time dependent the voltage source as considered as constant. And every such time step 'even number' tunnel events are simulated and averaged. For the purposes mentioned above, it was

therefore important to understand the operating mode of SET / SEM structure.

2. Principle of Operation

The single-electron transistor was connected to the memory node of the single-electron memory to detect the potential change of the memory node by the injection of the individual electrons.

Concerning the schemes workings of the proposed memory, we can consider three operation modes: writing, reading and erasing. The writing mode consists of recording information in the memory while erasing comprehends evacuating the stored charges. The writing and erasing data mode are made by applying different voltages to the entry points of the cell. In the case of a SEM, the memory node is ready to store information. The programming is done by controlling V_{Mem}.

The tunnel junction capacitor (Ct), the pure capacitance Cgt and the capacitance Cg are connected like a letter T. The memory node is capacitively coupled to the reading bloc via Cg which modelises a thick oxide layer, so the capacitance Cg is not considered in the programming mode. One-by-one electron transfer is achieved by increasing the bias V_{Mem}. Vt is the total charge divided by the sum of the capacitances by which the electrons can penetrate after applying the memory bias VMem. Initially there are no electrons in the memory node. The memory node potential Vt is Vt=V_{Mem}.Cgt/(Cgt+Ct) .

If we only consider the bloc memory, the voltage node Vt in the memory is expressed as the following:

$$V_t = \frac{C_{gt}V_{Mem} - ne}{C_{gt} + C_t} \qquad (1)$$

C_{gt} is the capacitance between memory node and the drain electrode, C_t is the capacitance between memory node and the ground, n is the number of electrons in the memory node, V_{Mem} is the SEM polarization and e is the elementary charge.

The SEM capacitance values used in the SIMON simulation are equal: $C_{gt} = C_t = 2.7 aF$ in order to have 8 charge levels. When the memory node potential

exceeds the coulomb gap bias of tunnel junction "V_0", an electron can tunnel through the tunnel junction towards the memory node , therefore the potential of the memory node will be decreased by (e/Ct+Cgt): (n=1).

The voltage drop from the maximum voltage node V_0 can be written as:

$$\Delta V_t = \frac{e}{C_{gt} + C_t} = 29,629 \; mV \qquad (2)$$

By increasing V_{Mem}, the potential in the node increases as well. When the charge energy is higher than Coulomb energy 'Ec' (eVt> Ec), an electron can pass from the junction tunnel to the node by reducing Vt till the value of the coulomb gap bias of tunnel junction "V_0".

By further increasing V_{Mem}, Vt increases again till the value V_0. At this time a second electron passes to the storage node and Vt decreases again. And so on until the injection of N electrons one by one is done with. In Fig. 3, we represent the evolution of the memory node potential Vt versus V_{Mem}. As for the writing mode, we have just applied a particular form of potential which is a positive ramp available in the library of SIMON simulator (V_{Mem} =0.5 V).

Indeed, we wanted to work with a low voltage value to respect the fact that the device operates at an electron in a small gap voltage in order to minimize power consumption. The number of written charges depends on the value of Cgt and Ct.

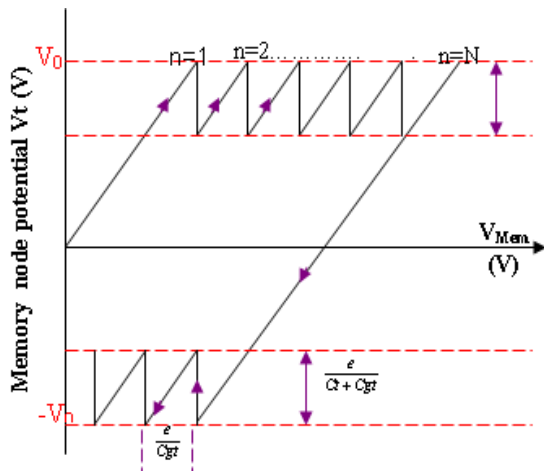Concerning the erasing process, we have applied a negative slop ramp. Thus, the storage node evacuates

electron by electron to the ground whenever Vt is higher than V_0 in absolute value. The erasing speed depends on the slope of the applied ramp.

The memory reading process is realized by a SET which will read the state's load circuit writing. This reading is carried out horizontally by polarizing the gate Vg. In our case Vg is a growing echelon (Vg= 0.4 V) applied just after writing in our memory between 0.5s and 1s as shown in Fig. 2. The sizing of the value of Cg is very important: if the Cg is very low (of the order of 1E-22 aF), we can not read memory. After several SIMON simulations, the Cg value is set at 1aF.

IV. SIMULATION RESULTS AND DISCUSSION

1. SET /SEM Simulation Using SIMON

The operating temperature of nano-devices used in the simulation has an impact on the characteristics Id-Vg and on the potential existence of the Coulomb blockade phenomena. The values of island -electrode capacitances have also a great influence on the charge energy.

The islands number existing in the SET has an effect on the total capacitance between the drain and the source and subsequent energy loading. The bias voltage value plays an important role in the current peak values.

In Fig. 4, we present the drain current versus the gate voltage "Id-Vg characteristic" for SET reading. The drain is biased by a voltage Vd = 20 mV, the coupling capacitance between the two blocs is Cg = 1 aF, the tunnel

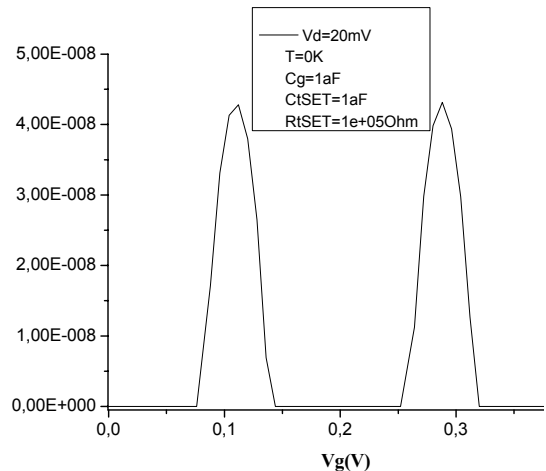**Fig. 3.** Dependence of the potential memory node 'Vt' of external voltage 'V_{Mem}'.

Fig. 4. SIMON simulation results of Id-Vg characteristic in the Reading SET at 0K for a symmetric SET.

junctions of the SET (CtSET and RtSET) are symmetrical (CtSET = 1aF, RtSET = 10^5 Ohm) and the operating temperature is zero to show better Coulomb oscillations. The current changes periodically and varies so sensitively on CgVg.

Fig. 5(a) and Fig. 5(b) present the two timing diagrams Write/Erase respectively of V_{Mem} and reading Vg and the current Id depending on the voltage gate. It is found out that the portion of the curve, representing the reading of the state, has shifted compared to that of the discharged state. The gap is 56.229 mV which represents the contribution of voltage in the SET. It's the equivalent of an additive voltage 7.028 mV for each passage of one electron to the storage node [Fig. 5(c)]. The drain current versus gate voltage for a programmed and erased cell is shown in Fig. 6.

A very interesting idea that brings multiple benefits to nanotechnology is to have a multi-level memory to a single electron. In this context, it has tried to highlight the discrete of the charge and energy charge for each passage of the electron node memory.
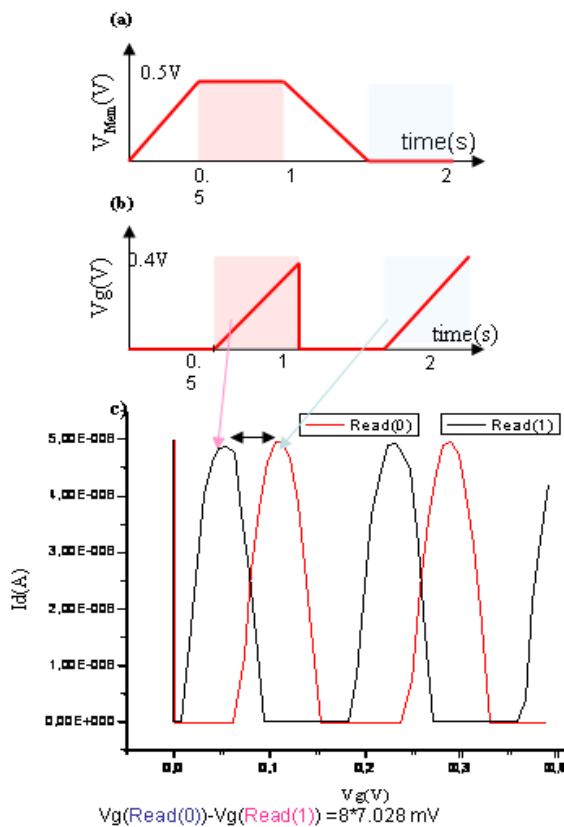

Fig. 5. (a) The signal pulse 'V_{Mem}' during Write/Ease cycles.(b) The signal pulse 'Vg' during read cycles (c) Drain current in the charge and discharge phase of memory.
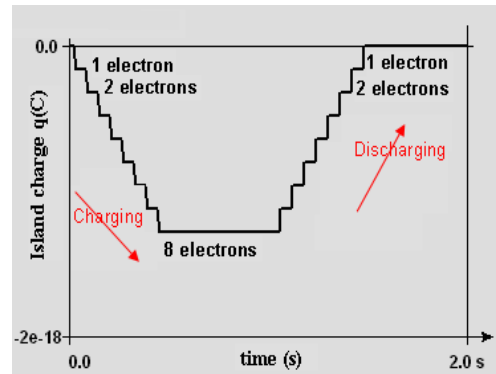

Fig. 6. Quantization of the electric charge in the write /erase phases as a function of time.

Determining the shape of the charge Q(t) in the island allows us to count the number of electrons stored in the memory node and to know at the instant 't' is there writing or erasing.

Fig. 6 presents the state of charge as a function of time simulation fixed in SIMON simulator.

Fig. 6 presents the SIMON simulation result and shows that there are 8 electrons in the memory node after the charging. Since energy levels are discrete, each state of charge or energy level is associated with an addition of an electron. For a shaft with 8 energy levels, each equal to one bit. Thus, when the structure is blank on a logic (000) will V^1_{island} worth reading. For a single charge correspond to logic (001) and therefore another V^2_{island}, and so "7 electrons" in island associated with logic (111) for each $V^7_{îlot}$ measurable. Through this strategy, we will determine a value of gate voltage Vg each drain current reading.

2. Commitment Folder

Following this new model proposed in paragraph III, we have fixed the electronic parameters of the SET/SEM structure (capacitances and resistors values) to get a commitment folder. It can be consistent with the actual parameters we can expect virtually with the best manufacturing technique. Hence, we get a structure working at large temperature. For these raisons, we have taken the same conditions and parameters of the SET realized at the University of Sherbrooke in 2007 [4].

For the value of the capacity of the tunnel junction fixed in the electric model (0.34 aF), we calculate the distance between the island and the drain, we obtain a tunnel junction with the following geometric parameters:

the TiO$_x$ oxide has 2.53 nm of length and 2 nm of high.

Since we have a purely capacitive coupling between the electrode polarization V$_{Mem}$ and the memory node, we can increase the oxide thickness 'TiO$_x$', therefore decrease the value of capacitance C$_{GT}$. After many simulations, we adopt C$_{GT}$ = 0.1 aF and we have an oxide thickness equal to 6.831 nm between the electrode and the memory node.

For the width of two tunnel junctions used in the memory bloc, we have taken the same width of the memory node which is fixed at 10 nm.

Table 1 and Table 2 resume the different geometric and electronic parameters considered in the SET/SEM structure.

Table 1. Reading SET parameters

Simulations parameters	Device parameters (en nm)
C$_{island-drain}$= 0.34aF	Oxide length =2
C$_{island\_source}$= 0.34aF =C$_{island\_drain}$	Oxide width=10
C$_{gate}$= 0.22aF	Oxide thickness=2
C$_{Total}$= 1aF	Titanium island (L=60;W=10 and height= 2)
R$_{Source}$=R$_{Drain}$= 5.7 10^{7}Ω	

Table Notes: C$_{island\_drain}$, C$_{island\_source}$, C$_{island\_drain}$ and C$_{gate}$ are the drain, source, gate and total capacitance respectively. R$_{Source}$ and R$_{Drain}$ are the source and drain junction resistance. The device parameters represent the junction length and width while L and W are the island length and width respectively. : we adopt a Titanium parallelepiped island and the TiO$_x$ oxide.

Table 2. Single Electron Memory parameters

Simulations parameters	Device parameters (en nm)
C$_t$= 0.27aF	d$_{island\_ground}$= 2.53 d$_{island\_electrode}$ = 6.83
C$_{gt}$= 0.1aF	Tunnel width = 10
C$_g$= 0.05aF	Oxide tunnel height =2
V$_{Mem}$= 0.4V	Oxide thickness between two blocks= 82.1
R$_{tunnel}$ = 5.7 10^7 Ω	Memory node (L=60; W=10 and height= 2)

Table Notes: C$_t$, C$_{gt}$ and C$_g$ are the junction tunnel capacitance, pure capacitance between memory node and electrode polarization and coupling capacitance respectively. R$_{tunnel}$ is the tunnel resistance of the tunnel junction. d$_{island\_ground}$ is the distance between island and ground, d$_{island\_electrode}$ is the distance between island and V$_{Mem}$ electrode. $\varepsilon_{[TiOx]} = 3.85$ is the relative permittivity, $\Phi_B = 0.3\,eV$ is the barrier height and $m^*_{[TiOx]} = 0.4\,m$ is the effective weight.

V. RETENTION TIME

The retention time is an important parameter of our single electron memory. To improve his retention time, three alternatives have been proposed. The first alternative was to change the dimensional parameters of structure. The second lied in changing the environmental characteristics. The last alternative was the material modifications.

Both the materials' choice and the temperature of operation combined with a MAPLE [9]code that determines the discharge kinetics can now predict in advance the retention time of several memory structures at different extended temperatures. The improved performance of the SET / SEM structure without changing its architecture is a challenge in this article through the use of judiciously selected materials.

The total current in the memory node J$_{Tot}$ is the summation of the thermionic current Jth with the tunnel J$_{TD}$ or Fowler Nordheim J$_{FN}$ current neglecting the electron transport from the memory node to V$_{Mem}$ electrode. To bascule from mechanism to another depend on the value of an electrical field. In fact, the total current in the memory node is given by the following expression [10]:

$$J_{Tot} = Jth + \delta(\frac{\phi_B}{q} - F_{OT}.d_{OT})J_{TD} + (1 - \delta(\frac{\phi_B}{q} - F_{OT}.d_{OT}))J_{FN} \quad (3)$$

Where

$$\begin{cases} \delta(\frac{\phi_B}{q} - F_{OT}d_{OT}) = 1 & if \frac{\phi_B}{q} - F_{OT}d_{OT} > 0 \\ \delta(\frac{\phi_B}{q} - F_{OT}d_{OT}) = 0 & if \frac{\phi_B}{q} - F_{OT}d_{OT} < 0 \end{cases} \quad (4)$$

q is elementary charge and Φ_B is the barrier height.

The retention time is calculated according to industrial criteria (85% of the discharge time) with a MAPLE code. Have a look at Fig. 7.

In our model, the discharging current during retention is dominated by electrons tunnelling out from memory node to the ground. Since the external potential V$_{Mem}$ is zero biased during retention and the number of charges stored in the metallic island is limited, the electric field in the tunnelling dielectric is low. As a result, the tunnelling mechanism is direct tunnelling and because
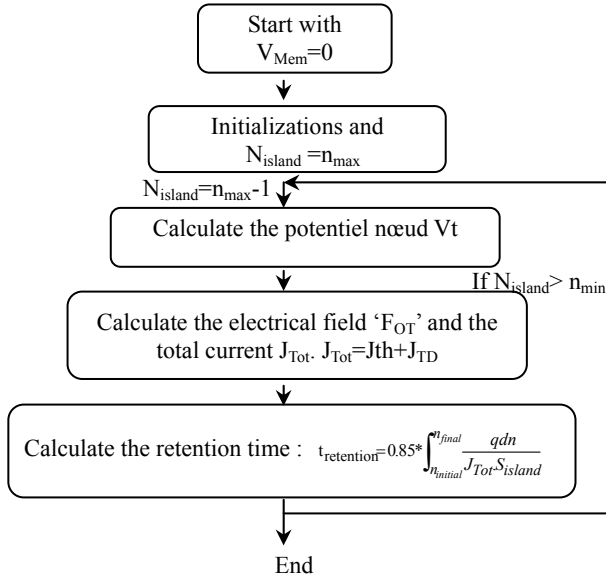
Fig. 7. Flowchart that calculates the retention time of SEM. Jth is the thermionic current, J_{TD} is the direct tunnel current and S_{island} = (2 nm*10 nm). n_{max} is the maximum number of electrons in the island, n_{min} is 0 and N_{island} is the number of electrons memorized in the memory node.

the FN conduction occurs at high electric field. For this reason, $\frac{\phi_B}{q} > F_{OT}.d_{OT}$ and the total current is the addition of thermoionic and direct tunnel current. (as shown in the fourth stage of the last flowchart).

Indeed, the retention time of memories depends strongly on the height of the potential barrier between the Fermi level of metal and the conduction band of oxide.

We compare the retention time of single electron memories to different metallic islands. First we consider an Aluminium island between two SiO_2 tunnel junctions each having an electronic affinity of 0.9 eV. Then, a Titanium island which has a work function of 3.95 eV is between two TiO_x oxide layers. From Fig. 8(a) and Fig. 8(b), we can determine 85% of discharge time. We conclude that the retention time in the case of an Aliminium island for $Al/SiO_2/ Al/SiO_2/Al$ SEM structure is much larger than that in the case of the Titanium island ($Ti/TiO_x/ Ti/TiO_x/Ti$ structure).

In the following part, we will present a comparative study for different high barriers. For a Ti/TiO_2 junction, we have the following parameters: the relative permittivity: $\varepsilon r[TiO2] = 85$; the effective weight $m^*[TiO2] = 3m_0$, the electronic affinity $EA_{(TiO2)} = \chi = 3.9$ eV [11] , the Titanium work function $\Phi_{Ti} = 3.95$ eV [12].
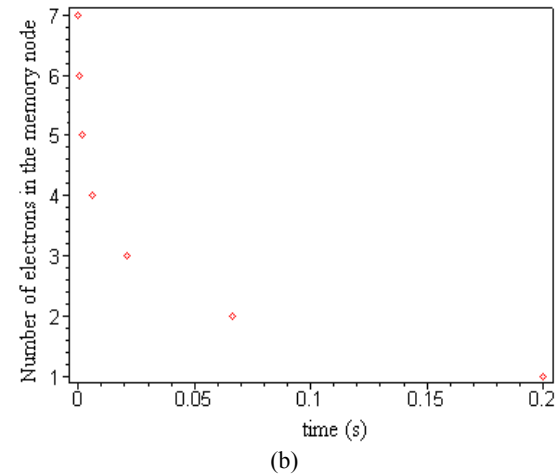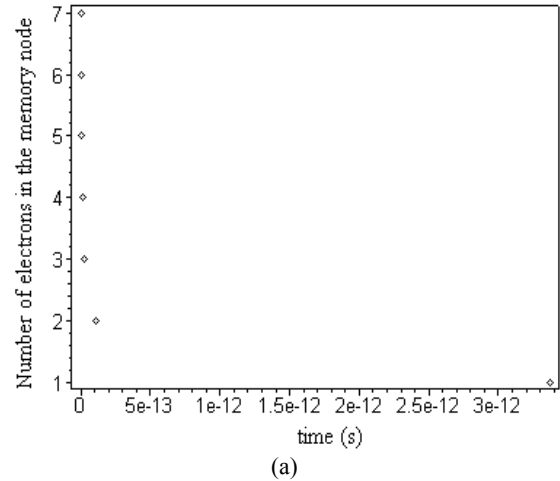

(a)

(b)

Fig. 8. (a) Discharge curve of 7 electrons to one, for Ti / TiO_x barrier height of 0.3 eV (b) Discharge curve of 7 electrons to one, for Al/ SiO_2 barrier height of 3.25 eV. The temperature of operation is 300K.

The height of the barrier is defined as the difference between the metal work function and silicon electronic affinity [13]. The height of the Ti/TiO_2 barrier is determined as following:

$$q\Phi b = q(\Phi_{Ti} - \chi) = 0.5 \text{ eV} \qquad (5)$$

Due to MAPLE code simulation, the retention time obtained for $m^* = 0.4m_0$, $\varepsilon_r = 3.85$ and the barrier of 0.3 eV is 0.00017 second, while that for $m^* = 3m_0$, $\varepsilon = 85$ and the height of barrier 0.5 eV is 0.05274432 second.

Below is a table that succinctly summarizes the performance of different retention time for the following barriers Ti / TiO_x, Ti/TiO_2, Pt/TiO_2, iSi/TiO_2, $TiSi_2/TiO_2$, $NiSi/TiO_2$ and Ti/SiO_2.

(See Table 3).

Table 3. Retention time for different metals for large temperatures

Barriers and electronics parameters	Retention time at T=300K (s)	Retention time at T=430K (s)
Ti/TiO$_x$ (m*=0. 4m$_0$,εr=3.85ε_0, Φ_B=0. 3eV)	1.7E-4	2.5E-6
Ti/TiO$_x$ (m*=0. 4m$_0$,εr=4,36 ε_0, Φ_B=0. 4eV)	1.6 E-2	7.4E-5
Ti/TiO$_2$ (m*=0. 5m$_0$, εr=85ε_0,Φ_B=0. 5 eV)	5 E-2	7.4E-5
Pt/TiO$_2$ (m*=3m$_0$,εr=85ε_0, Φ_B=1. 41 eV)	1.02 E14	3.43 E7
TiSi/TiO$_2$ (m*= 3m$_0$,εr=85ε_0, Φ_B=1. 64 eV)	7.4 E17	1.7E9
TiSi$_2$/TiO$_2$ (m*= 3m$_0$,εr=85ε_0, Φ_B=0.63 eV)	8.05	2.24E-3
NiSi/TiO$_2$ (m*=0. 5m$_0$, εr=85ε_0, Φ_B=0.78 eV)	2666	0.1418
Ti/SiO$_2$ (m*=0.5m0, εr=3.9ε0, Φ_B= 3.05eV)	2.17 E20	6.86 E08 >22 years

These simulations allowed us to predict the memory structure MIMIM gives us the maximum retention time with optimal geometric parameters of the structure for large temperatures up to 300K. Finally, we fixed our choice to realize a single electron memory with Ti/SiO$_2$/Ti/SiO$_2$/Ti structure which has a retention time (6.86 E08 second) which exceeds 22 years at 430K. This structure not only has a long retention time but also has small dimensions so low-power nature.

This result is quite impressive, since the retention time of current Silicon SEM as the storage node is after the order of weeks. This retention time is very important especially at the height barrier between the minimum of the conduction band of SiO$_2$ and the Fermi level of Titanium.

VI. Conclusions

To sum up, we have fixed in this paper a commitment folder and we have explained the principal of operation of a new single electron memory based on two islands. The design of SET/SEM has been presented and verified by the SIMON tool. We have developed a code for the simulation of erase process. Due to this code, we are able to compute the retention time at the temperatures of 300 K and 430 K. This allowed us to test the non-volatility of SEMs structures with different metallic memory nodes. A very long retention time up to 22 years is obtained for nonvolatile single electron memory. A technological challenge has been launched today which is to realize a memory SEM multi-bit storage providing electrons levels in discrete nanocrystal. However, the proposed SET / SEM has a metal bloc so there are no discrete energy levels.

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