Comparative Study on the Structural Dependence of Logic Gate Delays in Double-Gate and Triple-Gate FinFETs

Kwan Young Kim, Jae Man Jang, Dae Youn Yun, Dong Myong Kim, and Dae Hwan Kim

***Abstract*—A comparative study on the trade-off between the drive current and the total gate capacitance in double-gate (DG) and triple-gate (TG) FinFETs is performed by using 3-D device simulation. As the first result, we found that the optimum ratio of the hardmask oxide thickness (T_{mask}) to the sidewall oxide thickness (T_{ox}) is T_{mask}/T_{ox}=10/2 nm for the minimum logic delay (τ) while T_{mask}/T_{ox}=5/1~2 nm for the maximum intrinsic gate capacitance coupling ratio (*ICR*) with the fixed channel length (L_G) and the fin width (W_{fin}) under the short channel effect criterion. It means that the TG FinFET is not under the optimal condition in terms of the circuit performance. Second, under optimized T_{mask}/T_{ox}, the propagation delay (τ) decreases with the increasing fin height H_{fin}. It means that the FinFET-based logic circuit operation goes into the drive current-dominant regime rather than the input gate load capacitance-dominant regime as H_{fin} increases. In the end, the sensitivity of $\Delta\tau/\Delta H_{fin}$ or $\Delta I_{ON}'/\Delta H_{fin}$ decreases as L_G/W_{fin} is scaled-down. However, W_{fin} should be carefully designed especially in circuits that are strongly influenced by the self-capacitance or a physical layout because the scaling of W_{fin} is followed by the increase of the self-capacitance portion in the total load capacitance.**

***Index Terms*—Double-gate, drive current, finFET, intrinsic coupling ratio, logic gate delay, parasitic coupling ratio, total gate capacitance, triple-gate**

I. INTRODUCTION

With continuous scaling down of metal-oxide-semiconductor field-effect transistors (MOSFETs) into the nanometer regime, the scaling theory has faced serious technological difficulties. Especially in planar MOSFETs, short channel effects (SCEs) have been very challenging to efficiently control, despite deploying the silicon-on-insulator (SOI) technology, channel/gate engineering, and the ultrathin-body (UTB) structure. On the other hand, non-planar three-dimensional (3-D) transistors are expected to be promising novel device structures to circumvent hurdles of SCEs through the strong control of the electrostatic channel potential by multiple gates [1]. 3-D MOSFET structures, such as double-gate (DG) and triple-gate (TG) FinFETs, provide not only superior immunity to SCEs, the ideal subthreshold slope, and the higher drive current but also the compatibility with conventional CMOS process technology [2]. Although the research on 3-D transistors has been recently in active progress, most design guidelines for device parameters have been focused on the DC characteristics including SCEs or the drive current [3, 4] and the hot carrier reliability [5]. In nano-scale digital VLSI circuits, on the other hand, it is worthwhile to elaborately control both the parasitic capacitance and capacitive coupling between the input and the output in order to estimate the influence on the circuit performance [6]. As the structure of 3-D MOSFETs is getting more complicated, as a performance-booster, a systematic optimization of the trade-off between the gate capacitance and the drive current plays a significant role in the circuit performance.

FinFETs, on the other hand, are often fabricated by

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using the spacer fin patterning technique with a hard mask oxide or SiN on the top of the Si-fin to define the nano-scale feature size beyond the state-of-the-art lithography. The narrow multi-fin structure, which has flexible controllability on the drive current and circuit implementation, can be efficiently formed by spacer fin patterning [7]. Therefore, the drive current of TG FinFETs can be higher than that of DG FinFETs for the same fin size [8], because a thin gate oxide is used in the top channel of the Si-fin as is the case in the sidewall channel. Nevertheless, the intrinsic gate delay in TG FinFETs is not necessarily shorter than that in DG FinFETs because the total gate capacitance (the fan-out capacitance in the case of a chain of the logic gates) in the former is larger than that in the latter [9]. Therefore, there is a room to further optimize the top oxide (or hard mask oxide) thickness (T_{mask}) and the sidewall oxide thickness (T_{ox}) of the Si-fin for the improved logic gate delay. Furthermore, the height (H_{fin}) and the width (W_{fin}) of the Si-fin, which are determined at the initial front-end-of-line (FEOL) process step, should be transferred from the process parameters regime to the circuit design parameters regime in which the resolution of the drive current, controlled by the trimming revision of the back-end-of-line (BEOL), is limited by H_{fin} and W_{fin}.

In this work, motivated by the requirement of the unified design guide for T_{mask}, T_{ox}, H_{fin}, and W_{fin} for the logic gate delay, a comparative study on the trade-off between the drive current and total gate capacitance in DG and TG FinFETs is performed by using a TCAD 3-D device simulation [10, 11]. In addition to T_{mask}, T_{ox}, H_{fin}, and W_{fin} as design parameters, the ratio of the gate-to-drain coupling capacitance (C_{GD}) to the total gate capacitance (C_{total}) and the margin to process variations are also investigated.

II. FUNDAMENTAL SIMULATION FRAMEWORK

For improved DC and AC characteristics in FinFETs, several parameters should be considered in the design. As described in Section I, even in the case of a single-fin FET, each parameter critically influences the circuit performance. Therefore, the controlled part of the single-fin FET geometry in the simulation should be well defined as a prerequisite for unified design guidelines. In this Section, the fundamental simulation result on the DC characteristics is shown with geometrical design parameters.

1. Design Parameter in FinFETs

Geometrical parameters for the single-fin FET simulation are shown in Fig. 1. Device parameters are as follows: the relation between the gate length (L_G) and W_{fin} is fixed at L_G=1.5×W_{fin} as the well-known criteria for ideal SCEs in FETs [1]. According to this rule of thumb, L_G=50, 30, and 20 nm correspond to W_{fin}=30, 20, and 10 nm, respectively. Variable parameters in the device simulation include T_{ox} (=1~2 nm), T_{mask} (=1~10 nm), W_{fin} (=10~30 nm, corresponding L_G=20~50 nm), and H_{fin} (=20~60 nm) as summarized in Table 1. The other parameters are fixed as follows: the separation between the source/drain (S/D) contact and the gate (L_{sp}=30 nm), the height of the poly-Si gate (T_{poly}=50 nm), the sidewall thickness of the poly-Si gate (L_{poly}=20 nm), and the overlap length of S/D-to-gate (L_{ov}=4 nm; overlap S/D profile with σ=1 nm/dec [12]).

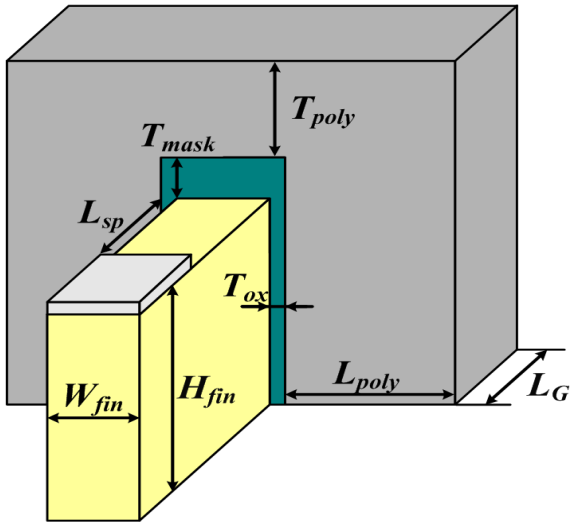

Fig. 1. The device structure and geometric parameters of the single-fin FET. The relation between L_G and W_{fin} is fixed at L_G=1.5×W_{fin} as the well-known criteria for ideal SCEs in FETs.

Table 1. Variable parameters in the device simulation

L_G [nm]	W_{fin} [nm]	T_{ox} [nm]	T_{mask} [nm]	H_{fin} [nm]	T_{poly} [nm]	L_{ov} [nm]	L_{poly} [nm]
50 30 20	30 20 10	1 2	1 2 5 10	20 40 60	50	4	20

While the conditions of T_{mask} /T_{ox}=1/1 and/or 2/2 nm correspond to TG FinFETs, the other conditions of T_{mask} /T_{ox} work as DG FinFETs (see Table 1). In addition, the quantum effects in the Si-fin are also incorporated in the 3-D device simulation.

Most of the split parameters affect each other in complicated manner and consequently determine the respective components in the total gate capacitance C_{total}. On the other hand, fixed parameters do not play a significant role in the logic gate delay or reflect the process-dependent parts [9]. However, it should be noted that I_{ON} (the drive current at V_G=V_D=V_{DD}) of FinFETs does not show a dramatic variation with the fluctuation of geometrical parameters, especially in the investigated range over H_{fin}=20~60 nm and W_{fin}=10~30 nm, while that of Si nanowire FETs with a surrounding gate is very sensitive to the variation of geometrical parameters [13].

2. DC Parameters and SCEs of FinFETs

Fig. 2 shows I_{DS}-V_{GS} and C-V_{GS} characteristics of single-fin DG and TG FinFETs as a function of T_{mask} for

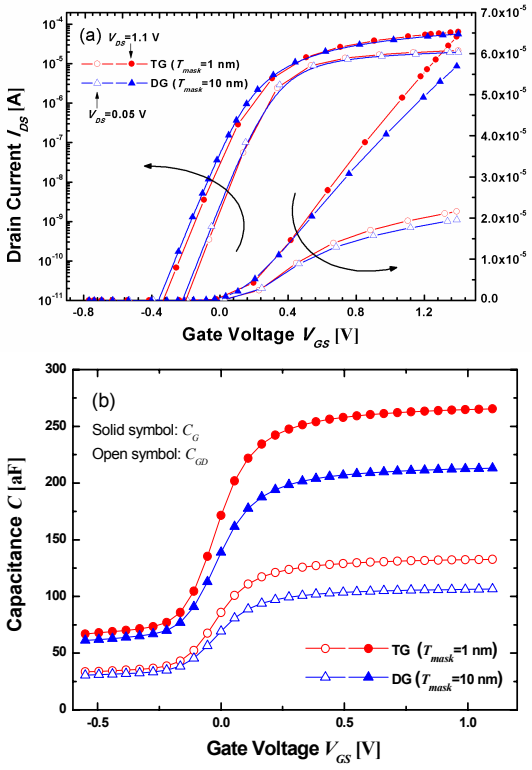

Fig. 2. (a) I_{DS}-V_{GS} and (b) C-V_{GS} characteristics of FinFETs with different T_{mask} for L_G=50 nm, H_{fin}=40 nm, W_{fin}=30 nm, and T_{ox}=1 nm. I_{ON} and C_{total} of the TG FinFET are larger than those of the DG FinFET.

L_G=50 nm, H_{fin}=40 nm, W_{fin}=30 nm, and T_{ox}=1 nm. It is clear that both I_{ON} and C_{total} of the TG FinFET are larger than those of the DG FinFET. Because the criteria for the suppression of SCEs (the subthreshold swing SS≤100 [mV/dec] and the drain-induced barrier lowering $DIBL$ ≤100 [mV/V]) [14] are satisfied as shown in Table 2, SCEs are efficiently suppressed in the simulation conditions. Moreover, DC parameters in the simulation results are consistent with previously reported experimental data [9].

Table 2. DC and SCE parameters in FinFETs

L_G [nm]	T_{mask} [nm]	V_T [V]	SS [mV/dec]	$DIBL$ [mV/V]
50	1 10	0.21 0.20	86.4 89.7	80 90
20	1 10	0.23 0.23	95.6 96.6	100 110

III. Simulation Results and Discussion

In this Section, the establishment of design guide for single-fin FETs is pursued by analyzing the structural dependence of C_{total}, I_{ON}, and τ (the intrinsic logic gate delay) at supply voltage V_{DD}=1.1 V. τ is estimated from the simulation results of C_{total} and I_{ON}. For the purpose of more systematic approach, C_{total} is decomposed into the intrinsic gate capacitance (C_{in}) and the parasitic self-capacitance (C_p). Furthermore, the sensitivity of process variations is discussed.

1. Decomposition of the Total Gate Capacitance C_{total}

In Fig. 3, various capacitance components consisting of C_{total} are defined with C_{Tmask} as the intrinsic gate capacitance between the gate and the top of the fin, C_{Tox} as the intrinsic gate capacitance between the gate and sidewall of the fin, C_{Tfr} as the gate-to-S/D fringing capacitance through the top of the fin, C_{Tov} as the gate-to-S/D overlap capacitance through T_{mask}, C_{Sfr} as the gate-to-S/D fringing capacitance through the sidewall of the fin, and C_{Sov} as the gate-to-S/D overlap capacitance through T_{ox}, respectively. C_{total} includes all of the fringing field effects for the inner and outer fringing fields over the insulator, except the contact-to-contact fields [15].

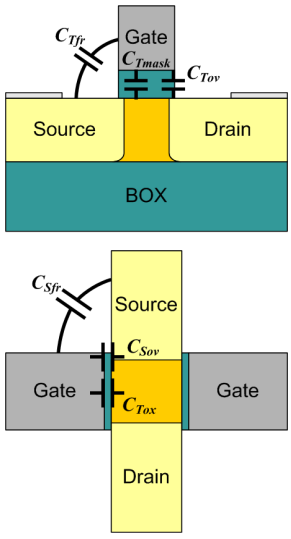

Fig. 3. Capacitance components consisting of C_{total}. While C_{Tmask} and C_{Tox} correspond to C_{in}'s, C_{Tfr}, C_{Sfr}, C_{Tov}, and C_{Sov} do C_p's.

Then, C_{total} can be obtained from

$$\begin{aligned} C_{total} &= L_G \times W_{fin} \times C_{Tmask}' + 2L_G \times H_{fin} \times C_{Tox}' \\ &+ 2T_{poly} \times W_{fin} \times C_{Tfr}' + 2L_{ov} \times W_{fin} \times C_{Tov}' \\ &+ 4L_{poly} \times H_{fin} \times C_{Sfr}' + 4L_{ov} \times H_{fin} \times C_{Sov}' \end{aligned} \quad (1)$$

with C_i' defined as the capacitance of C_i per unit area. Then, by applying the fixed parameters (T_{poly}=50 nm, L_{ov}=4 nm, and L_{poly}=20 nm), C_{total} can be re-described as

$$C_{total} = C_1 + C_2 + C_3 + C_4 \quad (2)$$

$$C_1 = L_G \times W_{fin} \times C_{Tmask}' \quad (3)$$

$$C_2 = 100W_{fin} \times C_{Tfr}' + 8W_{fin} \times C_{Tov}' \quad (4)$$

$$C_3 = 2L_G \times H_{fin} \times C_{Tox}' \quad (5)$$

$$C_4 = 80H_{fin} \times C_{Sfr}' + 16H_{fin} \times C_{Sov}' \quad (6)$$

where $C_{in} \equiv C_1 + C_3$ and $C_p \equiv C_2 + C_4$, respectively. Eq. (2) can be re-described as the sum of the W_{fin}-dependent term and the H_{fin}-dependent term written by

$$C_{total} = AW_{fin} + BH_{fin} \quad (7)$$

$$A = L_G \times C_{Tmask}' + 100C_{Tfr}' + 4C_{Tov}' \quad (8)$$

$$B = 2L_G \times C_{Tox}' + 80C_{Sfr}' + 16C_{Sov}' \quad (9)$$

For fixed L_G, T_{mask}, and T_{ox}, the constants A and B are independent of W_{fin} and/or H_{fin}. Therefore, A and B can be extracted by using the simulation result of C_{total} as a function of various sets of H_{fin} and W_{fin}.

With the definition of the *intrinsic coupling ratio* $ICR \equiv (C_1+C_3)/C_{total}$, and the *parasitic coupling ratio* $PCR \equiv (C_2+C_4)/C_{total}$ (=1–*ICR*), Fig. 4 shows the W_{fin}- and H_{fin}-dependence of *ICR* in TG and DG FinFETs. As *ICR* increases, the design and analysis of the FinFET- based logic circuit by using the simple RC model become more reasonable. In contrast, as *PCR* increases, the performance of the logic gate becomes more sensitive to the layout, 3-D physical structure, and the Miller effect. As shown in Fig. 4, while the *ICR* for W_{fin}=20~30 nm lies in the range of 0.5~0.8, it is lower than 0.5 for W_{fin}=10~20 nm.

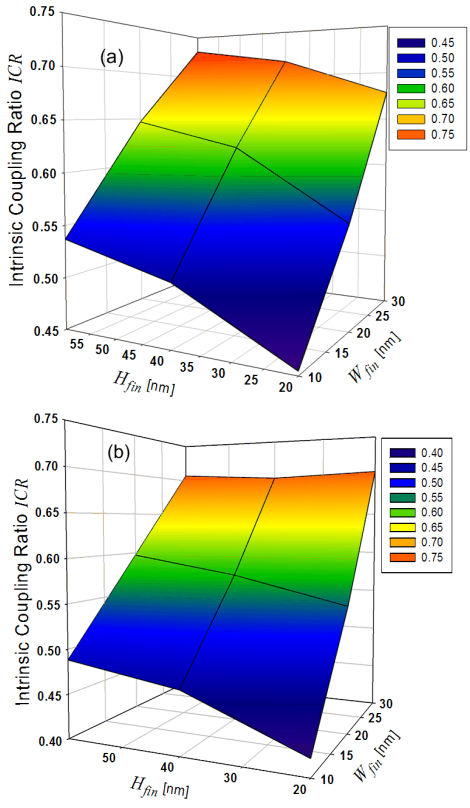

Fig. 4. The W_{fin}- and H_{fin}-dependence of *ICR* in (a) DG FinFET (with T_{mask}=10 nm and T_{ox}=1 nm) and (b) TG FinFET (with T_{mask}=1 nm and T_{ox}=1 nm). While the *ICR* for W_{fin}=20~30 nm lies in the range of 0.5~0.8, it is lower than 0.5 for W_{fin}=10~20 nm.

2. Geometrical Dependence of the Intrinsic Coupling Ratio *ICR*

As shown in Figs. 5 and 6, the W_{fin}-dependence of *ICR* is more significant than the H_{fin}-dependence. Here, Fig. 5 shows the case of T_{ox}=1 nm and Fig. 6 does T_{ox}=2 nm,

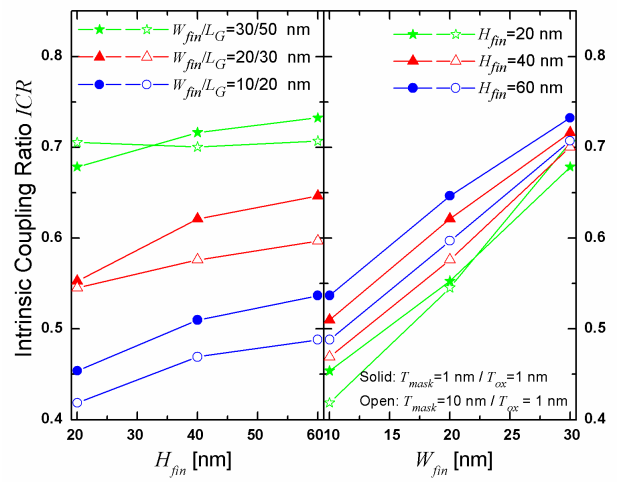

Fig. 5. The W_{fin}- and H_{fin}-dependences of *ICR* in DG (T_{mask}/T_{ox}=10/1 nm) and TG FinFET (T_{mask}/T_{ox}=1/1 nm) in the case of T_{ox}=1 nm.

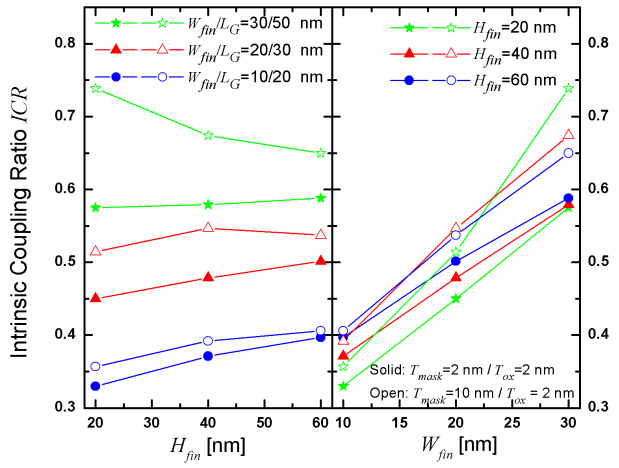

Fig. 6. The W_{fin}- and H_{fin}-dependences of *ICR* in DG (T_{mask}/T_{ox}=10/2 nm) and TG FinFET (T_{mask}/T_{ox}=2/2 nm) in the case of T_{ox}=2 nm.

respectively. Considering the pre-assumption of the simultaneous scaling of both W_{fin} and L_G, Figs. 5 and 6 show that *ICR* becomes shrunken down to a lower value than 0.5 from 45 nm LSTP (low standby power) technology node (L_G of FinFET≤30 nm) in the ITRS 2007. Assuming *ICR* >0.5 as the criterion of FinFETs, the crossover point lies in W_{fin}≤20 nm. In addition, in the case of T_{ox}=2 nm (Fig. 6), the DG FinFET is superior to the TG FinFET with respect to *ICR*. However, this superiority becomes less conspicuous with further scaling of L_G and W_{fin}.

The geometrical dependence of *ICR* is summarized in Figs. 7 and 8. W_{fin} is observed to be the most sensitive parameter to *ICR*. As H_{fin} increases, *PCR* decreases in

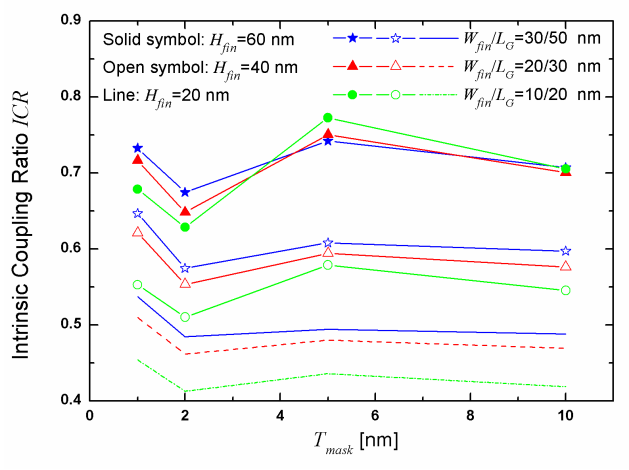

Fig. 7. The geometric dependence of *ICR* in the FinFET with T_{ox}=1 nm.

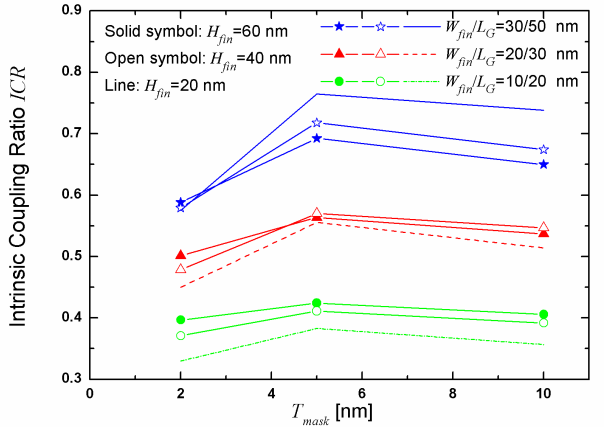

Fig. 8. The geometric dependence of *ICR* in the FinFET with T_{ox}=2 nm.

almost all of conditions. However, the H_{fin}-dependence of *PCR* is not so significant and *PCR* becomes higher than *ICR* for L_G≤30 nm as mentioned above. Given that the TG FinFET with T_{ox}=1 nm is not desired due to the dramatically increasing gate leakage current in spite of a high *ICR*, the optimum condition is T_{mask}/T_{ox}=5/1~2 nm. Especially, it is worth to note that the superiority of the *ICR* in the DG FinFET with the optimized T_{mask}/T_{ox} (=5/1~2 nm) to that in TG FinFET becomes more prominent with increasing the W_{fin}/L_G and/or H_{fin}.

Because of the strong T_{ox}-dependence of *PCR*, the variation of *PCR* (ΔC_p) due to a process variation of T_{ox} (ΔT_{ox}) is very important in the co-design of circuits with a 3-D FinFET technology. The H_{fin}-dependence of the sensitivity $\Delta C_p/\Delta T_{ox}$ is shown in Fig. 9, where the margin of C_p to the process variation of T_{ox} becomes more widened with the decrease of H_{fin}.

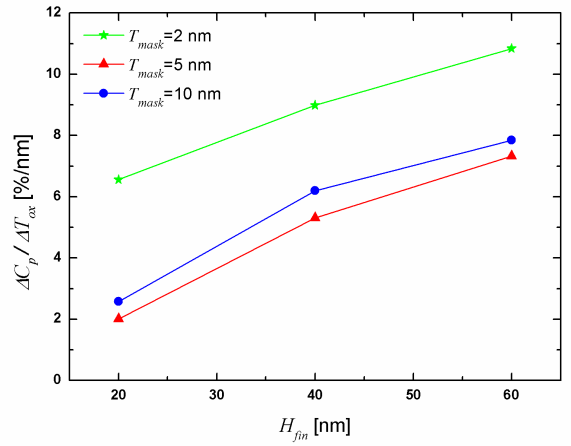

Fig. 9. The H_{fin}-dependence of $\Delta C_p/\Delta T_{ox}$. The margin of C_p to the process variation of T_{ox} becomes more widened as H_{fin} decreases.

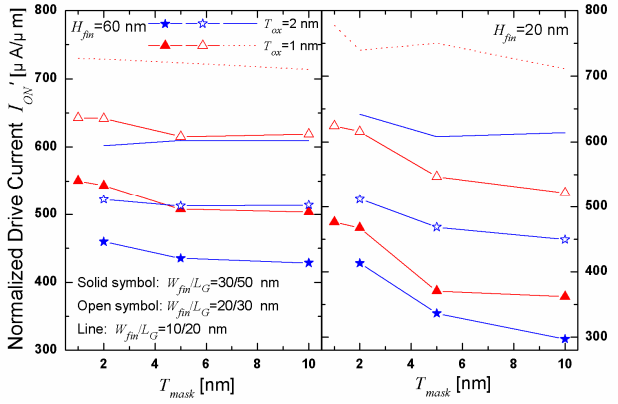

Fig. 10. The normalized drive current (I_{ON}') of FinFET as the functions of T_{mask} (1, 2, 5, and 10 nm), T_{ox} (1 and 2 nm), and H_{fin} (60 and 20 nm). I_{ON}' decreases as T_{mask} increases. Also, the I_{ON}' of TG FinFET is higher than that of DG FinFET.

3. The Drive Current Per Unit Channel Width I_{ON}' and Intrinsic Logic Gate Delay τ

With the definition of I_{ON}' as I_{ON} per unit channel width (=I_{ON}/(W_{fin}+2×H_{fin})), Fig. 10 shows the T_{mask}- and L_G/W_{fin}-dependence of I_{ON}'. Needless to say, I_{ON}' decreases as T_{mask} increases. Also, I_{ON}' of the TG FinFET is higher than that of the DG FinFET. As shown in Fig. 11 for the H_{fin}-dependence of I_{ON}' of TG (T_{mask}/T_{ox}=2/2 nm) and DG (T_{mask}/T_{ox}=10/2 nm) FinFETs, I_{ON}' increases with increasing H_{fin}.

Additionally, in order to investigate the immunity to process variations, the T_{mask}-dependence of $\Delta I_{ON}'/\Delta T_{mask}$ is shown in Fig.12. I_{ON}' is found to be the most sensitive to T_{mask} for T_{mask}=2~5 nm. On the other hands, as seen in Fig. 13 for the H_{fin}-dependence of $\Delta I_{ON}'/\Delta H_{fin}$, the ratio of $\Delta I_{ON}'/\Delta H_{fin}$ increases with the increase of H_{fin}. However, it is negligible compared with $\Delta I_{ON}'/\Delta T_{mask}$.

Finally, τ is estimated from C_{total} and I_{ON} and plotted in Fig. 14. For specific L_G and W_{fin}, τ is improved as T_{mask} increases. In other words, the TG FinFET is not the best

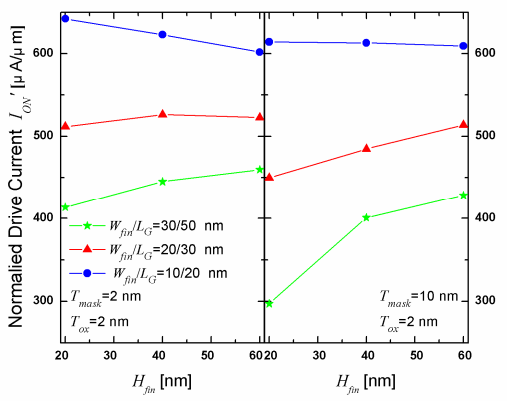

Fig. 11. I_{ON}' of DG and TG FinFETs as a function of H_{fin} and W_{fin}. I_{ON}' increases with the increase of H_{fin}.

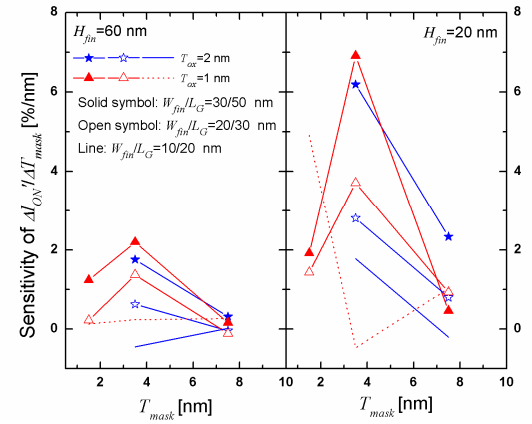

Fig. 12. $\Delta I_{ON}'/\Delta T_{mask}$ of FinFETs as the functions of T_{mask}, T_{ox}, and H_{fin}. I_{ON}' is the most sensitive to T_{mask} for T_{mask}=2~5 nm.

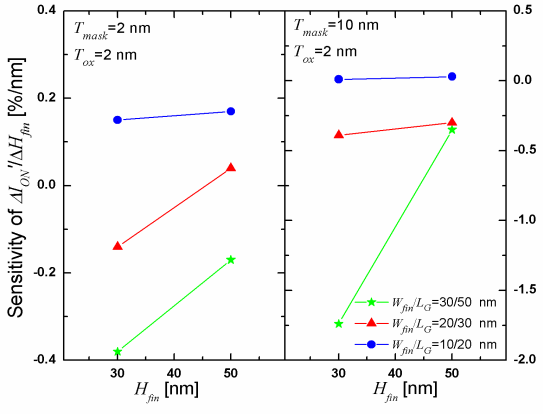

Fig. 13. $\Delta I_{ON}'/\Delta H_{fin}$ of DG and TG FinFETs for the variation of H_{fin} and W_{fin}.

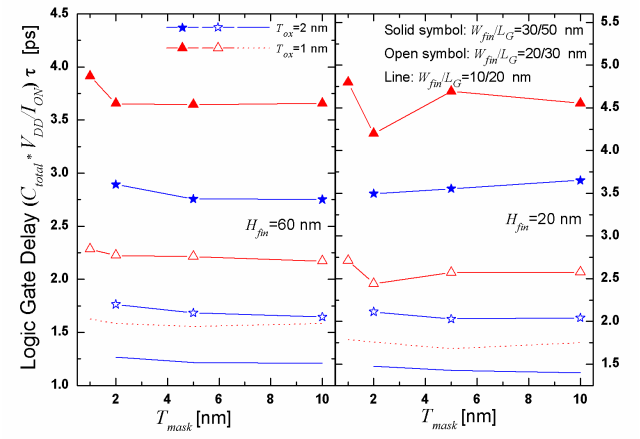

Fig. 14. τ of FinFETs as a function of T_{mask}, T_{ox}, H_{fin} and W_{fin}/L_G. τ is improved as T_{mask} increases. The condition for the minimum τ is T_{mask}/T_{ox}=10/2 nm.

solution in the viewpoint of the switching speed of the logic gate in spite of the maximum I_{ON}'. For the minimum τ, T_{mask}/T_{ox}=10/2 nm is the condition. Also, Fig. 15 shows the H_{fin}-dependence of τ. In cases of DG and

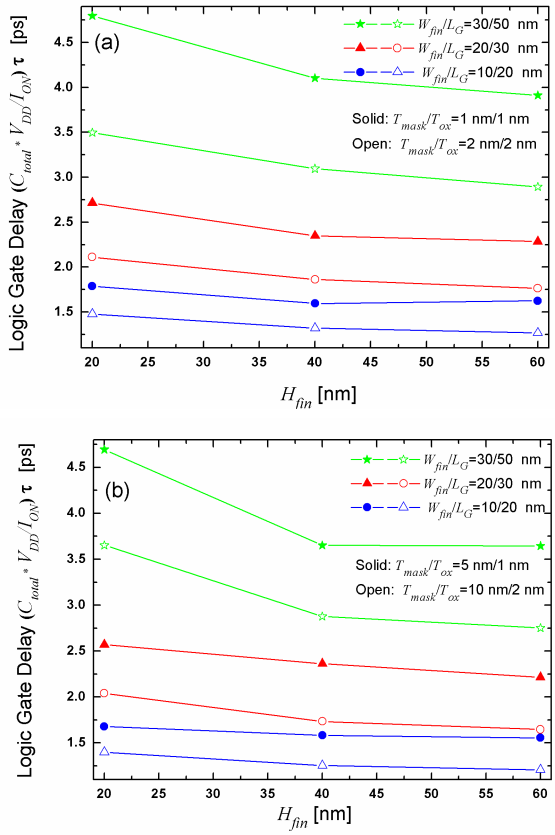

Fig. 15. The H_{fin}- and W_{fin}/L_G-dependence of τ (a) for TG FinFET (T_{mask}/T_{ox}=1/1 and 2/2 nm) and (b) for DG FinFET (T_{mask}/T_{ox}=5/1 and 10/2 nm). τ is improved as H_{fin} increases. It shows that the increase of I_{ON} becomes more prominent than the increase of C_{total}.

TG FinFETs, τ is improved as H_{fin} increases. It is because the increase of I_{ON} becomes more prominent than the increase of C_{total}. It means that the FinFET-based logic circuit operation goes into the drive current-dominant regime rather than the input gate load capacitance-dominant regime as H_{fin} increases. Therefore, H_{fin} should be designed as large as possible as long as the process technology is acceptable.

Table 3 summarizes the H_{fin}- and W_{fin}-dependence of $\Delta\tau/\Delta H_{fin}$. As the advantage of the DG FinFET becomes more significant, the precise control of T_{mask} and H_{fin} is strongly required. The sensitivity of τ to H_{fin} decreases with the increase of H_{fin}. Therefore, H_{fin} should be designed as large as possible in perspective of not only the performance but also the design for the process variability.

Table 3. The H_{fin}- and W_{fin}-dependence of $\Delta\tau/\Delta H_{fin}$

$\Delta\tau/\Delta H_{fin}$ [%/nm]			W_{fin} [nm]	30	20	10
Type	T_{mask} / T_{ox} [nm]/[nm]	H_{fin} change [nm]				
TG	1/1	20 → 40		-0.0347	-0.0183	-0.0096
		40 → 60		-0.0096	-0.0032	0.0015
	2/2	20 → 40		-0.0200	-0.0124	-0.0078
		40 → 60		-0.0101	-0.0050	-0.0027
DG	5/1	20 → 40		-0.0522	-0.0104	-0.0048
		40 → 60		-0.0003	-0.0074	-0.0014
	10/2	20 → 40		-0.0387	-0.0153	-0.0073
		40 → 60		-0.0063	-0.0044	-0.0022

IV. CONCLUSIONS

A comparative study on the trade-off between the drive current and the total gate capacitance in DG and TG FinFETs is investigated by using a 3-D device simulation. Our results are summarized as follows:

A. Under fixed L_G and W_{fin} in accordance with the SCE criterion, the optimum condition for the minimum τ is T_{mask}/T_{ox}=10/2 nm and T_{mask}/T_{ox}=5/1~2 nm for the maximum ICR, respectively. It means that the TG FinFET is not the optimal condition for the circuit performance. Therefore, the thickness of the hard

mask oxide (T_{mask}) should be elaborately controlled.

B. In addition, H_{fin} should be designed as large as possible for the circuit performance and the immunity to the process variation of T_{mask} and H_{fin} as long as the process technology is allowed. The H_{fin}-dependence of τ is originated from the increase of I_{ON}' with the increase of H_{fin}. The remaining issue is resolution of I_{ON} controllable by revision of the BEOL process.

C. As L_G and W_{fin} become further scaled-down, either $\Delta\tau/\Delta H_{fin}$ or $\Delta I_{ON}'/\Delta H_{fin}$ decreases. It is very optimistic in perspective of the margin to the process variation of critical parameters. However, W_{fin} should be carefully designed especially in circuits that are strongly influenced by the self-capacitance or the physical layout, for examples, the driver with a large load capacitance, I/O (input/output) interface circuit, and most analog blocks, because scaling of W_{fin} is followed by the increase of *PCR*. Another remaining issue is the hot carrier reliability. The immunity to hot carrier effects has been reported to be improved with increasing W_{fin} [5] and further study is required.

Therefore, when the logic circuits based on single-fin FET and/or multi-fin FET structures are physically designed, guidelines suggested in this work will be useful for the assessment of process variations, optimization of structures, and prediction of the circuit performance.

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