Effect of Counter-doping Thickness on Double-gate MOSFET Characteristics

George James T, Saji Joseph, and Vincent Mathew

Abstract—**This paper presents a study of the influence of variation of counter doping thickness on short channel effect in symmetric double-gate (DG) nano MOSFETs. Short channel effects are estimated from the computed values of current-voltage (I-V) characteristics. Two dimensional Quantum transport equations and Poisson equations are used to compute DG MOSFET characteristics. We found that the transconductance (g_m) and the drain conductance (g_d) increase with an increase in p-type counter-doping thickness (T_c). Very high value of transconductance (g_m= 38 mS/μm) is observed at 2.2 nm channel thickness. We have established that the threshold voltage of DG MOSFETs can be tuned by selecting the thickness of counter-doping in such device.**

Index Terms—**Quantum transport, DGMOSFET, threshold voltage, transcoductance, DIBL**

I. INTRODUCTION

The double-gate metal-oxide-semiconductor field-effect transistor (DG MOSFET) is a particularly promising candidate for ultimate CMOS scaling due to its good control of short channel effects (SCEs) such as the subthreshold slope and the drain induced barrier lowering (DIBL). The intimate coupling between the gates and the channel makes DG MOSFET technology the most scalable of all MOSFET designs [1]. The DG MOSFET is electrostatically superior to a single-gate MOSFET because two gates are used to control the channel from both sides. This allows additional gate length scaling by nearly a factor of two. The two gates together control roughly twice as much current as a single gate, resulting in stronger switching signals. The challenge lies in obtaining suitable threshold voltages Vt for high-speed logic devices, while controlling the extrinsic resistance [2]. In bulk MOSFETs, counter-doping is used at the surface to obtain low threshold voltages [3]. However, as a method to adjust the threshold voltage, undoped DG MOSFETs need to rely on gate work function to achieve multiple threshold voltages on a chip, but metal gates with work functions lower than that of n+ Si are not available [3, 4]. In this work, we are studying the possibility of adjusting threshold voltages for DG MOSFETs by varying the thickness of counter-doping located within a thin layer of n+ or p+ doped Si below and above the insulator. The structure of the DG MOSFET used in this paper is schematically presented in Fig. 1. This symmetric structure is characterized by two identical gates with no overlap with the source/drain extensions.

The study has been carried out using a method based on the two dimensional Quantum transport equations [5]. For 10 nm DG MOSFETs, the threshold voltage roll off

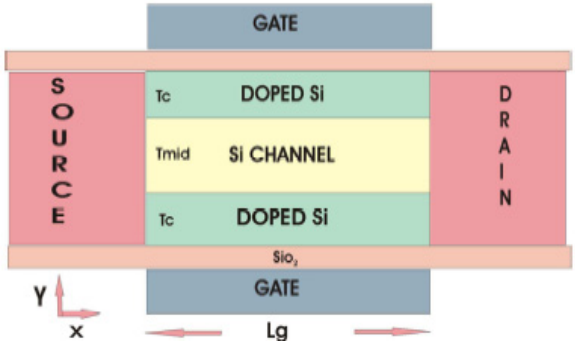

Fig. 1. A double-gate MOSFET structure with counter-doping. The 2D simulation domain is the portion excluding the top and bottom rectangles marked as 'Gate'.

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ΔVt, drain induced barrier lowering (DIBL) and degradation of the subthreshold swing (SS) are crucial issues that cannot be neglected. The calculated current-voltage (I-V) characteristics from our computation were analyzed and used to optimize DG MOSFETs.

II. SIMULATION

In the simulation scheme we employ the 3D effective mass Hamiltonian which is split in to a longitudinal part and a transverse part, since the width of the device is large compared to the other dimensions of the device. As pointed out previously [5], the MOSFET can then be considered as essentially a 2D charge sheet, enabling one to write the transverse eigen states as plane waves. The 3D Hamiltonian can then effectively be reduced to 2D longitudinal Hamiltonian H, if each transverse mode energy is added to the longitudinal energy to get the total energy, which can be written as

$$H = \frac{h^2}{2m_x^*}\frac{\partial^2}{\partial x^2} - \frac{h^2}{2m_y^*}\frac{\partial^2}{\partial y^2} + U_{sc} \qquad (1)$$

where m_x^*, m_y^* are the effective masses of electrons in the x and y directions respectively. We have added the self-consistent potential U_{SC} to the Hamiltonian.

The sub bands formed from the strong confinement in the vertical direction are calculated using the uncoupled mode space approach, which is based on the expansion of the 2D active device Hamiltonian in the sub band eigen function space [6]. In the uncoupled mode space approach, we need to solve the 1D Schrödinger equation along the y direction at each x-point of the finite difference grid to obtain the sub band energy levels and eigen functions (modes). The original 2D device Hamiltonian, when expanded in the above mode space, transforms into a 1D Hamiltonian in the transport direction, which can be solved to calculate the electron density ρ(r) and current within the Quantum transport equations, taking into consideration the effect of coupling of the channel to the source and drain contacts [5]. The self consistent potential U_{SC} is determined from the Poisson equation,

$$\nabla \cdot \varepsilon(r) \nabla \cdot U_{SC}(\vec{r}) = -\rho(\vec{r}) \qquad (2)$$

The process is repeated till a self consistent solution for electron density is reached. With the converged values of electron density and potential, the drain current is calculated. Uniformly-spaced grids are used in both x and y directions for solving the Poisson equation and the Quantum transport equations using the finite difference method.

We assume a metal gate contact Aluminum (Al) with work function 4.28 eV and 1 nm thick SiO_2 layers as the top and bottom gate dielectric. The source and drain regions included in the finite difference simulation grid are 3.2 nm in extension and have a uniform doping of 10^{20} cm^{-3}. The channel is made up of counter-doped layers with doping concentration 10^{19} cm^{-3} and undoped Si layer for all devices simulated. The channel length is 10 nm and channel thickness is varied from 2.2 nm to 3.2 nm in steps of 0.5 nm for studying the variation of DIBL, drain current, threshold voltage transconductance and drain conductance and subthreshold swing with change in thickness of counter-doping (T_c).

III. RESULTS AND DISCUSSION

The DIBL is calculated from the computed values of Ids and Vg for different values of counter-doping thickness and are plotted in Fig. 2. It is observed that as n+ counter-doping thickness increases, DIBL increases slightly. The DIBL value remains almost same when there is increase in p+ counter-doping thickness. Fig. 3

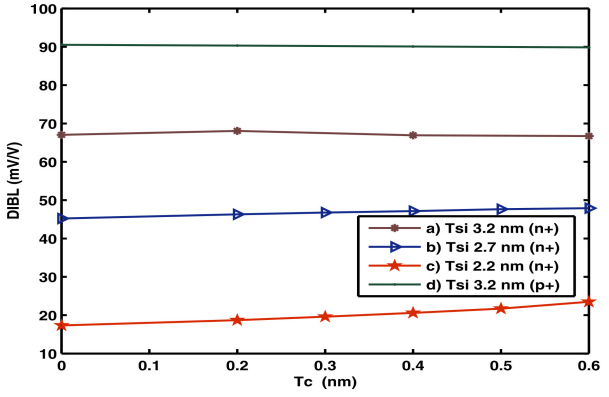

Fig. 2. DIBL as a function of counter-doping thickness for channel thickness (a) 3.2 nm (b) 2.7 nm (c) 2.2 nm (n+ type) and (d) 3.2 nm (p+ type).

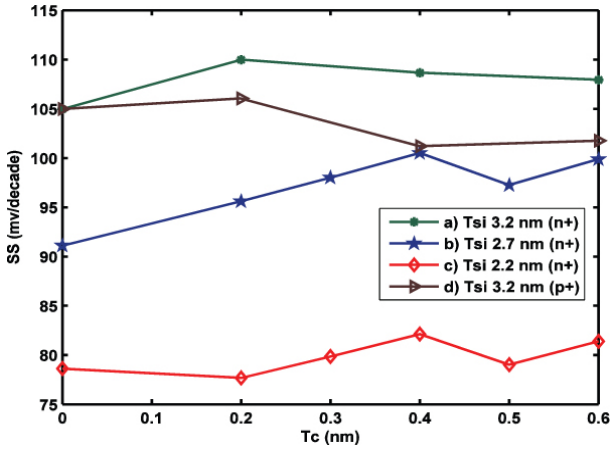

Fig. 3. Subthreshhold swing as a function of counter-doping thickness for channel thickness (a) 3.2 nm (b) 2.7 nm (c) 2.2 nm (n+ type) and (d) 3.2 nm (p+ type).

shows the subthreshold slope as a function of the counter-doping thickness at different (2.2, 2.7 and 3.2 nm) channel thickness. Increase in n type counter-doping thickness of DG MOSFET exhibits slight subthreshold slope degradation. But in the case of p-type counter-doping, the subthreshold slope improves substantially compared to the n-type counterdoping. It is of significant importance to reduce the subthreshold swing, which is a measure of the rate of change in current (I_d) as a function of gate voltage (V_g) in a MOSFET, since a lower subthreshold swing will lower the supply voltage and hence the dissipation. As can be seen from Fig. 4, the n-type counter-doping slightly reduces the threshold voltage.

However, a reduction in the threshold voltage gives rise to an increase in the subthreshold leakage current, which is the current that is conducted through a transistor from its source to drain when the device is intended to be off. Due to this increase in subthreshold current, static power consumption is increased. In contrast, increase in p-type counter-doping thickness improves V_t and the subthreshold slope improves substantially compared to the n type counter-doping thickness. With the n-type counter doping overall performance is degraded due to the large increase in subthreshold leakage current. An increase in threshold voltage is observed if those layers are p-doped, with an accompanying decrease in off state leakage current when compared with an intrinsic channel device (Fig. 4). Increasing the threshold voltage of the DG MOSFET is an effective way to reduce subthreshold leakage.

Transconductance, g_m, is a measure of the sensitivity of drain current to changes in gate-source bias. Our results show that devices with channel thickness as thin as 2.2 nm have high transconductance (38 mS/μm) and relatively small DIBL (20 mV/V), and thus may be suitable for nearly all digital applications. The barrier width is modulated by the application of gate voltage and thus the transconductance of the device is dependent on the gate voltage (Fig. 5). From the Fig. 5, curve a & b represent (p-type) the variation of transconductance of counter doped and undoped channel with gate voltage V_g. The effect of counter doping on drain conductance compared to undoped channel represented in Fig. 5, curve c & d (undoped and p-type counter doped). It is evident from the Fig. 5 transconductance (g_m) and the

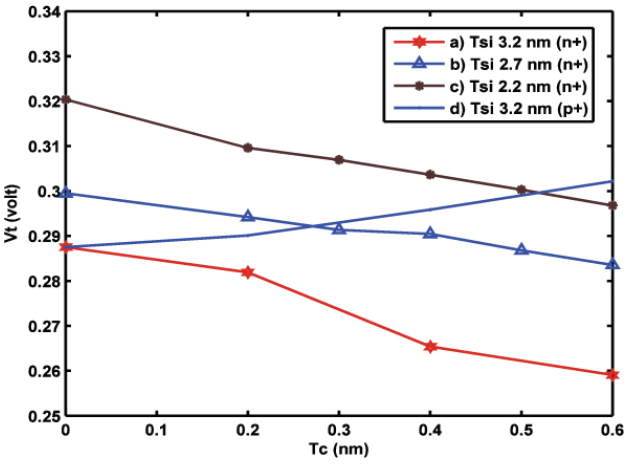

Fig. 4. Threshold voltage as a function of counter-doping thickness for channel thickness (a) 3.2 nm (b) 2.7 nm (c) 2.2 nm (n+ type) and (d) 3.2 nm (p+ type).

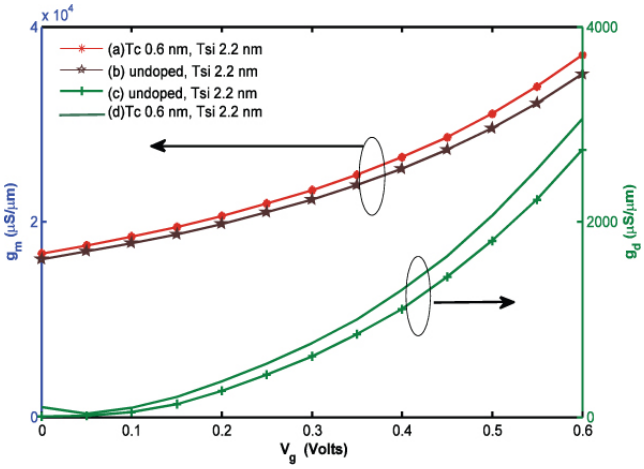

Fig. 5. Transconductance (g_m) and drain conductance (g_d) function of Vg for undoped and counter doped channel, (a) Tc 0.6 nm(p+ type) (b) undoped Tsi 2.2 nm (c) undoped Tsi 2.2 nm and (d) Tc 0.6 nm (p+ type).

drain conductance (g_d) increased due to counter doping thickness (T_c).

IV. CONCLUSIONS

We have investigated the variation of important short channel effects, DIBL and subthreshold swing, in counter-doped DG MOSFETs. Increasing the threshold voltage of the DG MOSFET is an effective way to reduce subthreshold leakage and DIBL. Increase in p-type counter-doping thickness improves Vt, and improves substantially the subthreshold slope compared to the n-type counter-doping thickness. Therefore, counter-doping thickness can be used as an alternative to achieve multiple threshold voltages on a chip. Our results show that devices with channel thickness as thin as 2.2 nm have high transconductance (38 mS/μm) and relatively small DIBL (20 mV/V), and thus may be suitable for nearly all digital applications.

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