A Low Vth SRAM Reducing Mismatch of Cell-Stability with an Elevated Cell Biasing Scheme

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***Abstract*—A lower-threshold-voltage (LVth) SRAM cell with an elevated cell biasing scheme, which enables to reduce the random threshold-voltage (Vth) variation and to alleviate the stability-degradation caused by word-line (WL) and cell power line (VDDM) disturbed accesses in row and column directions, has been proposed. The random Vth variation (σVth) is suppressed by the proposed LVth cell. As a result, the LVth cell reduces the variation of static noise margin (SNM) for the data retention, which enables to maintain a higher SNM over a larger memory size, compared with a conventionally being used higher Vth (HVth) cell. An elevated cell biasing scheme cancels the substantial trade-off relationship between SNM and the write margin (WRTM) in an SRAM cell. Obtained simulation results with a 45-nm CMOS technology model demonstrate that the proposed techniques allow sufficient stability margins to be maintained up to 6σ level with a 0.5-V data retention voltage and a 0.7-V logic bias voltage.**

***Index Terms*—SRAM, stability, static-noise margin, write margin**

I. INTRODUCTION

Demands for lowering the operating voltage Vdd for system LSIs has been growing for the battery-operated applications, such as mobiles. Scaling the minimum operating voltage (Vdd_min) of embedded SRAM is one of the keys to lowering a whole-chip operating voltage for the system LSI.

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However, the scaling pace of Vdd_min for SRAM has been slowed down due to decreasing stability caused by increases in amount of random Vth variation (σVth) with device size scaling. Since all the memory cells embedded in the system LSIs have to guarantee those read/write functionality with sufficient margins of SNM and WRTM, a larger memory size SRAM design requires a lower bit failure probability at a higher z-score. As a result, cell-operating voltage is prone to be increased. Consequently, the level of difficulty of scaling the SRAM cell depends on the required memory size and Vdd_min for the amount of σVth for SRAM transistors.

Fig. 1 shows the Vdd_min of SRAM with a 45-nm CMOS technology depending on the σVth without any stability assist circuit techniques. Since the z-score corresponds to the number of memory bits which has to be guaranteed the stable operation, the bit failure probability has to be reduced more as the guaranteed z-score is larger. The Vdd_min is defined as the voltage at SNM=0 V, and is plotted in each σVth. It can be seen from Fig. 1 that the stability for only 1.75-Mbit (5σ) memory

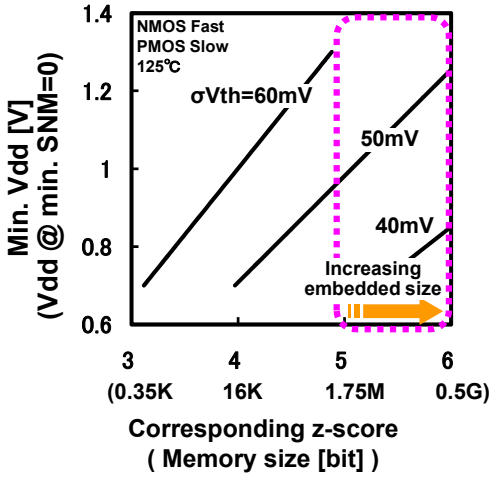


Fig. 1. Vdd_min of SRAM versus z-score corresponding to memory size.

cells is guaranteed with over 50-mV σVth below Vdd=1.0 V. In other words, a higher operating voltage is required to maintain sufficient data retention SNM for all memory cells over larger memory size in a whole chip. The correlation between the z-score and the memory size is shown in Fig. 1. The design target is to maintain the sufficient SRAM margins over the larger memory size from several M-bits to G-bits. The corresponding z-score is over 5 as shown in Fig. 1.

This paper proposes the robust cell design for an embedded SRAM to improve the stability under a larger σVth and to lower the Vdd_min. As the Vth mismatch between the pair transistors in an SRAM memory cell increases at a higher z-score range of the variation, the mismatch of the flip-flop characteristics shown by butterfly curves increases.

In this paper, the Vth random distribution is assumed as Gaussian distribution so that the distribution can be expressed by only two parameters of 1) sigma: σVth and 2) median: μVth. The Vt shift amount at z-point caused by random variation can be expressed by the following equation (1)

$$\delta Vth = +/- \sigma Vth \times z \quad (1)$$

Thus, if z=4σ, μVth=300 mV, and σVth=50 mV, the minimum and maximum Vths at z=4σ are estimated as

Min-Vth= μVth-σVth×4=300 mV-50 mV×4=100 mV

Max-Vth =μVth+σVth×4=300 mV+50 mV×4=500 mV

Fig. 2 shows an example of the decrease in SNM caused by the increase in the random Vth mismatch (4σ mismatch at the half side of the flip-flop). The stability

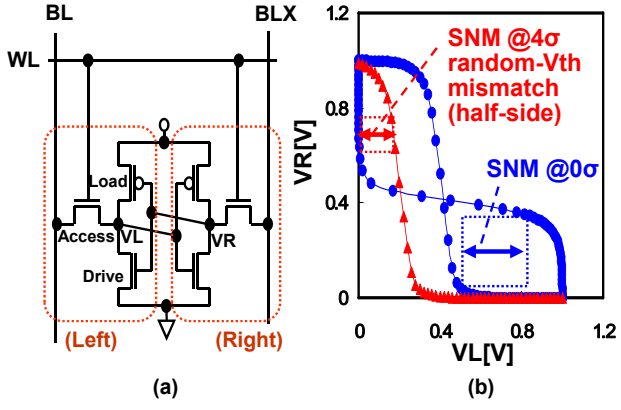


Fig. 2. Increasing mismatch of butterfly-curve at higher z-score of variation range (compared between 0σ and 4σ).

of SRAM cell (SNM), which is defined as the width of the nested square in the smaller side of the eyes, decreases as the asymmetry of the butterfly curve increases at higher z-score (4σ). Reducing this mismatch of the stability is crucial to guarantee the stability in a higher range of z-score which is actually required for a larger scale embedded memory.

Another problem in cell stability is the substantial trade-off relationship between the read and write operating margins. For example, the conventional SRAM has a substantial trade-off problem between WRTM and SNM, because every column under a selected word-line (WL) has to guarantee the disturbed SNM in the half-selected cells even for a write access. Even if the best possible balance between the read and write cell-margins could be achieved to optimize the operating window, the opening eye is closing quickly caused by the increasing device variation and the memory capacity described above.

To address the above issues and lower the bias voltage of the logic and SRAM while maintaining the sufficient stability, a lower-Vth (LVth) cell with an elevated biasing scheme has been proposed by the author [1]. Since Vth and σVth are reduced by decreasing the dopant concentration [2-4], the Vth mismatch in the high z-score range can be reduced by the proposed LVth cell, compared with the commonly-used conventional higher Vth (HVth) cell. The mismatch of the cell-margin characteristics is alleviated with the proposed LVth cell, and the failure probability at an actually-required higher z-score point is reduced. The cell bias voltage is lowered by benefiting from the increased SNM for data-retention, then the leakage power is reduced to the same extent as that of the conventional HVth cell with the higher bias voltage. Furthermore, a disturb-free biasing for the cell and the peripheral logic, which suppresses the levels of WL and bit-line (BL) and controls the cell Vss (VSSM), is proposed. The trade-off relationships between operating margins are cancelled and the peripheral logic-bias voltage is reduced.

This paper is organized as follows. A technique for reducing the mismatch of the cell-margin is demonstrated in Section II. Following the discussion on the trade-off relationships between cell margins, the proposed disturb-free cell biasing is described in Section III. After showing the simulated results of stability over the high z-

score rage in Section IV, the conclusion is given in Section V.

II. Reducing Mismatch of Cell-Margin Characteristics

Lowering the SRAM operating voltage results in the decrease in SNM for the data retention. Reducing the σVth, resulting in a smaller variation of SNM, is one of the key to reduce the bit failure probability at a higher point of z-score at a lower Vdd.

In general, a higher-Vth transistor is employed to increase the mean value μ of SNM even if the variation σ of SNM is increased. Thus, it is true that a higher-Vth transistor decreases the failure probability of SRAM in the range of the lower z-score, that is, in the range of smaller memory capacity. On the other hand, the LVth cell can increase the failure tolerance more than that for HVth in the range of a higher z-score, because lowering Vth with a lower dopant concentration leads to smaller σVth, resulting in a smaller variation of SNM (σSNM).

The σVth is expressed as equation (2), where φ_{bi} is the Fermi level, V_{bs} is the body bias, ε_{Si} is the dielectric constant of silicon, ε_{ox} is the dielectric constant of oxide, q is the unit charge, Na is the doping concentration, Tox is the oxide thickness of MOSFET and Leff and Weff are the length and width of the transistor, respectively [2].

$$\sigma Vth = \frac{\left(2(2\phi_{bi} - V_{bs}) * \varepsilon_{Si} * q^3 * Na\right)^{1/4} * T_{ox}}{\left(L_{eff} * W_{eff}\right)^{1/2} * \varepsilon_{ox}} \qquad (2)$$

The σVth can be reduced by lowering the Na [3]. In this report, the impacts of using LVth transistor on the stabilities in SRAM cell are discussed based on the measured σVth reduction data. The percentage changes in the σVth of a PMOS and an NMOS are 9% and 13%, respectively, with reducing the Vth from 300 mV (HVth) to 150 mV (LVth) as shown in Fig. 3, which are experienced by reducing Na and almost equal to the percentage changes in the σVth for the reference [3].

The parameters for the stability simulation are shown in Table 1. The inter-chip Vth variations and σVth (the dimensions of each cell transistor, and Pelgrom coefficients) are described in this table. The dimensions

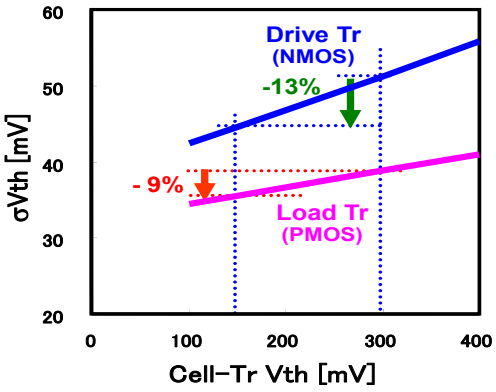


Fig. 3. Correlation between cell-transistor. Vth and σVth.

Table 1. Inter-chip Vth variations, cell-transistor. dimensions and Pelgrom coefficients for stability simulation

		Inter-chip Vth Variations [mV]			Random-Vth Variation Parameters	
		PMOS Typ NMOS Typ	PMOS Slow NMOS Fast (SNM worst)	PMOS Fast NMOS Slow (WRTM worst)	1/SQRT(L*W) [um-1]	Pelgrom Coefficient [mVum]
HVth	Drive (NMOS)	300	142	417	12.7	4.0
	Access (NMOS)	300	161	406	11.3	4.0
	Load (PMOS)	- 300	- 451	-175	19.6	2.0
LVth	Drive (NMOS)	150	31	229	12.7	3.5
	Access (NMOS)	150	35	226	11.3	3.5
	Load (PMOS)	- 150	- 265	-30	19.6	1.8
Junction Temperature		27℃	125℃	-40℃		

of the proposed LVth cell transistors are the same as those of the conventional HVth with 45 nm CMOS technology. For SNM and WRTM simulations, the inter-chip Vth variations are assumed as the worst corners for the SNM and WRTM, that is, PMOS slow and NMOS fast at 125 degree C for SNM and PMOS fast and NMOS slow at -40 degree C for WRTM, respectively. The random Vth variation is also considered by the convolution of the inter-chip Vth variations with its Gaussian distribution of the random Vth variation (σVt) for both of the SNM and WRTM simulation. The simulation tool, the model and model parameter are HSPICE, BISM model version 4.4, and a 45 nm CMOS technology, respectively. The distributions of SNM and WRTM are obtained by using the Monte Carlo simulation.

Using the parameters in Table 1, the Vth sets of the combination of six LVth cell transistors, which lead to the worst SNM and WRTM at 6-σ point, are obtained by using which is generated by Monte Carlo simulation as

shown in Figs. 4(a) and (b), respectively. The operating margins of SRAM cell, SNM and WRTM, depend on the combinations of Vth of the six transistors (Vth-vector). Each Vth position for NMOS pair transistors for drive and access and PMOS one for load transistors are marked by "Right" and "Left". Each Vth is given by the both of inter-chip and the worst random Vth set of 6σ variation. It can be seen that the random-Vth variation for each cell transistor Vth is within 4σ range even assuming that the Vth set for six transistors is generated by the random combination within 6σ range which corresponds to the 500-Mbit memory capacity.

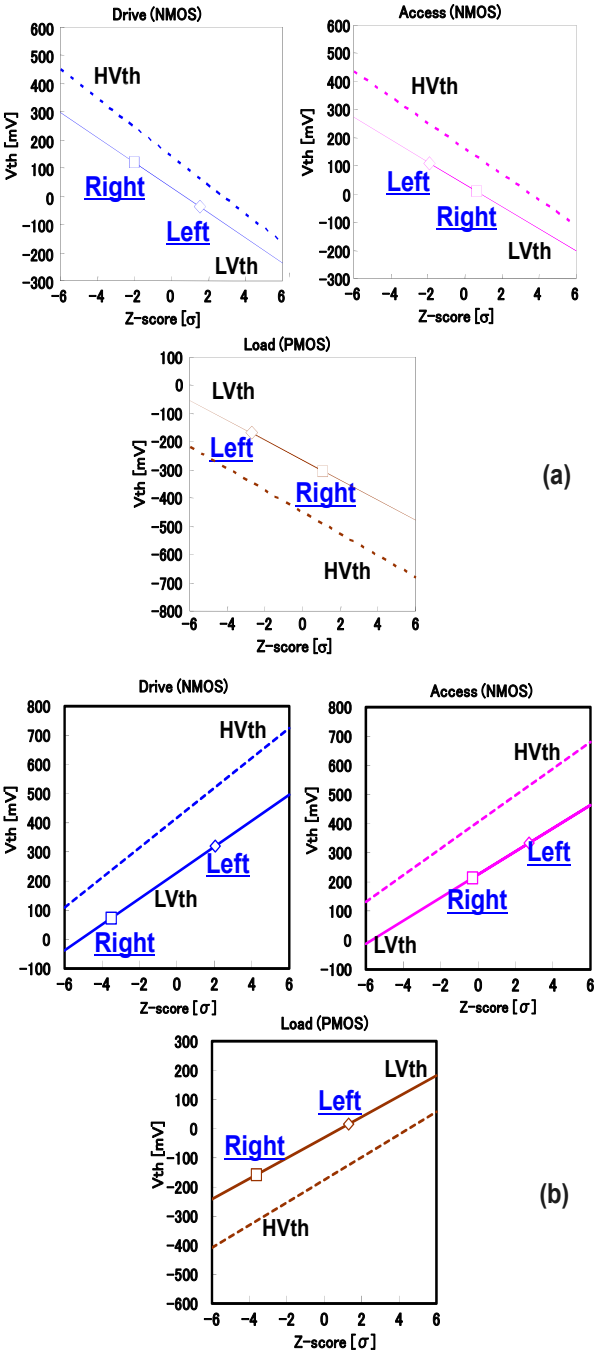


Fig. 4. Vth sets of six cell transistors at 6σ random Vth variation under worst condition (a) for SNM simulation (NMOS fast, PMOS slow, 125℃). and (b) for WRTM simulation (NMOS slow, PMOS fast, -40 ℃).

The asymmetry of butterfly curve is compared in Fig. 5 using the parameters in Table 1. The butterfly curves of HVth cell (Vth=300 mV) and LVth cell (Vth=150 mV) at z-score=0 and 4 are compared. It can be seen that the asymmetry of the butterfly-curve for LVth cell is alleviated compared with HVth cell at z-score of 4σ. This trend means that bit cell failure probability at a larger z-score can be reduced with this proposed LVth transistor because it suppresses the deviation of the cell-margin from the mean value at the larger z-score.

To make clear the dependency of cell stability on z-score, the data retention SNM (WL is inactivated) is compared between each cells, Vth=300 mV and the proposed LVth=150 mV at Vdd=0.5 V and 125 degree C, in Fig. 6. Since the mean value μ of SNM (SNM at z-score=0) of the conventional HVth cell is higher than that of the proposed LVth cell, the conventional HVth cell is suitable for a smaller memory size, that is, for a lower z-score. However, the failure probability for the proposed LVth cell becomes smaller than that for HVth over 3-σ random Vth variation, because σ value of proposed one is smaller than that for the conventional one. The failure probability of the proposed LVth cell is lower than that for HVth cell over the memory size from 3σ (0.35Kbit) to 7σ (390Gbit) as shown in Fig. 6.

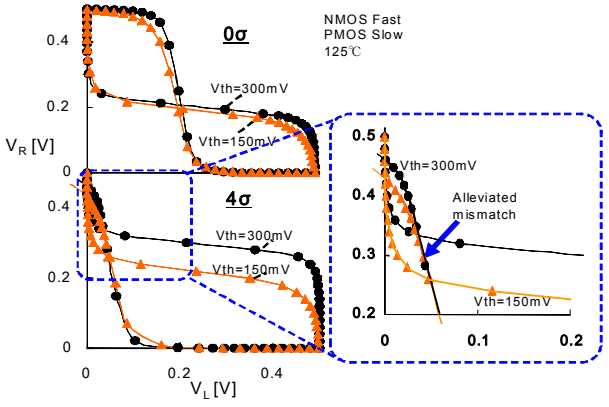


Fig. 5. Comparison of butter-fly curve under 0σ and 4σ random-Vth variation (VDD=0.5 V, 125℃, PMOS slow, NMOS fast). SNM decreases as asymmetry in cell characteristics increases at larger Z-score of σVth.

Retention SNM	Vth=0.30V (Conv.)	Vth=0.15V (Proposed)
μ [mV]	133.8	108.1
σ [mV]	24.7	15.6

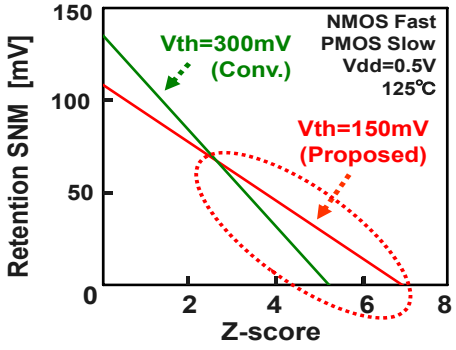


Fig. 6. Comparisons of dependency of retention SNM on z-score between the conventional and proposed one.

III. DISTURB-FREE BIASING SCHEME

1. Various Trade-off Relationships between Cell Operating Margins

Various useful assist techniques to increase the operating margins have been reported so far. However they work effectively only within the limited conditions [5-15]. The WL level is suppressed by a dual-Vdd supply [5-7] or an internal voltage generator [8-10] to assist the SNM at a half-selected cell (Cell B in Fig. 7(a)) in a read and write operation, whereas it results in the decrease in WRTM because the suppressed WL degrades the drivability of the access transistor of the written cell. As for the technique for the write assist, the column-based dynamic cell Vdd (VDDM) [11, 12] or VSSM [13] level control assists the WRTM, whereas it reduces the data-retention SNM in the write-selected column (Cell C in Fig. 7(b)) due to reducing the retention bias voltage. Negatively BL overdriving scheme for the write assist [14] can increase WRTM, whereas its excessively negative BL causes to flip the cell data in the write-selected column. Despite the trade-off relationship between those margins as shown in Table 2, the conventional SRAM design requires the best possible balance to satisfy them all simultaneously. Even if the best possible balance between the read and write cell-margins could be achieved to optimize the operating window, the opening eye is closing quickly caused by the increases in device variation and the memory size.

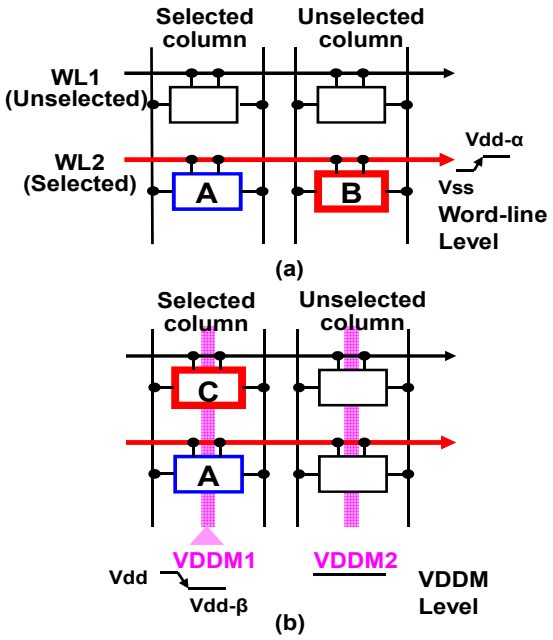


Fig. 7. Margin trade-off relationships of conventional stability assist techniques. (a) Read assist technique [6-11]: WRTM at selected cell (cell A) vs. SNM at half-selected (WL-disturbed) cell (cell B). (b) Write assist technique [3, 4]: WRTM at write-selected cell (cell A) vs. half-selected (VDDM-disturbed) cell (cell C).

Table 2. Trade-off relationship between cell margins with conventional techniques

	Trade-off relationship between cell margins		
	WRTM	SNM (WL disturbed)	SNM (VDDM disturbed)
Suppressed WL for read assist [6-11]	Conflict	OK	-
Suppressed VDDM for write assist [3,4]	OK	-	Conflict
Proposed biasing scheme	*No conflict*		

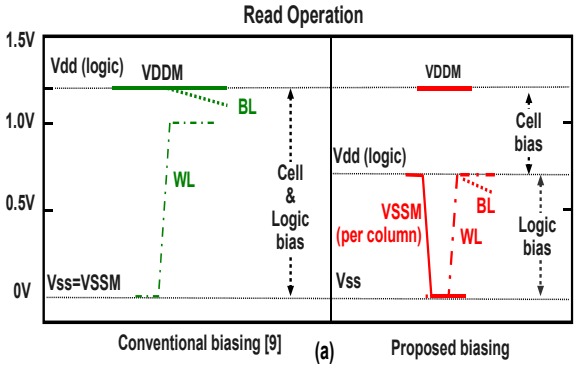
The SNM for the half-selected cell can be improved by suppressing the WL level. However it has only come at the expense of decreasing of the cell current and WRTM [12].

2. Elevated Cell Biasing

A new elevated cell biasing scheme, which alleviates the trade-off relationship of cell margins between a selected cell and a half-selected cell, has been proposed to reduce the failure probability at a larger z-score and suppress the operating voltage (Table 3 and Figs. 8 and 9).

Table 3. Comparisons between proposed biasing and conventional one at unselected cell

		Conventional	Proposed
		Unselected Cell	Unselected Cell
Cell Bias	VDDM	1.2V	1.2V
	VSSM	0V	0.7V
Peripheral Logic Bias	Vdd	1.2V	0.7V
	Vss	0V	0V
Word Line		Vss (0V)	Vss (0V)
Bit Line		Vdd (1.2V)	Vdd (0.7V)



		Conventional		Proposed	
		Selected Cell	Half-Selected Cell (Row direction)	Selected Cell	Half-Selected Cell (Row direction)
Cell Bias	VDDM	1.2V		1.2V	
	VSSM	0V	0V	0V	0.7V
Peripheral Logic Bias	Vdd	1.2V		0.7V	
	Vss	0V		0V	
Word Line		1.2V– α	1.2V– α	VSSM (0.7V)	VSSM (0.7V)
Bit Line		Vdd (1.2V)		Vdd (0.7V)	

(b)

Fig. 8. (a) Comparisons between proposed biasing and conventional one at read operation. (b) Cell biases at selected cell and half-selected cell.

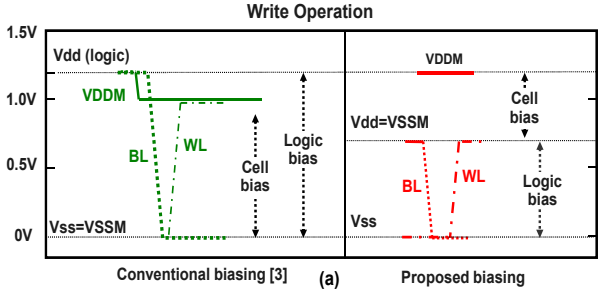
The key concept of the proposed elevated cell biasing is that the potential of storage nodes for "H" and "L" are elevated by 0.7 V while keeping the potential difference of 0.5 V, resulting in the shifts of VDDM and VSSM from 0.5 V to 1.2 V for "H" and 0 V to 0.7 V for "L", respectively. Such potential shifts of the storage nodes allows the conventional voltage swings for WL (0 to 0.7 V) and BL (0.7 V to 0 V) accesses to play the roles of "suppressed WL" and "negatively overdriving BL" compared with the level of the potential of storage node for "L".

These pseudo accesses with "suppressed WL" and "negatively BL overdriving" for written column allow to avoid the conventional read and write margin trade-off accesses, resulting in significantly alleviating the decreases of the stabilities for the WL-disturbed cells in the row direction at read and write operation (cell B in Fig. 7(a)) and VDDM-disturbed cells in the column direction at write operation (cell C in Fig. 7(b)).

This elevated biasing allows increasing data retention SNM as described in Section II. The inactivated-WL level is logic Vss (0 V) below VSSM level (0.7 V) to reduce the BL-leakage current (Table 3). The activated-WL level is generated from the peripheral-logic Vdd.

BL is pre-charged to Vdd level (0.7 V) that is different from the conventional VDDM level (1.2 V) to reduce the peripheral logic bias (Table 3) and it is driven from VSSM (0.7 V) to Vss (0 V) at a write access (Fig. 9), and does not pull-down the VDDM level (1.2 V) as conventional biasing does [11, 12]. VSSM is routed in each column [13] and is driven from VSSM to Vss at a read access (Fig. 8). The activated WL level is VSSM (=0.7 V) same as cell "L" level which is different from the conventional one [6-11] as shown in Figs. 8 and 9.

The cell-array biasing levels for a write and a read operation are shown in Figs. 10 and 11, respectively. The cells A, B, C and D in each figure are a selected cell, a half-selected cell by WL, a half-selected cell by BL and an unselected cell, respectively.



		Conventional		Proposed	
		Selected Cell	Half-Selected Cell (Column direction)	Selected Cell	Half-Selected Cell (Column direction)
Cell Bias	VDDM	1.2V- β	1.2V- β	1.2V	1.2V
	VSSM	0V		0.7V	
Peripheral Logic Bias	Vdd	1.2V		0.7V	
	Vss	0V		0V	
Word Line		1.2V– α	1.2V– α	VSSM (0.7V)	0V
Bit Line		0V / Vdd (1.2V)		0V / Vdd (0.7V)	

(b)

Fig. 9. (a) Comparisons between proposed biasing and conventional one at write operation. (b) Cell biases at selected cell and half-selected cell.

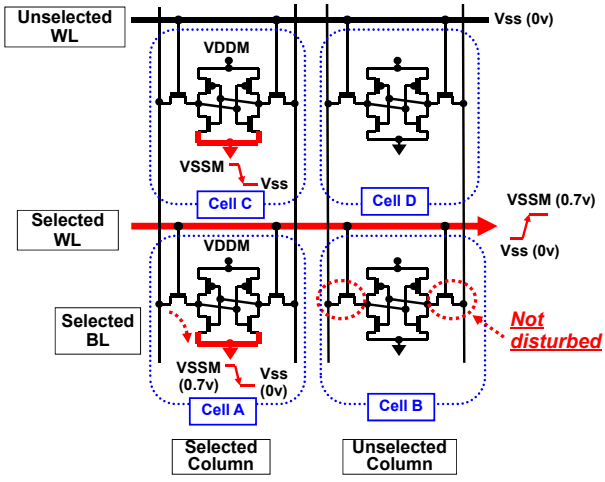


Fig. 10. Cell array biasing at read operation.

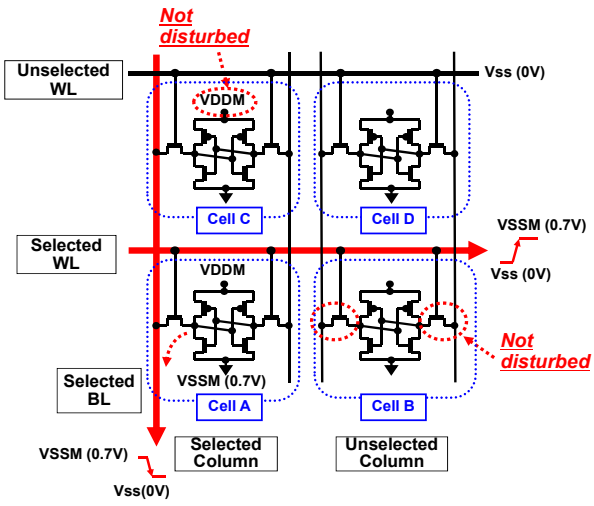


Fig. 11. Cell array biasing at write operation.

A read operation is executed by discharging the drive-transistor source of the selected-column from VSSM to Vss (Fig. 10). The retention SNM at Cell-C increases, and WL does not disturb the half-selected cell (Cell-B) as well as the write operation. As described above, the proposed elevated cell biasing cancels the trade-off relationships between WRTM, the retention SNM and the WL-disturbed SNM.

As shown in Fig. 11, discharging the selected BL during a write operation will not cause the reduction in the retention SNM at an half-selected cell in a write accessed column (Cell-C) as the conventional VDDM control [11, 12] does. This proposed write biasing does not cause a reliability problem due to the excessively applied bias to the cell transistor as the conventional negatively biased BL [14] does, because the BL level swings within the Vdd bias for peripheral logic. Thus, this biasing cancels the trade-off relationships between WRTM (at Cell-A) and the disturbed SNM (at Cell-B), and WRTM (at Cell-A) and the retention SNM (at Cell-C) in the conventional write assist scheme.

The sub-threshold leakage of the flip-flop in a memory cell is suppressed by the reduced cell bias (0.5 V), whereas the Vth is reduced. And the leakage from BL (0.7 V) into the cell is also reduced due to the relatively negative gate to source potential difference (-0.7 V) of the cell access transistor.

The operating current is reduced by lowering the Vdd level (0.7 V) of peripheral logic and BL pre-charge. Moreover the activated WL at VSSM level (0.7 V) does not cause undesirable BL discharge by the half-selected cells.

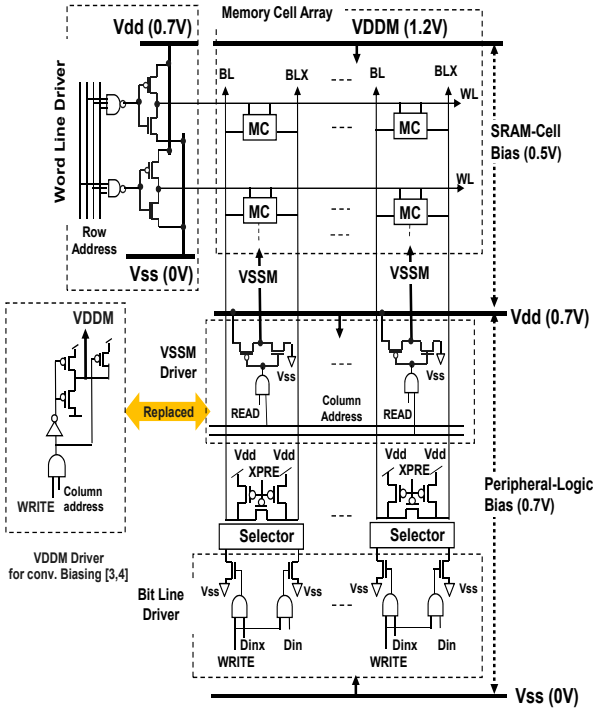


Fig. 12. Block diagram of bias supply to peripheral logic and SRAM cell array.

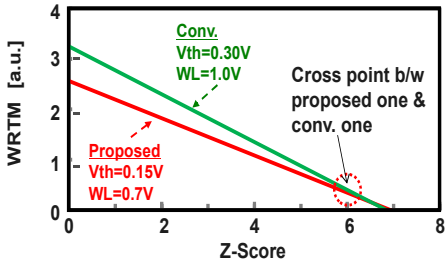
The block diagram of the proposed bias-supplies are shown in Fig. 12. VDDM and Vdd are supplied to the memory cell array and peripheral logic, respectively. VSSM for memory cell array is generated from Vdd of peripheral logic. The routing for VDDM is the same as for the conventional dual-Vdd [5-10]. It is not necessary to change the layout for Vdd and Vss supplies in the peripheral logic. The driver circuits for WL and BL are the same as those for conventional one. This simple biasing scheme without any intermediate or negative

levels does not require any additional level-shifter that causes a significant area penalty for an embedded SRAM module. VSSM is separated column by column in the memory cell array [13], and is driven by each VSSM driver in the peripheral-logic under Vdd supply (Fig. 12). VSSM driver does not cause an area penalty because the column VDDM driver for the conventional biasing [11, 12] can be replaced with this driver.

IV. Evaluation Results

The simulated SNM and WRTM with a 45-nm CMOS technology are demonstrated in Figs. 13-16. The SNM (Figs. 14-16) of the proposed bias scheme and the conventional one were compared under the bias condition characterized by maintaining the same WRTM at 6σ point between the proposed scheme and conventional one (shown in Fig. 13). Activated WL level is 1.0 V at Vdd=1.2 V for the conventional bias and 0.7 V at VDDM=1.2 V for the proposed one, respectively, as shown in Fig. 13.

The parameters related variations for SNM simulation in Figs. 14-16 are shown in Table 4. The inter-chip Vth variation is PMOS slow and NMOS fast at 125 degree C as the worst condition for SNM (same as the condition for SNM simulation in Table 1).



		Conventional	Proposed	Effect of proposed biasing for stability
Cell Bias	VDDM	1.0V	1.2V	Improve SNM at half-selected cell (Column direction)
	VSSM	0V	0.7V	–
Peripheral Logic Bias	Vdd	1.2V	0.7V	–
	Vss	0V	0V	–
Word Line		1.0V	0.7V	–
Bit Line		0V /1.2V	0V / 0.7V	Write without disturb half-selected cell (Column direction)
Inter-chip Vth Variation		Write worst condition in Table 1		
Junction Temperature		- 40℃		

Fig. 13. Comparisons of dependency of Minimum WRTM on z-score and related bias conditions between the conventional and proposed one.

Table 4. Parameters for SMM simulation in Figs. 14-16. Inter-chip Vth variations, cell-transistor dimensions and Pelgrom coefficients

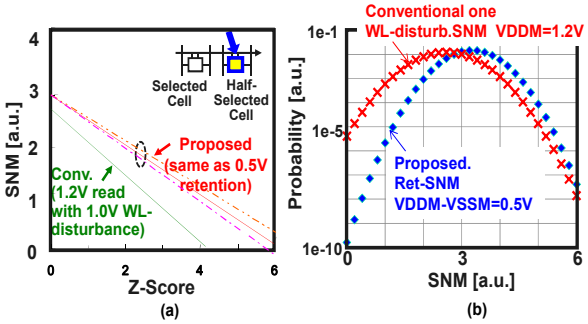
		Inter-chip Vth Variation [mV]	Random-Vth Variation Parameters			
		PMOS Slow NMOS Fast Tj=125℃ (SNM worst)	1/SQRT(L*W) [um-1]	Pelgrom Coefficient [mVum]		
				Typical Case i)	Best Case ii)	Worst Case iii)
LVth	Drive (NMOS)	31	12.7	3.5	3.2	3.8
	Access (NMOS)	35	11.3	3.5	3.2	3.8
	Load (PMOS)	- 265	19.6	1.8	1.7	1.9
HVth	Drive (NMOS)	142	12.7	4.0	—	—
	Access (NMOS)	161	11.3	4.0	—	—
	Load (PMOS)	- 451	19.6	2.0	—	—
Design Target		Z-score > 5σ				

To make clear the effectiveness of the proposed biasing, SNM for LVth cell is simulated under three conditions with different Pelgrom coefficient as follows;

i) The typical case that the percentage changes in σVth reduction between HVth and LVth are 9% and 13 % for PMOS and NMOS, respectively (typical case in Table 4, and solid lines in Figs. 14-16).

ii) An assumed best case that the percentage changes in σVth are 15% and 20% (best case in Table 4, and one-dotted and dashed lines in Figs. 14-16).

iii) An assumed worst case that the percentage changes in σVth are 5% and 7 % (worst case in Table 4, and two-dotted and dashed lines in Figs. 14-16).



		Conv.	Proposed	Effect of proposed biasing for stability
Cell Bias	VDDM	1.2V	1.2V	–
	VSSM	0V	0.7V	Proposed VSSM whose level is same as WL eliminates WL-disturbance
Peripheral Logic Bias	Vdd	1.2V	0.7V	–
	Vss	0V	0V	–
Word Line (WL)		1.0V	0.7V	Eliminate disturbance to half-select cell (Row direction)
Bit Line (BL)		1.2V	0.7V	Eliminate noise from BL into cell

Fig. 14. (a) Comparisons of SNM dependency on z-score at a half-selected (WL-disturbed) cell in an unselected column and related bias conditions and effects between the conventional and proposed one, (b) comparison of SNM distributions between conventional biasing and proposed one.

SNMs for the three cells, which are WL and VDDM disturbed cells in row and column directions and read selected cell (Figs. 10 and 11) were simulated under above three conditions. And the results of the simulation verified that the stability of the proposed biasing with LVth cell met our design target (Fig. 1(b)) as follows.

1. SNM at WL-disturbed half-selected cell in unselected column

At first, Fig. 14 shows SNM for the conventional cells that is degraded by the WL-disturbed accesses for both write and read operations. On the other hand, as shown in Figs. 10 and 11, the proposed elevated cell allows WL disturbed-free cell accesses. This is because the potential level for WL-on (=0.7 V) is same as those for "L" nodes of the unselected cells (=VSSM), making the access transistors for unselected cells hard to turn on. As a result, the SNM for proposed one is almost same as the retention SNM. This leads to elimination of the conventional trade-off between SNM and WRTM due to the WL-disturbed half-selected accesses.

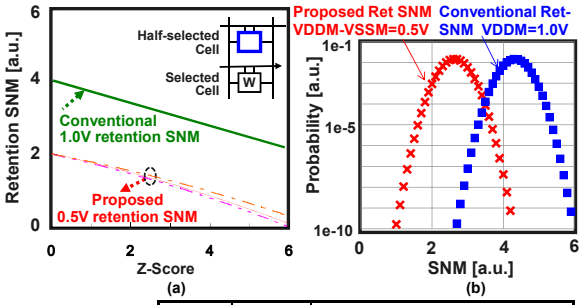
That is the reason why the SNM for proposed biasing (VDDM(1.2 V)-VSSM(0.7 V)=0.5 V, WL=0.7 V) is larger than that for conventional biasing (VDDM=1.2 V, WL=1.0 V). As can be seen from the distribution of SNM in Fig. 14(b), sigma value (σSNM) for the proposed one is smaller than that for WL-disturbed SNM. This is because the Vth mismatch between access and drive transistors gives a strong impact on distribution of WL-disturbed SNM but it does not give an impact on the proposed one at all due to WL-cut-off (WL=0.7 V and VSSM=0.7 V, i.e., Vgs for access transistor is 0 V).

As a result, the proposed biasing scheme maintains sufficient stability (bit-failure tolerance) up to 6σ.

It should be noted that even if the amounts of σVth reduction fluctuates as much as the cases of ii) and iii), the SNM of the proposed biasing is maintained sufficiently high compared with the conventional one. Even under the worst condition of case iii), SNM is higher than that of the conventional one.

2. Retention SNM at half-selected cell in written column

The retention SNM at the unselected cell in the write selected column is compared with the conventional VDDM control for write assist [3, 4], at Vdd=1.2 V and 125 degree C, in Fig. 15. The conventional write assist technique reduces VDDM level from Vdd (1.2 V) to 1.0 V (Fig. 15(b)) that results in the reduction in the data-retention SNM at the unselected cell in the same column as shown in Fig. 7(b). The proposed biasing does not disturb the data retention at an unselected cell because the write operation is executed by lowering the BL level from VSSM (0.7 V) to Vss (0 V), and does not reduce the VDDM level. The SNM for the proposed biasing is the same as the 0.5 V retention SNM discussed in Fig. 14. The retention SNM for proposed biasing keeps higher up to 6σ with the lower cell/logic bias of 0.5 V/0.7 V than that of the conventional one at 1.2 V.

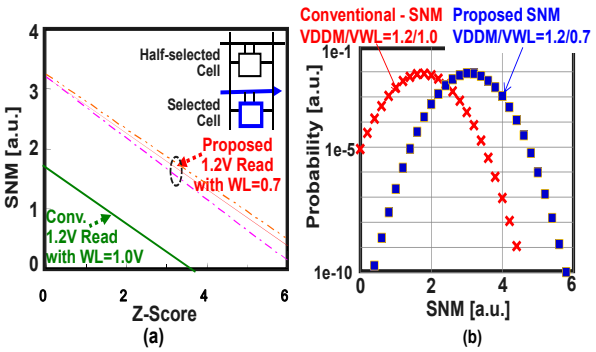


		Conv.	Proposed	Effect of proposed biasing for stability
Cell Bias	VDDM	1.0V	1.2V	Improve SNM at half-selected cell (Column direction)
	VSSM	0V	0.7V	–
Peripheral Logic Bias	Vdd	1.2V	0.7V	–
	Vss	0V	0V	–
Word Line (WL)		1.0V	0.7V	–
Bit Line (BL)		0V / 1.2V	0V / 0.7V	Eliminate disturbance to half-select cell (Column direction)

Fig. 15. (a) Comparisons of retention SNM dependency on z-score at an unselected cell in a write-accessed column and related bias conditions and effects between the conventional and proposed one, (b) comparison of retention SNM distributions between conventional biasing and proposed one.

3. SNM for read cell

Compared with previously proposed suppressed WL technique [5-11], the proposed biasing scheme maintains a larger SNM at the read cell and covered the higher z-score range over 6.5σ, which is much higher than 4σ of conventional scheme as shown in Fig. 16. This is because the elevated cell biasing allows much larger potential difference (=0.5 V for WL-on=0.7 V and "H"=1.2 V) between WL-on (forced to access transistor) and storage node of "H" (forced to drive transistor), compared with that for the conventional one (=0.2 V for



		Conv.	Proposed	Effect of proposed biasing for stability
Cell Bias	VDDM	1.2V	1.2V	–
	VSSM	0V	0V	Read without disturb half-selected cell (Row direction)
Logic Bias for Peripheral	Vdd	1.2V	0.7V	–
	Vss	0V	0V	–
Word Line (WL)		1.0V	0.7V	Suppress noise from BL to cell
Bit Line (BL)		1.2V	0.7V	Reduce noise into cell

Fig. 16. (a) Comparisons of WL-disturbed SNM dependency on z-score at read selected cell and related bias conditions and effects between the conventional and proposed one, (b) comparison of WL-disturbed SNM distributions between conventional and proposed one.

WL-on=1.0 V and "H"=1.2 V). The read operation was executed by the column-based VSSM level control down to Vss (0 V) level.

V. Conclusions

The LVth SRAM cell design combined with the elevated cell biasing reduces the variation of the cell stability margins and alleviates the stability-degradation caused by the WL and VDDM line disturbed accesses, resulting in allowing a larger stability margins to be maintained at a higher z-score range over 3σ random-Vth variation.

The obtained simulated results with a 45-nm CMOS technology demonstrate that the proposed elevated biasing schemes achieve the significantly larger stability margins over 6σ random-Vth variation, compared with the conventional biasing by canceling the cell-margin trade-off relationship between SNM and WRTM.

These proposed techniques allow the operating voltage for system LSIs and the bit failure probability to be lowered at the larger high z-score region, compared with High-Vth SRAMs .

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