A Subthreshold Swing Model for Symmetric Double-Gate (DG) MOSFETs with Vertical Gaussian Doping

Pramod Kumar Tiwari and S. Jit

Abstract—**An analytical subthreshold swing model is presented for symmetric double-gate (DG) MOSFETs with Gaussian doping profile in vertical direction. The model is based on the effective conduction path effect (ECPE) concept of uniformly doped symmetric DG MOSFETs. The effect of channel doping on the subthreshold swing characteristics for non-uniformly doped device has been investigated. The model also includes the effect of various device parameters on the subthreshold swing characteristics of DG MOSFETs. The proposed model has been validated by comparing the analytical results with numerical simulation data obtained by using the commercially available ATLAS™ device simulator. The model is believed to provide a better physical insight and understanding of DG MOSFET devices operating in the subthreshold regime.**

Index Terms—**DG MOSFET, ATLAS simulation, 2D potential, subthreshold swing, effective conduction path effect (ECPE), gaussian doped channel**

I. INTRODUCTION

The conventional MOSFETs show severe short channel effects like drain induced barrier lowering (DIBL) and poor on-off characteristics as the channel length of device goes down in the sub-50 nm range. The Double Gate (DG) MOSFETs are good enough to replace the conventional MOSFETs in this particular regime because of their excellent immunity to the short channel effects, good control of gates on the channel and better on–off characteristics [1-3]. Since scalability and on-off characteristics of DG-MOSFETs are defined by the subthreshold slope of the device, accurate modeling of DG MOSFETs are of great importance for the designing of switching circuits for VLSI and ULSI applications. A number of theoretical models for the subthreshold swing for DG MOSFETs have been proposed for the undoped [4-6] and uniformly doped [7-11] channels. Liang et al. [4] proposed a subthreshold swing model for undoped DG MOSFETs where the effect of doping on the subthreshold characteristics was ignored. The model reported by Hamid et al. [5] included the weak inversion charge which shows the channel length dependency on the subthreshold swing. Recently, Ray et al. [6] proposed a subthreshold swing model based on evanescent mode approach to solve the channel potential including the effect of inversion charge. Both of the models, Hamid et al. [5] and Ray et al. [6], assumed the concept of effective conduction path parameter, d_{eff} [10], to define the path of subthreshold conduction current in the channel. Further, both of them assumed that the inversion charge could appear in the entire channel region just opposite to the doped channel and computed the subthreshold swing parameter S (say) for $d_{eff} = \frac{t_{si}}{4}$ where, t_{si} is the silicon channel thickness. Moldovan et al. [12] and Cerderia et al. [13, 14] suggested that actual devices get generally be doped due to the residual impurities. Further, they had also emphasized that doped channels could provide better control of the threshold voltage (than the undoped devices) without changing the gate material leading to the multi-threshold processes which are of great interests for analog applications [12, 15]. Based on the above

Manuscript received Nov. 22, 2009; revised Jan. 23, 2010.
Centre for Research in Microelectronics (CRME), Department of Electronics Engineering, Institute of Technology, Banaras Hindu University, Varanasi-221005, India
E-mail : sjit.ece@itbhu.ac.in

assumptions, a number of subthreshold swing models [7-11] were also reported for DG MOSFETs with doped channels. Bhattacherjee et al. [7] presented an analytical model to consider only the effect of channel length on the subthreshold swing parameter of DG-MOSFETs with a doped channel. Agrawal et al. [8] reported a model based on the assumption that the effective subthreshold conduction path would be located at Si-SiO_2 interfaces under both the gates as was considered in [16]. On the other hand, Tosaka et al. [9] presented a model based on the assumed location of the subthreshold conduction path at the centre of silicon channel as suggested in Ref. [17]. The model of Tosaka et al. [9] was very simple (only dependent on $\alpha = \frac{L}{\lambda}$ where L is the channel length and λ is the character length) because the effect of channel doping was neglected. The assumptions made by Agrawal et al. [8] and Tosaka et al. [9] are partially true as Chen at al. [10] suggested that the effective conduction path may be anywhere in the channel depending on the magnitude of doping in the channel. In this process, Chen et al. [10] evaluated the effective conduction path effect parameter (d_{eff}) but failed to provide a closed form expression for d_{eff} due to the complexity involved in the evanescent mode analysis to obtain the channel potential in their model. Dey et al. [11] proposed an analytical model for the subthreshold swing of uniformly doped DG-MOSFETs in terms of the charge centroid parameter d_{eff}. The model was used to study the subthreshold characteristics with asymmetry in gate-oxide thickness, gate-material work function and gate voltages. They had developed an approximated closed form expression for the effective conduction path effect parameter (d_{eff}) as a function of the difference in two gate voltages but independent of doping concentration of the uniformly doped channel of DG MOSFETs. It may be mentioned that the actual transistor channel doping profile becomes closer to Gaussian profile in nature due to many ion implantation stages required during the fabrication process [18, 19]. Further, due to the retrograde channel doping in the vertical channel engineering [20], the original implant gets altered after thermal annealing and the annealed profile becomes closer to uniform in the lateral direction and nonuniform in the vertical direction [21]. However, all the reported models discussed above for the subthreshold swing of DG MOSFETs are based on the assumption of a uniformly doped channel. Zhang et al. [21] reported a threshold voltage model for SOI-MOSFETs with a vertical Gaussian doping profile in the channel but they did not consider the subthreshold swing characteristics of the device. Thus, it may be of great interest to many researchers to model the subthreshold swing of the Gaussian doped DG MOSFETs to accurately predict the on-off behaviour of a real DG-MOS device.

In this paper, an attempt has been made to explore the effective conduction path effect concept to model the doping dependent subthreshold swing of symmetric DG-MOSFETs with a Gaussian profile in the vertical direction of the channel as was considered by Zhang et al. [21] for SOI MOSFETs. The effective conduction path parameter (d_{eff}) has been obtained by following the method suggested by Dey et al. [11] for uniformly doped channel. The model results have been compared with simulation results obtained by using the ATLAS^{TM} [22] device simulation software to show the validity of our proposed model.

II. THEORETICAL MODEL

The schematic structure of a symmetric DG-MOSFET used for our model and simulation is shown in Fig. 1 where L, t_{si} and t_{ox} are the gate-length, channel thickness

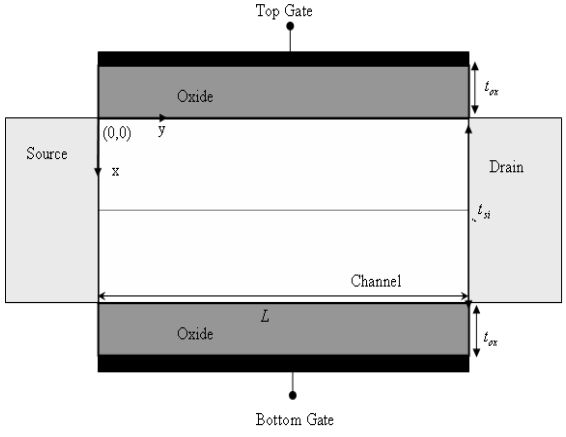

Fig. 1. Schematic diagram of a symmetric DG MOSFET where L, t_{si} and t_{ox} are the channel length, channel thickness and oxide thickness respectively. It is assumed that peak doping is located at the centre of the channel.

and gate-oxide thickness of the device respectively. The doping profile in the vertical direction, *x* of the channel is assumed to be Gaussian function $N_b(x)$ described by Zhang et al. [21] as

$$N_b(x) = N_p \exp\left(-\left(\frac{x-R_p}{\sqrt{2}\sigma_p}\right)^2\right) \tag{1}$$

where, N_p is the doping concentration at the projected range R_p with a straggle σ_p. The *x*- and *y*- axes are considered to be along source-channel interface and channel-upper oxide interface respectively, as shown in the figure.

Let $\psi(x,y)$ be the 2D potential distribution function in the channel. Now, $\psi(x,y)$ can be obtained by solving 2D Poisson's equation

$$\frac{\partial^2\psi(x,y)}{\partial x^2} + \frac{\partial^2\psi(x,y)}{\partial y^2} = \frac{qN_b(x)}{\varepsilon_{si}} \tag{2}$$

with the following boundary conditions [7]:

$$\psi(x,y)\big|_{x=0} = \psi_s(y) \tag{3}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left[V_G - V_{fb} - \psi(0,y)\right] = -\varepsilon_{si}\left.\frac{\partial\psi}{\partial x}\right|_{x=0} \tag{4}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left[V_G - V_{fb} - \psi(t_{si},y)\right] = \varepsilon_{si}\left.\frac{\partial\psi}{\partial x}\right|_{x=t_{si}} \tag{5}$$

$$\psi(x,0) = V_{bi} \tag{6}$$

$$\psi(x,L) = V_{bi} + V_{DS} \tag{7}$$

where ψ_s is the surface potential at $x=0$, and ε_{si} is the permittivity of silicon, ε_{ox} is the permittivity of the gate-oxide SiO_2, V_{bi} is the built-in potential and can be written as $V_{bi} = V_T \ln\frac{N_{DS}N_b(x)}{n_i^2}$ with V_T, N_{DS} and n_i are thermal voltage, source-drain doping and intrinsic silicon doping respectively, $V_{fb} = \phi_M - \left(\chi + \frac{E_g}{2} + V_T \ln\frac{N_b(x=0,t_{si})}{n_i}\right)$ is the flat-band voltage with ϕ_M, χ and E_g are the gate metal work function, electron affinity of silicon and silicon band gap respectively , V_G is the gate-source voltage and V_{DS} is the drain-source voltage.

By introducing a variable τ as $\tau = \frac{x-R_p}{\sqrt{2}\sigma_p}$, Eq. (2) and boundary conditions can be modified as

$$\frac{1}{2\sigma_p^2}\frac{\partial^2\psi(\tau,y)}{\partial\tau^2} + \frac{\partial^2\psi(\tau,y)}{\partial y^2} = \frac{qN_p}{\varepsilon_{si}}\exp(-\tau^2) \tag{8}$$

$$\psi(\tau,y)\big|_{\tau=B} = \psi_s(y) \tag{9}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left[V_G - V_{fb} - \psi(B,y)\right] = -\frac{\varepsilon_{si}}{\sqrt{2}\sigma_p}\left.\frac{\partial\psi}{\partial\tau}\right|_{\tau=B} \tag{10}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left[V_G - V_{fb} - \psi(A,y)\right] = \frac{\varepsilon_{si}}{\sqrt{2}\sigma_p}\left.\frac{\partial\psi}{\partial\tau}\right|_{\tau=A} \tag{11}$$

$$\psi(\tau,0) = V_{bi} \tag{12}$$

$$\psi(\tau,L) = V_{bi} + V_{DS} \tag{13}$$

where

$$A = \frac{t_{si}-R_p}{\sqrt{2}\sigma_p} \quad \text{and} \quad B = \frac{-R_p}{\sqrt{2}\sigma_p} \tag{14}$$

Using the method proposed by Zhang et al. [21], Eq. (8) can be solved by using the boundary conditions described by Eqs. (9)-(13) to obtain the 2D potential function $\psi(\tau,y)$ in the channel which can be written as

$$\psi(\tau,y) = C_1(y) + C_2(y)\,\tau + C_3(y)\times\left[\tau\, erf(\tau) + \frac{\exp(-\tau^2)}{\sqrt{\pi}}\right] \tag{15}$$

where

$$erf(\tau) = \frac{2}{\sqrt{\pi}}\int_0^{\tau}\exp(-t^2)\,dt \tag{16}$$

is the error function of τ and

$$C_1(y) = V_G - V_{fb} + KC_3(y) \tag{17}$$

$$C_2(y) = -PC_3(y) \tag{18}$$

$$C_3(y) = \frac{\left(\psi_s - V_G + V_{fb}\right)}{\left(K - PB + B\, erf(B) + \frac{\exp(-B^2)}{\sqrt{\pi}}\right)} \tag{19}$$

where

$$P=\left\{t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}\sqrt{2}\sigma_p}erf(B)-Berf(B)-\frac{\exp(-B^2)}{\sqrt{\pi}}+Aerf(A)+\frac{\exp(-A^2)}{\sqrt{\pi}}+t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}\sqrt{2}\sigma_p}erf(A)\right\} \times\left(2t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}\sqrt{2}\sigma_p}-B+A\right)^{-1} \quad (20)$$

$$K=P\left(A+t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}\sqrt{2}\sigma_p}\right)-A\,erf(A)-\frac{\exp(-A^2)}{\sqrt{\pi}}-t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}\sqrt{2}\sigma_p}erf(A) \quad (21)$$

Note that the Poisson's equation (i.e. Eq. (8)) at the upper Si-SiO_2 interface can be written as

$$\frac{1}{2\sigma_p^2}\frac{\partial^2\psi(\tau,y)}{\partial\tau^2}\bigg|_{\tau=B}+\frac{\partial^2\psi(\tau,y)}{\partial y^2}\bigg|_{\tau=B}=\frac{qN_p}{\varepsilon_{si}}\exp(-\tau^2)\bigg|_{\tau=B} \quad (22)$$

With the help of Eqs. (15), (17) and (18), Eq. (22) can be modified as

$$\frac{\partial^2\psi_s}{\partial y^2}+\frac{V_G-V_{fb}-\psi_s}{\lambda^2}=\frac{qN_p}{\varepsilon_{si}}\exp(-B^2) \quad (23)$$

where

$$\lambda=\sqrt{\pi}\sigma_p^2\left(\frac{PB-K-Berf(B)-\frac{\exp(-B^2)}{\sqrt{\pi}}}{\exp(-B^2)}\right) \quad (24)$$

is the so called characteristic length associated with the surface potential ψ_s. Equation (23) can be solved to obtain $\psi_s(y)$ as

$$\psi_s(y)=k_1\exp\left(\frac{y}{\lambda}\right)+k_2\exp\left(-\frac{y}{\lambda}\right)+V_G-V_{fb}-\lambda^2\frac{qN_p}{2\varepsilon_{si}}\exp(-B^2) \quad (25)$$

where k_1 and k_2 are two arbitrary constants determined by using Eqs. (12)-(13) and can be expressed in compact forms as

$$k_1=D-\left(\frac{\exp(-\alpha)-1}{\exp(-\alpha)-\exp(\alpha)}\right)V_G \quad (26)$$

$$k_2=E-\left(\frac{\exp(\alpha)-1}{\exp(\alpha)-\exp(-\alpha)}\right)V_G \quad (27)$$

where

$$\alpha=\frac{L}{\lambda} \quad (28)$$

$$D=\left(\frac{\left(V_{bis}+V_{fb}+\lambda^2\frac{qN_p}{2\varepsilon_{si}}\exp(-B^2)\right)(\exp(-\alpha)-1)-V_{DS}}{\exp(-\alpha)-\exp(\alpha)}\right) \quad (29)$$

$$E=\left(\frac{\left(V_{bis}+V_{fb}+\lambda^2\frac{qN_p}{2\varepsilon_{si}}\exp(-B^2)\right)(\exp(\alpha)-1)-V_{DS}}{\exp(\alpha)-\exp(-\alpha)}\right) \quad (30)$$

where, $V_{bis}=V_T\ln\left(\frac{N_{DS}N_b(x=0,t_{si})}{n_i^2}\right)$ is the value of the built in voltage on the channel surfaces.

Using Eqs. (17), (18), (19) and (25), in Eq. (15), the 2D potential function in the channel can be written as

$$\psi(\tau,y)=V_G-V_{fb}+\left(K-P\tau+\tau\,erf(\tau)+\frac{\exp(-\tau^2)}{\sqrt{\pi}}\right)\left(\frac{(\psi_s(y)-V_G+V_{fb})}{K-PB+Berf(B)+\frac{\exp(-B^2)}{\sqrt{\pi}}}\right) \quad (31)$$

Suppose that $\psi_{s\min}=\psi_s(y_{s\min})$ represents the minimum value of $\psi_s(y)$ at $y=y_{s\min}$. The distance $y_{s\min}$ can be obtained by solving $\frac{d\psi_s(y)}{dy}\Big|_{y=y_{s\min}}=0$ which gives

$$y_{s\min}=\sqrt{\frac{\lambda}{8}}\ln\left(\frac{k_2}{k_1}\right) \quad (32)$$

Using Eq. (32) in Eq. (25), $\psi_{s\min}$ can be written as

$$\psi_{s\min}=2\sqrt{k_1k_2}+V_G-V_{fb}-\lambda^2\frac{qN_p}{2\varepsilon_{si}}\exp(-B^2) \quad (33)$$

At any arbitrary position *x* along the transverse direction of the channel (i.e. for any arbitrary value τ), the minimum channel potential, $\psi_{vcm}(\tau)=\psi(\tau,y_{s\min})$ obtained by replacing $\psi_s(y)$ by the $\psi_{s\min}$ in Eq. (31) can be expressed as

$$\psi_{vcm} = V_G - V_{fb} + \left(K - P\tau + \tau\, erf(\tau) + \frac{\exp(-\tau^2)}{\sqrt{\pi}} \right) \times \left(\frac{\psi_{s\min} - V_G + V_{fb}}{K - PB + Berf(B) + \frac{\exp(-B^2)}{\sqrt{\pi}}} \right) \quad (34)$$

Using the concept of the virtual cathode [10] located along the x-direction at $y = y_{s\min}$, the free carrier concentration at the cathode can be given by [10]

$$n_m(\tau) = \frac{n_i^2}{N_p} \exp\left(\frac{\psi_{vcm}(\tau)}{V_T} \right) \quad (35)$$

Since the drain current in the subthreshold regime of operation of a DG MOSFET is proportional to the free carrier concentration at the virtual cathode, the subthreshold swing (say, S) can be written as

$$S = \left(\frac{\partial \log I_D}{\partial V_G} \right)^{-1} = \ln 10 \left(\frac{\partial \ln I_D}{\partial V_G} \right)^{-1} = \frac{kT}{q} \ln 10 \left[\frac{\partial \psi_{vcm}(\tau)}{\partial V_G} \right]^{-1} \quad (36)$$

From Eq. (34), we can write

$$\frac{\partial \psi_{vcm}}{\partial V_G} = 1 - \frac{\left(K - P\tau + \tau\, erf(\tau) + \exp(-\tau^2)/\sqrt{\pi} \right)}{\left(K - PB + Berf(B) + \exp(-B^2)/\sqrt{\pi} \right)} M \quad (37)$$

where

$$M = \frac{1}{\sqrt{k_1 k_2}} \left(\frac{k_1 \exp(\alpha) - k_2 \exp(-\alpha) + k_2 - k_1}{\exp(\alpha) - \exp(-\alpha)} \right) \quad (38)$$

From Eqs. (36)-(38), the subthreshold swing S can now be expressed as

$$S = \frac{kT}{q} \ln 10 \left(1 - \frac{\left(K - P\tau + \tau\, erf(\tau) + \frac{\exp(-\tau^2)}{\sqrt{\pi}} \right)}{\left(K - PB + Berf(B) + \frac{\exp(-B^2)}{\sqrt{\pi}} \right)} M \right)^{-1} \quad (39)$$

Note that the value of subthreshold swing, S, described by Eq. (39) is a function of the variable $\tau = \frac{x - R_p}{\sqrt{2}\sigma_p}$. Since, S is a device parameter, it must be independent of τ. If we assume that the peak of the doping profile is located at the centre of the channel (i.e. $R_p = \frac{t_{si}}{2}$), the device shown in Fig.1 will represent a symmetric DG-MOSFET device. We can thus use the concept of the doping dependent effective conduction path effect as in [10] to describe the resultant punch-through current path in the channel at $\tau = \tau_{eff}$, where τ_{eff} can be written as [10]

$$\tau_{eff} = \frac{\int_B^C \tau \exp\left(\frac{\psi_{vcm}(\tau)}{V_T} \right) d\tau}{\int_B^C \exp\left(\frac{\psi_{vcm}(\tau)}{V_T} \right) d\tau} \quad (40)$$

where

$$C = \frac{(t_{si}/2) - R_p}{\sqrt{2}\sigma_p} \quad (41)$$

It may be noted that Eq. (40) does not give any closed form expression for τ_{eff} and hence a suitable numerical method may be used for the same. However, we can obtain an approximate analytical expression for τ_{eff} from Eq. (40) as follows:

The channel in the vertical direction can be divided into two equal regions namely the front-gate and back-gate regions corresponding to $0 \le x < \frac{t_{si}}{2}$ (i.e. $B < \tau < C$) and $\frac{t_{si}}{2} \le x < t_{si}$ (i.e. $C < \tau < A$) respectively. Since, the model deals with a symmetric DG MOS structure, it may be quite reasonable to assume that each of the regions contribute equal amount of current to the resultant drain current of the device. Now, using the linear approximation model for $\psi_{vcm}(\tau)$ in $B < \tau < C$ as considered in [11], we can approximate $\psi_{vcm}(\tau)$ as a linearly varying function from $\psi_{vcm}^f = \psi_{vcm}(\tau = B)$ to $\psi_{vcm}^m = \psi_{vcm}(\tau = C)$. Thus, Eq. (40) can be approximately written as

$$\tau_{eff} \approx \frac{\int_B^C \tau \exp\left(\frac{E_n\tau - E_nB + \psi_{vcm}^f}{V_T}\right) d\tau}{\int_B^C \exp\left(\frac{E_n\tau - E_nB + \psi_{vcm}^f}{V_T}\right) d\tau} \quad (42)$$

where

$$E_n = \frac{\psi_{vcm}^m - \psi_{vcm}^f}{C - B} \quad (43)$$

Eq. (42) can be solved to obtain an approximate expression for τ_{eff} as

$$\tau_{eff} \approx \frac{\exp\left(\frac{\psi_{vcm}^m}{V_T}\right)\left(\frac{CV_T}{E_n} - \left(\frac{V_T}{E_n}\right)^2\right) - \exp\left(\frac{\psi_{vcm}^f}{V_t}\right)\left(\frac{BV_T}{E_n} - \left(\frac{V_T}{E_n}\right)^2\right)}{\frac{V_T}{E_n}\left(\exp\left(\frac{\psi_{vcm}^m}{V_T}\right) - \exp\left(\frac{\psi_{vcm}^f}{V_T}\right)\right)} \quad (44)$$

It may be mentioned that Eq. (44) gives reasonably good matching with the numerical results for the peak doping up to the value of $10^{19}\,\mathrm{cm}^{-3}$.

Clearly, if $x = d_{eff}$ represents the location of effective subthreshold conduction path in the channel, we can then write,

$$d_{eff} = \left(\sqrt{2}\sigma_p\right)\tau_{eff} + R_p \quad (45)$$

where τ_{eff} can be computed from Eq. (44).

Substituting the τ_{eff} in place of τ in Eq. (39) will give the final expression for the subthreshold swing as

$$S = \frac{kT}{q}\ln 10\left(1 - \frac{\left(K - P\tau_{eff} + \tau_{eff}\, erf(\tau_{eff}) + \frac{\exp(-\tau_{eff}^2)}{\sqrt{\pi}}\right)}{\left(K - PB + B\, erf(B) + \frac{\exp(-B^2)}{\sqrt{\pi}}\right)} M\right)^{-1} \quad (46)$$

where $erf(\tau_{eff})$ is the error function to be computed from Eq. (16) for $\tau = \tau_{eff}$.

Note that the error function $erf(\tau_{eff})$ is a non-analytical function of τ_{eff} and hence the model for the subthreshold swing, S, described by Eq. (46) is not a fully analytical one. However, S can be expressed by an approximate analytical form by approximating the error function in Eq. (46) as [23]

$$erf(\tau_{eff}) = \pm\sqrt{1 - \exp\left(-\frac{\tau_{eff}^2\left(1.27 + 0.14\,\tau_{eff}^2\right)}{1 + 0.14\,\tau_{eff}^2}\right)} \quad (47)$$

where plus and minus signs are used for $\tau_{eff} > 0$ and $\tau_{eff} < 0$ respectively.

III. Outline of the ATLAS™ Simulation

The commercially available ATLAS™ [22] device simulation software has been used to obtain the simulation results for the validation of our proposed model. The ATLAS software solves numerically the 2D Poisson's equation. Among the drift-diffusion model (DD), hydrodynamic (HD) model and energy balance (EB) model available in the ATLAS library, the drift-diffusion (DD) model has been used because of its validity in the subthreshold regime even for channel length less than 30 nm [24, 25] and simple implementation. Recently, Granzner et al. [26] have demonstrated excellent agreement between DD and Monte-Carlo simulation results of I_D vs. V_G characteristics (both for on current and subthreshold current) in DG MOSFETs with $L > 10$ nm by using a suitable modification of *beta* and *vsat.n* parameters in the Caughey-Thomas parallel high field mobility model implemented in ATLAS [22]. Following [26], Jankovic et al. [27] have modified ATLAS default model parameter *beta* and *vsat.n* by setting *beta*=1 and $vsat.n = \frac{1.5L + 21.6}{L + 2.7} \times 10^7$ cm/s (where L is in nanometer). Similar modifications in the mobility model have been applied to simulate the DG MOSFET device.

We have employed the Fermi-Dirac carrier statistics and standard recombination models for the simulation of our DG MOS structure. The Quantum Mechanical (QM)

effects have negligible effect on the subthreshold swing characteristics of DG-MOSFETs with channel thickness more than 3 nm [5, 28]. Since, our study is limited to channel thickness $t_{si} \geq 10\ nm$, the QM effects have been neglected for the simplification of the present model. The device has been simulated by assuming tungsten (with work function $\Phi_m = 4.7$ V) as the gate-electrode and $N_{DS} = 10^{20}$ cm^{-3} as the doping concentration of the source and drain regions.

IV. RESULTS AND DISCUSSIONS

This section presents some theoretical and simulated results for the symmetric DG MOSFET structure with a vertical Gaussian doping profile for which the peak concentration N_p is assumed to be located at the center of the channel. ATLAS™ device simulation software has been used to obtain the simulation results for the validation of our proposed model. The dependence of the effective conduction path parameter (d_{eff}) on the peak concentration N_p has been shown in Fig. 2 for different gate lengths. For the validity of the expression for τ_{eff} described by Eq. (44), the actual and approximated values of d_{eff} computed by using the actual and approximated values of τ_{eff} which are obtained by the numerical integration of Eq. (40) and using Eq. (44) respectively, are compared and shown in the inset of Fig. 2. The parameter values used for comparison are: L = 45 nm, t_{ox} = 1.5 nm, t_{si} = 8 nm, V_G = 0.1 V V_{DS} = 0.1 V, R_p = 6 nm and σ_p = 8 nm. The Simpson's 3/8 Rule has been used in MATLAB to determine τ_{eff} from Eq. (40) and hence d_{eff} from Eq. (45). It is observed that a good matching is found below the doping value of 10^{19} cm^{-3}. It is also observed from Fig. 2 that for smaller values of N_p (<10^{18} cm^{-3}), the value of d_{eff} becomes much closer to the centre of the channel which implies that the center potential is higher than the surface potential and charge carrier responsible for subthreshold conduction mainly flows through the centre of the device. However, as N_p

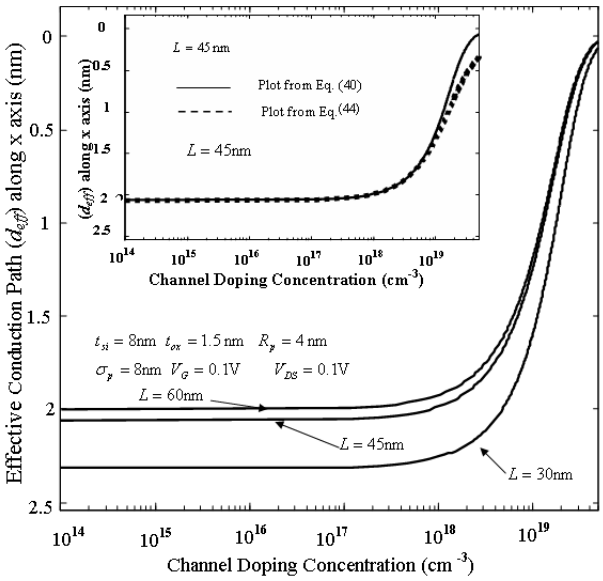

Fig. 2. Demonstration of effective conduction path, d_{eff} with peak channel doping (N_p) for a DG MOSFET for three different channel lengths devices having channel thickness t_{si} = 8nm and gate oxide thickness t_{ox} = 1.5 nm. Inset of the Figure shows the comparison of Eq. (40) and Eq. (44).

increases further, the surface potential becomes much larger near the surface than that of other positions along the transverse direction of the channel and hence the overall conduction becomes highly confined to Si/SiO_2 interfaces. This validates the assumption of surface conduction in conventional long channel MOS devices. Fig. 3 shows the dependence of the subthreshold swing

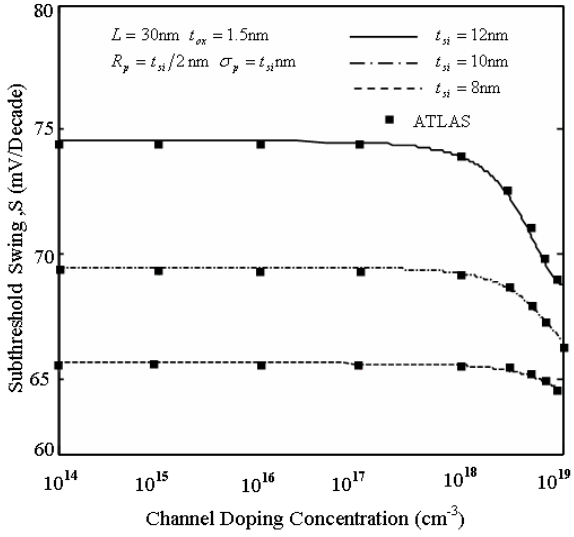

Fig. 3. Demonstration of subthreshold swing, S variation against the peak channel doping (N_p) for the three different values of channel thickness (t_{si}) and V_{DS} = 0.1 V.

parameter, S, on the peak doping concentration N_p for different values of channel thickness. Comparing Figs. 2 and 3, we may observe that N_p can modify the switching characteristics of a symmetric DG-MOSFET device by controlling both the position of the effective conduction path in the channel and subthreshold swing of the device. It may also be observed from the figure that the subthreshold swing, S, is almost constant for $N_p < 10^{18}$ cm^{-3} and S is increased with N_p for higher values implying an improved subthreshold characteristics of the device. The figure further shows that the channel thickness of the device can also play an important role in controlling the subthreshold swing parameter. As the channel thickness goes down from 12 nm to 8 nm with all other parameters remaining unchanged, the value of the subthreshold swing goes down significantly. A good agreement is observed between the model results and ATLAS simulation results. Fig. 4 shows the variation of subthreshold swing parameter with the peak channel doping N_p for different channel lengths with fixed t_{ox} = 1.5 nm and t_{si} = 1.2 nm. It shows that for fixed values of t_{si} and t_{ox}, S is decreasing with increasing L but becomes almost insensitive to N_p for larger channel lengths. It can be justified by the smaller variations in the position of effective conduction path parameter (d_{eff}) for the larger channel lengths of the device as was shown in Fig. 2.

The variation of subthreshold swing parameter S as a function of the channel length L for different channel thicknesses (t_{si}) is shown in Fig. 5. The parameter S is found to be increased with the shrinkage of channel length resulting in the poor switching characteristics of the device. However, for a fixed gate-length, the switching characteristics are observed to be improved with decreasing values of channel thickness. Since, the gate will be in better position to control it for smaller channel thickness, the above results seem to be well justified. Finally, the variation of subthreshold swing with the channel length is shown in Fig. 6 but for different oxide thicknesses. The results of Fig. 6 suggest that thinner gate oxides are required to get better subthreshold characteristics.

The model results shown in Figs. 3-6 are also compared with the ATLAS^{TM} simulation data. A reasonably good matching between the theory and simulation shows the validity of our proposed model.

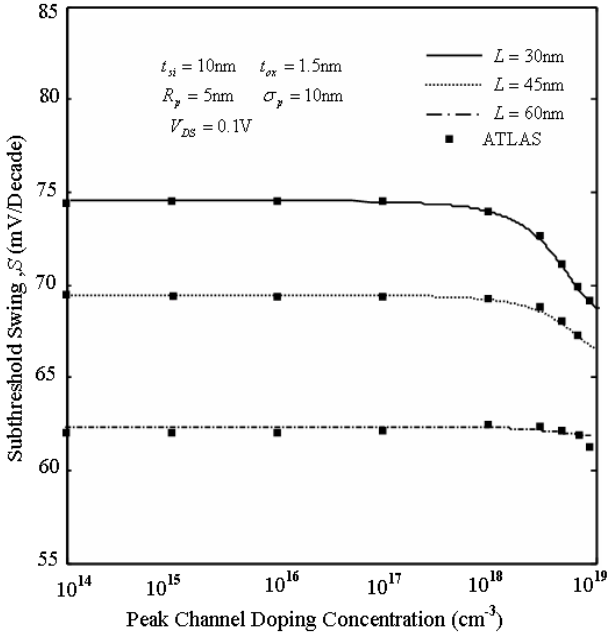

Fig. 4. Variation of subthreshold swing (S) with peak channel doping (N_p) for three different values of device channel lengths L = 30 nm, 45 nm and 60 nm.

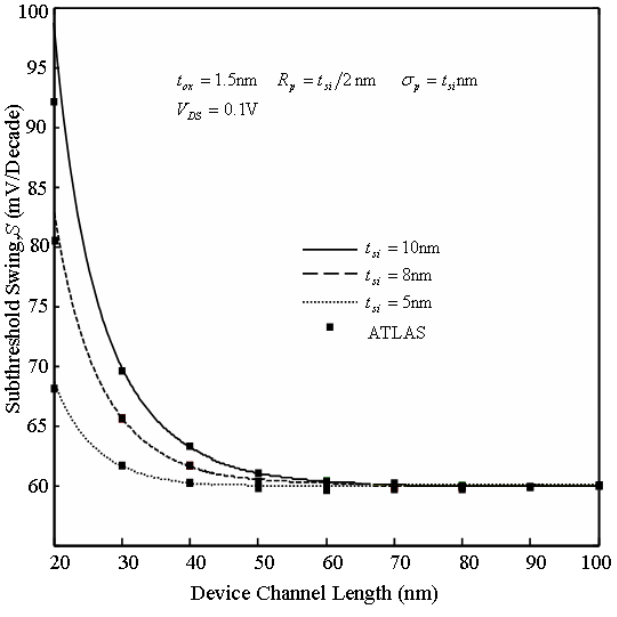

Fig. 5. Depiction of S with the channel lengths L for three different values of silicon channel thickness (t_{si}). The peak channel doping is taken as N_P = 10^{16} cm^{-3}.

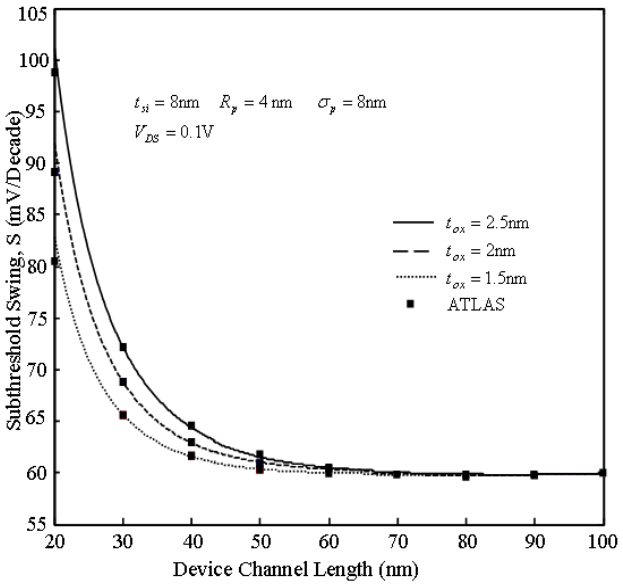

Fig. 6. The subthreshold swing S with the channel lengths L for three different gate oxide thicknesses (t_{ox}). The peak channel doping is taken as $N_P = 10^{16}$ cm^{-3}.

V. CONCLUSIONS

In this paper, a subthreshold swing model for Gaussian doped symmetric DG MOSFETs is presented. The model is based on the effective subthreshold conduction effect phenomenon in DG MOS devices. The effect of doping and various device parameters on the subthreshold swing S are examined in this paper. It is observed that punch-through current path is dependent on the doping concentrations of the channel. The current conduction path is observed to be confined near the center of the channel for lower doping concentration and the path is confined near the channel-oxide interface for considerably higher doping concentrations in the channel. Although, the model is developed for a symmetric DG MOS structure, it can also be extended to asymmetric structures for different values of R_p with incorporating suitable modifications in the model.

REFERENCES

[1] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance," *Electron Device Letters, IEEE*, vol. 8, Issue 9, 1987, pp. 410-412.

[2] L. Huaxin and Y. Taur, "An analytic potential model for symmetric and asymmetric DG MOSFETs," *Electron Devices, IEEE Transactions on.*, vol. 53, Issue 5, 2006, pp. 1161-1168.

[3] T. Tanaka, K. Suzuki, H Horie and T. Sugii, "Ultrafast operation of V_{th} adjusted p^+-n^+ double-gate SOI MOSFET's", *Electron Device Letters, IEEE*, vol.15, Issue 10, 1994, pp.386-388.

[4] X. Liang and Y. Taur, "A 2-D analytical solution for SCEs in DG MOSFETs", *Electron Devices, IEEE Transactions on*, vol. 51, Issue 9, 2004, pp. 1385-1391.

[5] H. A. E. Hamid, J. R. Guitart and B. Iniguez, "Two-Dimensional Analytical Threshold Voltage and Subthreshold Swing Models of Undoped Symmetric Double-Gate MOSFETs", *Electron Devices, IEEE Transactions on,* vol.54, Issue 6, 2007, pp. 1402-1408.

[6] B. Ray and S. Mahapatra, "Modeling of Channel Potential and Subthreshold Slope of Symmetric Double-Gate Transistor", *Electron Devices, IEEE Transactions on*, vol. 56, Issue 2, 2009, pp. 260-66.

[7] S. Bhattacherjee and A. Biswas, "Modeling of threshold voltage and subthreshold slope of nanoscale DG MOSFETs." *Semiconductor Science and Technology*; vol.23, Issue 1, 2008, pp. 015010(8).

[8] B. Agrawal, "Comparative scaling opportunities of MOSFET structures of giga scale integration (GSI)",. *Ph.D Thesis*: Rensselare polytech. Inst. 1994, Troy, NY.

[9] Y. Tosaka, K Suzuki and T Sugii, "Scaling-parameter-dependent model for subthreshold swing S in double-gate SOI MOSFET's", *Electron Devices, IEEE Transactions on*, vol.15, Issue 11, 1994, pp. 466-68.

[10] Q. Chen, B. Agrawal and J. D. Meindl, "A comprehensive analytical subthreshold swing (S) model for double-gate MOSFETs. *Electron Devices, IEEE Transactions on,* vol. 49, Issue 6, 2002, pp. 1086-90.

[11] A. Dey, A. Chakravorty, V. DasGupta and A. DasGupta; "Analytical Model of Subthreshold Current and Slope for Asymmetric 4-T and 3-T Double-Gate MOSFETs", *Electron Devices, IEEE Transactions on,* vol. 55, Issue12, 2008, pp.3442-49.

[12] O. Moldovan, A. Cerdeira, D. Jiménez, J. P. Raskin, V. Kilchytska, D. Flandre, N. Collaert and B. Iñiguez, "Compact model for highly-doped double-gate SOI MOSFETs targeting base band analog applications", *Solid-State Electronic*, vol. 51, Issue 5, 2007, pp. 655-661.

[13] A. Cerdeira, B. Iñiguez and M. Estrada, "Compact model for short channel symmetric doped double-gate MOSFETs", *Solid-State Electronic*; vol.52; Issue7, 2008, 1064-70.

[14] A. Cerdeira, O. Moldovan, B. Iñiguez and M. Estrada, "Modeling of potentials and threshold voltage for symmetric doped double-gate MOSFETs"; *Solid-State Electronic*, vol. 52, Issue 5, 2008, pp. 830-37.

[15] J. P. Raskin, C. T. Ming, V. Kilchytska , D. Lederer and D. Flandre, "Analog/RF performance of multiple gate SOI devices: wideband simulations and characterization", *Electron Devices, IEEE Transactions on,* vol.53, Issue 5, 2006, pp. 1088-95.

[16] R H. Yan, A. Ourmazd and K. F. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk" *Electron Devices, IEEE Transactions on,* vol.39, Issue7, 1992, pp. 1704-10.

[17] K. Suzuki , T. Tanaka, Y. Tosaka, H. Horie and Y. Arimoto, "Scaling theory for double-gate SOI MOSFET's", *Electron Devices, IEEE Transactions on,* vol. 40, Issue 12, 1993; pp. 2326-29.

[18] K. Suzuki , Y Kataoka , S Nagayama, C.W. Magee, T.H Buyuklimanli and T. Nagayama, "Analytical Model for Redistribution Profile of Ion-Implanted Impurities During Solid-Phase Epitaxy," *Electron Devices, IEEE Transactions on*, vol. 54, Issue.2, 2007;pp. 262-271.

[19] S.M. Sze., *Physics of Semiconductor Devices*, 2nd ed: New York:Wiley, 1983.

[20] Y. Feixia, M. C. Cheng and X. Jun, "High performance SOI DTMOS using a retrograde base with a low impurity surface channel," presented at *Semiconductor Device Research Symposium, International*, 2001. pp.613-616.

[21] G. Zhang, S. Zhibiao and Z. Kai, "Threshold Voltage Model of Short-Channel FD-SOI MOSFETs With Vertical Gaussian Profile", *Electron Devices, IEEE Transactions on,* vol.55, Issue 3, 2008, pp. 803-09.

[22] *S. Int.*, "ATLAS User manuals :A 2D numerical device simulator," 2004.

[23] A. Choudhury and P. Roy, "A Fairly Accurate Approximation to the Area Under Normal Curve," *Communications in Statistics - Simulation and Computation*, vol. 38,Issue.7, 2009 pp. 1485 - 1492.

[24] U. Monga and T. A. Fjeldly, "Compact Subthreshold Current Modeling of Short-Channel Nanoscale Double-Gate MOSFET," *Electron Devices, IEEE Transactions on*, vol. 56, Issue 7, 2009 ,pp. 1533-1537.

[25] B. Diagne, F. Prégaldiny, C. Lallement, J.-M. Sallese, and F. Krummenacher, "Explicit compact model for symmetric double-gate MOSFETs including solutions for small-geometry effects," *Solid-State Electronics*, vol. 52, Issue1., 2008; pp. 99-106.

[26] R. Granzner, V. M. Polyakov, F. Schwierz, M. Kittler, and T. Doll, "On the suitability of DD and HD models for the simulation of nanometer double-gate MOSFETs," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 19, Issue 1-2, 2003, pp. 33-38.

[27] N. D. Jankovic and G. A. Armstrong, "Comparative analysis of the DC performance of DG MOSFETs on highly-doped and near-intrinsic silicon layers," *Microelectronics Journal*, vol. 35, Issue 8, 2004, pp. 647-653.

[28] A. Kumar, J. Kedzierski, and S. E. Laux, "Quantum-based Simulation analysis of scaling in ultrathin body device structures," *Electron Devices, IEEE Transactions on*, vol. 52, Issue 4, 2005; pp. 614-617.

Pramod Kumar Tiwari was born in the Deoria district, Uttar Pradesh (UP), India on June 5, 1981. He received the B.E. degree in Electronics and Telecommunication from the C.C.S. University Meerut, UP, India in 2002, and the M.Tech. degree from the Department of Electronics Engineering, Aligarh Muslim University (AMU), Aligarh, India, in 2007. He is pursuing the Ph.D. degree in the Department of Electronics Engineering, Institute of Technology, BHU. His present research interests concern modeling, and simulation of nano-channel SOI-MOSFETs.

S. Jit was born in the Midnapore District, West Bengal, India, on November 2, 1970. He received the B.E. degree from the department of Electronics and Telecommunication Engineering, Bengal Engineering College, University of Calcutta, West Bengal, in 1993, M.Tech. degree from the Department of Electrical Engineering, Indian Institute of Technology (IIT), Kanpur, India, in 1995, and the Ph.D. degree from the Department of Electronics Engineering, Institute of Technology (IT), Banaras Hindu University (BHU), Varanasi, India in 2002. Dr. Jit has joined the Department of Electronics Engineering, IT-BHU, Varanasi as Lecturer in 1998 where he is working as Associate Professor since 2007.

Dr. Jit is the recipient of Visiting Fellowship of Indian National Science Academy (INSA) in 2006. He has worked as Postdoctoral Research Fellow in the Optolelctronics Laboratory, Department of Physics and Astronomy, Georgia State University, Atlanta, USA during March-August, 2007. He has published more than 40 papers in various peer reviewed international journals and conference proceedings. His present research interests include modeling and simulation of optically controlled microwave devices and circuits, Terahertz photodetectors, short-channel SOI-MESFETs, multi-gate SOI-MOSFETs, etc. Dr. Jit is a Life Member of The Institution of Electronics and Telecommunication Engineers (IETE), India.