# The Pulsed $I_d$-$V_g$ methodology and Its Application to the Electron Trapping Characterization of High-κ gate Dielectrics

**Chadwin D. Young*, Dawei Heh**, Rino Choi***, Byoung Hun Lee****, and Gennadi Bersuker***

*Abstract*—**Pulsed current-voltage (I-V) methods are introduced to evaluate the impact of fast transient charge trapping on the performance of high-κ dielectric transistors. Several pulsed I-V measurement configurations and measurement requirements are critically reviewed. Properly configured pulsed I-V measurements are shown to be capable of extracting such device characteristics as trap-free mobility, trap-induced threshold voltage shift ($\Delta V_t$), as well as effective fast transient trap density. The results demonstrate that the pulsed I-V measurements are an essential technique for evaluating high-κ gate dielectric devices.**

*Index Terms*—**High-κ, pulse I-V, threshold voltage instability, fast transient charge trapping, mobility, bias temperature instability, hafnium, MOSFET**

## I. INTRODUCTION

Since silicon dioxide gate dielectric thickness continues to be scaled, gate leakage current may exceed the required specification limits for future technology nodes. To circumvent this issue, higher permittivity (κ) gate dielectrics, which allow thicker dielectric layers at the same equivalent oxide thickness (EOT), have been introduced [1]. This new class of gate dielectrics requires new measurement methods and analysis. In particular, hafnium (Hf)-based oxides, which are being widely accepted as a leading candidate for high-κ gate dielectrics [1], exhibits high density of as-grown structural defects [2-16], some representing electron traps that complicate the evaluation of "intrinsic" performance in high-k gate stacks.

The electron charge trapping process potentially causes threshold voltage instability, mobility degradation, and poor reliability and performance, which are some of the primary issues affecting the use of Hf-based materials in production [17-65]. While significant progress has been made in fabricating high-κ gate stacks with less charge trapping [66-69], pulse-based characterization techniques [30, 70-73] remain critically important in understanding charge trapping processes for low power applications, memory cells, etc. This review addresses pulsed current-voltage (I-V) characterization and analysis approaches.

## II. FAST TRANSIENT CHARGE TRAPPING

Hf-based high-κ gate dielectrics exhibit a phenomenon known as the fast transient charging effect (FTCE) [37]. This effect is caused by substrate electrons injected to and captured by shallow traps (just below the Hf-based dielectric conduction band, Fig. 1) [74], where the trapping may occur within hundreds of nanoseconds to microseconds [50, 73]. The charges trapped during this process are well-localized within the dielectric, with their spatial distribution through the dielectric thickness being determined by the Fermi energy of the channel electrons and the trap energy (presumably, a neutral or single-charged negative oxygen vacancies) [4, 7, 9-11, 16]. The

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* SEMATECH, 257 Fuller Road, Suite 2200, Albany, NY 12203, USA
** Currently at National Nano Device Laboratories, Hsinchu, Taiwan
*** Currently at Inha University, 253 Yonghyun-dong, Nam-gu, Incheon 402-751, Korea
**** Currently at Gwangju Institute of Science and Technology, Korea
E-mail : chadwin.young@sematech.org

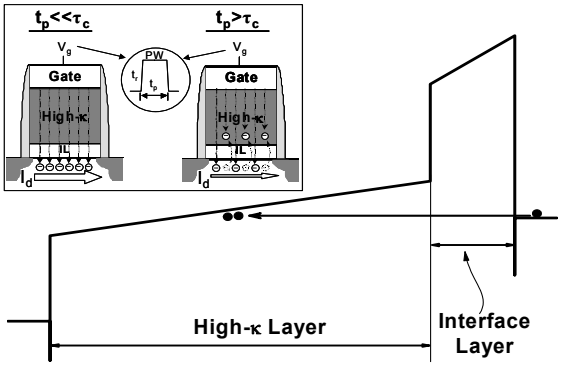



**Fig. 1.** Band diagram schematic for the electron trapping process during pulsed I-V measurements. Inset: Two scenarios are shown: when the pulse time $t_p$ (sum of $t_r$ and pulse width) is much shorter and longer than the trapping time $\tau_c$. The latter defines the onset of electron trapping into the high-κ bulk.

fast trapping, which is reversible with no residual damage [30, 75, 76], can contribute significantly to threshold voltage ($V_t$) instability and degradation of device performance in Hf-based gate stack nMOS transistors.

pMOS Hf-based transistors, on the other hand, typically exhibit negligible fast transient charging (FTC) [33, 77] in inversion due to a lack of defect states with the appropriate energies. An example is shown in Fig. 2 for an inversion bias of $V_g$ = -2 V with a standard mid-gap work function metal electrode illustrating that the FTC sites are far away from any resonant injection with the gate or substrate injection points. If significant FTC is detected, the test set-up or measurement may have issues [73] (should not be confused with NBTI measurements, which may have a fast component).

Because conventional DC characterization can be

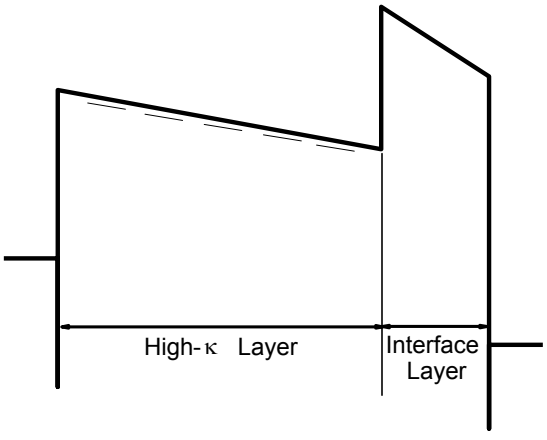



**Fig. 2.** Band diagram schematic for a pMOS gate stack illustrating injected electrons from the gate are not in resonance with the FTC trap sites, thereby demonstrating that negligible FTC occurs in pMOS devices.

adversely affected by FTC while the DC measurement is being conducted, thus lowering the drive current (Fig. 3(a)), the pulsed I-V methodology was introduced to quantify the transient charge trapping as well as to measure "intrinsic" (i.e., trapping-free) device characteristics [30, 70-72].

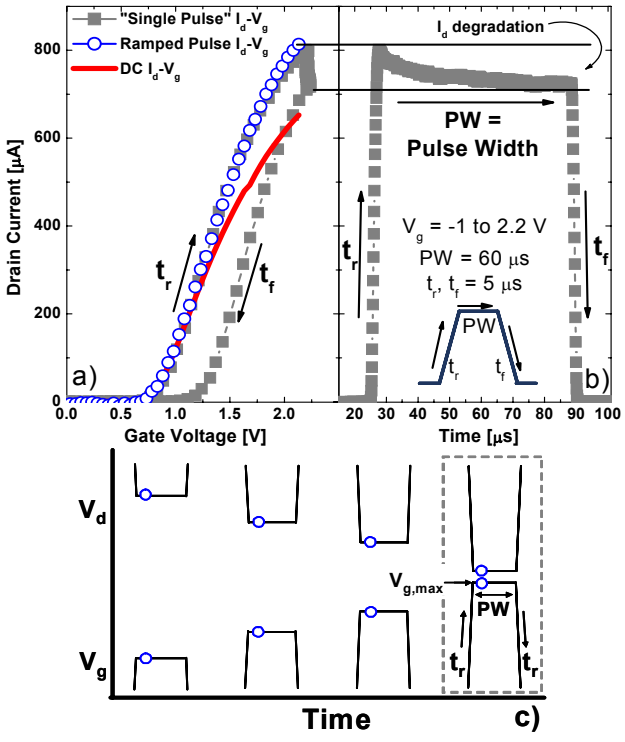



**Fig. 3.** Various forms of pulsed $I_d$ data in the (a) pulse voltage, or (b) time domains based on the "ramped" pulse or "single" pulse (dashed box) illustration in (c). Results clearly show that $I_d$ degrades at the top of the pulse (i.e., pulse width portion) due to FTC while the ramped pulse $I_d$ and the $t_r$ portion coincide to demonstrate trapping-free characteristics. DC $I_d$-$V_g$ is included for comparison.

## III. Measurement Technique and Instrumentation Configurations

### 1. Measurement Technique

Pulsed drain current-gate voltage ($I_d$-$V_g$) measurements are usually performed by applying a trapezoidal (e.g., rise time, pulse width, and fall time) or triangular (e.g., rise and fall time only) $V_g$ pulse on the gate of a transistor configured as an inverter and then measuring $I_d$. While a voltage pulse is applied to the gate of the FET, the $V_g$ and drain voltage ($V_d$) are simultaneously recorded on a digital storage oscilloscope. The drain

voltage response is converted to $I_d$ and plotted against the pulse bias,$V_g$, or pulse time. From the $V_d$ response, $I_d$ (in the linear regime) can be calculated as [78]

$$I_d = \frac{V_{dd}}{V_d}\left(\frac{V_{dd} - V_d}{R_L}\right) \quad (1)$$

where $V_{dd}$ is the drain voltage, $V_d$ is the drain response voltage, and $R_L$ is the load resistance.

Figs. 3(a) and 3(b) illustrate $I_d$-$V_g$ (pulse voltage domain) and $I_d$-time (pulse time domain) characteristics, respectively, wherein the change of $I_d$ during a "single" pulse measurement can be determined. The dashed box in Fig. 3(c) illustrates the "single" pulse wherein the $V_g$ pulse with its corresponding $V_d$ response is captured and converted into $I_d$-$V_g$ or $I_d$-time. From this, the hysteresis in the $I_d$-$V_g$ curve (Fig. 3(a)) or the decrease of $I_d$ in the $I_d$-time plot (Fig. 3(b)) illustrates the threshold voltage change due to charge trapping.

Another approach to the pulsed I-V technique is the "ramped pulse" I-V (Fig. 3(a)), which generates a complete $I_d$-$V_g$ curve within the total "single" pulse $V_g$ range by applying multiple pulses with incrementally rising amplitude $V_g$ up to $V_g = V_{g,max}$ and extracting $I_d$ at each $V_g$ value (Fig. 3(c)) [33, 72]. The advantage of this approach is that each pulse can have a very short characteristic time (around 37 ns = rise time + pulse width with ~0.1% duty cycle in this work), allowing "intrinsic" $I_d$ values to be obtained. It also provides better resolution by averaging the response pulse $V_d$ values during a portion of the pulse width time, thereby reducing the effect of fluctuations. Comparing this approach to the "single" pulse method (see Fig. 3(a)) revealed that a 5 μs rise time in the single pulse measurement is short enough to obtain the trapping-free $I_d$ characteristic in this particular gate stack due to the 1 nm $SiO_2$ interfacial layer since both techniques coincide on the "trapping-free" portion of the $I_d$-$V_g$.

In summary, the "ramped pulse" approach executes a truly trap-free $I_d$-$V_g$ curve, which is vital, for instance, for extracting intrinsic mobility [79]. However, because it is ultra-fast, this methodology does not allow the amount of trapping that can occur in the gate stack to be quantified. Therefore, the "single" pulse measurement should be used to study charge trapping. To obtain a correct charge trapping quantity, the rise time portion in the "single" pulse measurement must coincide with the ultra-short, "ramped" pulse one. In the ($I_d$-time) domain, the "single" pulse approach also delivers information on the charge trapping kinetics. This is the method used to obtain $\Delta V_t$, explained in section V-1.

## 2. Instrumentation Configurations

Four basic test set-up configurations have been employed to execute many of the pulse-based methodologies reported in the literature [30, 70-72]. In two of these configurations, the MOSFET is operated in an inverter circuit with a load resistor arranged in two ways: 1) a standard resistor placed in series between $V_{dd}$ and the drain of the MOSFET as shown in Fig. 4(a) [30], or 2) the 50 Ω environment of a radio frequency (RF) set-up (Fig. 4(b)) [72]. The third configuration, shown in Fig. 4(c), incorporates an operational amplifier (op-amp) [71] that takes advantage of the virtual short circuit property of op-amp operation. This allows the drain current to be measured across the sense resistor, R. The fourth measurement incorporates a current amplifier in series between common ground and the source of the MOSFET (Fig. 4(d)) [70].

### *A. "Conventional" set-up*

This configuration is a straightforward approach to setting up a pulsed $I_d$-$V_g$ measurement because it can be built using "standard" lab equipment and cables (Fig. 4(a)) [30]. This configuration can facilitate measurements typically within tens of microseconds when conducting the $I_d$-$V_g$ form of the measurement [30]. The time limitation is caused by not having a true radio frequency (RF)-capable configuration. Explicit and quantifiable limitations can be found in [71]. However, simply using a small dimension device (e.g., W/L = 10/1 μm or smaller) and relatively short cables will enable measurements in the tens of microseconds regime.

### *B. Ultra-Short Pulsed I-V set-up*

This configuration requires RF-capable instrumentation and test structures to achieve optimum measurement performance with nanosecond regime timing. The

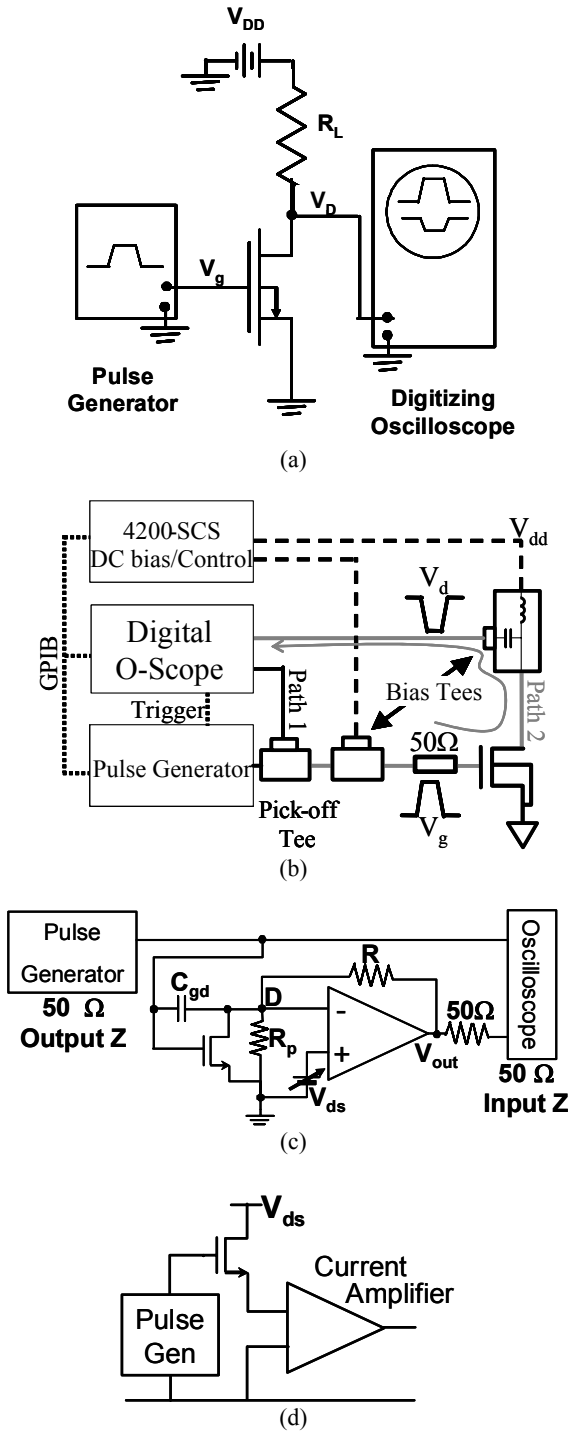



**Fig. 4.** (a) Schematic illustration of the measurement setup used for pulsed $I_d$–$V_g$ experiments in the μs range; (b) Experimental set-up for the ultra-short pulsed I-V measurement illustrating signal propagation paths (1 and 2) that should be equal in length and the internal circuitry of a conventional bias tee consisting of an inductor and capacitor; (c) custom op-amp circuit that takes advantage of the "virtual short" property of the op-amp to mitigate the charging and discharging of parasitic capacitance; (d) current amplifier configuration with the current amplifier placed between source and ground with $V_{dd}$ applied to the drain.

approach still operates with the device under test in an inverter circuit, but uses the 50 Ω environment as the load resistor. The difference in the experimental set-up is shown in Fig. 4(b) [72]. K. Jenkins, et al., first introduced this type of measurement configuration [80]. Bias tees present a critical component in this RF set-up due to the 50 Ω environment. The schematically shown bias tee in Fig. 4(b) isolates the AC and DC signals intended for the oscilloscope and transistor drain, respectively, from each other. Note that the characteristic charging time of the internal capacitor in the bias tee may limit the upper range of the pulse width while the minimum current resolution is limited by the voltage resolution of the scope at the smallest range divided by 50 Ω. The set-up discussed here also permits a pulsed $I_d$-$V_d$ capability due to the two bias tees used in the measurement set-up (Fig. 4(b)) without having to change the test set-up configuration [33, 73]. The "pick-off" tee used in the gate circuit in Fig. 4(b) allows the gate pulse voltage to be monitored non-intrusively. More configuration details can be found in [73]. A potential limiter of this technique is the need for RF timescale equipment and test structures. In addition, this ultra-fast measurement typically measures a completely trap-free result, which does not allow levels of fast transient trapping to be quantified. However, it should serve as a benchmark for all other pulse measurements to ensure an accurate FTCE analysis (see section V. 1.).

### *C. Operational Amplifier/Current Amplifier Set-up*

This configuration has been achieved in two ways: a) a custom design using a standard op-amp circuit (Fig. 4(c)) [71], and 4(b) a current amplifier (Fig. 4(d)) [70].

The custom-designed op-amp circuitry takes advantage of the short circuit property of the op-amp in which the voltage of the two inputs is expected to be equal. The fixed $V_{dd}$ applied to the drain is provided by the voltage source; therefore, the parasitic capacitance, $C_o$, does not charging or discharge [71]. The measured output voltage captured from the oscilloscope is linked to $I_d$ through the following expression [71]:

$$V_{out} = \left(I_d - I_{gd}\right) \cdot R + V_{ds} \tag{2}$$

where $I_{gd}$ is the gate-to-drain current through the parasitic

capacitor ($C_{gd}$), $V_{ds}$ is the drain voltage, and R is the sense resistance. Because the $C_{gd}$ is weak in short channel devices, $I_{gd}$ is negligible compared to the drain current, thereby allowing $I_d$ to be extracted. The limiting factor for the time resolution of this configuration is determined by the bandwidth of the op-amp. Further set-up details can be found in [71].

The current amplifier, placed in series between ground and the source terminal while $V_{dd}$ is applied to the drain, provides a relatively simple way to make the pulsed $I_d$-$V_g$ measurement when a $V_g$ pulse is applied to the gate of the MOSFET [70]. Similar to the op-amp circuit, the time resolution for this configuration is determined by the bandwidth of the op-amp.

## IV. MEASUREMENT REQUIREMENTS

Several key components must be implemented to ensure robust measurement execution, otherwise significant errors can occur that will impact the extracted signals that are captured and stored on the digital oscilloscope. First, the trapezoidal or triangular pulse should start and end at a discharge condition. For the FTCE, reversibility of this effect was found to be at a discharge voltage of -1V [30, 75, 76]. In addition, a very low duty cycle (e.g., $\leq$ 0.1 %) should be implemented. This allows the device under test to essentially be in an "off"/discharge condition most of the time and "on" for extremely short times. This way the "single" pulse can actually be a standard pulse train, allowing averaging if better resolution is desired and/or required to avoid fluctuations.

When using the measurement in the $I_d$-$V_g$ form (Fig. 3(a)), the input pulse (i.e., $V_g$ pulse) must be synchronized with the output response (i.e., response at the $V_d$ node, dashed box, of Fig. 3(c)). To achieve this, the signal "paths" must take the same propagation time to traverse the path and simultaneously arrive at the oscilloscope. This is achieved by having the same cable length path for the $V_g$ input and $V_d$ response and by having an oscilloscope that can effectively remove any remaining propagation delay (e.g., paths 1 and 2 in Fig. 4(b)) [73, 81]. If this is not done, a measurement error could occur at the minimum frequency/time range of the particular pulse set-up. The error can manifest itself as a false hysteresis as shown in Fig. 5. This 2 nm $HfO_2$ gate stack,

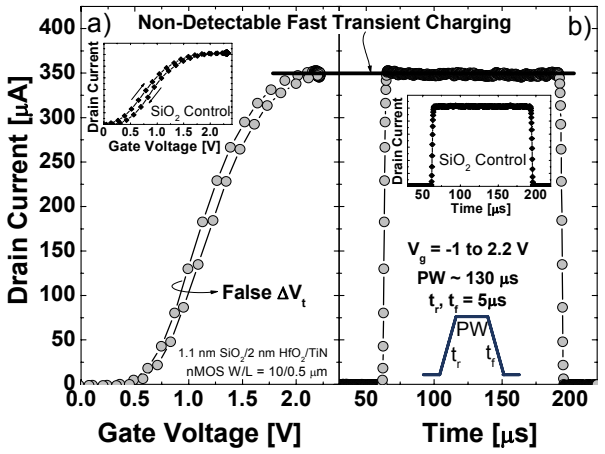



**Fig. 5.** Single pulsed I-V data illustrating a hysteresis artifact ($\Delta V_t$) in the $I_d$-$V_g$ domain (a) while no detectable charging (i.e., $I_d$ degradation) is observed in the time domain, (b). The measurement set-up limitation is verified by the artificial hysteresis on conventional $SiO_2$, which does not exhibit the FTCE (insets).

which has not suffered from significant FTC [66, 69, 82], should not exhibit any hysteresis. However, Fig. 5a clearly illustrates a small hysteresis, although the $I_d$-time data (Fig. 5(b)) shows no decay in the pulse width portion. The inset results exhibit a $V_t$ shift artifact for a fast trapping-free $SiO_2$ sample (insets, Fig. 5) as well, confirming the hysteresis is not real. Therefore, estimating $\Delta V_t$ as a shift between $I_d$-$V_g$ traces corresponding to the rise and fall of the pulse bias may not be accurate [70, 83, 84] when a non-optimized measurement set-up is used.

## V. APPLICATIONS

The pulsed I-V methodology can be used for more than just measuring the "intrinsic" drive current performance in the absence of FTC. Proper analysis techniques can provide information on charge trapping [32, 70-74, 81, 83, 85] and the effect on device performance, separation of fast and slow trapping processes [20, 32, 50, 54, 55, 74, 86], and bias temperature instability [50, 87-90].

### 1. Quantifying Trapped Charge and Its Effects on Device Performance

Using pulsed $I_d$-time [30, 33, 73, 83] or a correction technique for pulsed $I_d$-$V_g$ can circumvent the issues discussed in section IV [81]. In the case of $I_d$-time, very

fast rise and fall times can be used since propagation delay is not an issue. The $V_d$ response is plotted against time instead of the input $V_g$ pulse. The degradation in $I_d$ with time is reflected in the fast transient charge trapping. The threshold voltage shift, $\Delta V_t$, can be determined from the change in $I_d$ through the expression [83, 91]

$$\Delta V_t = \frac{\Delta I_d}{I_d}\left(V_g - V_t\right) \quad (3)$$

where $\Delta I_d$ is the $I_d$ degradation between the start and end of the $V_g$ pulse width, $I_d$ is the maximum $I_d$ before transient charging, $V_g$ is the pulse amplitude applied to the gate, and $V_t$ is the threshold voltage. The approximation used in Eq. (3) is applicable when mobility does not decrease significantly due to a high vertical field in the channel caused by high gate bias (i.e., when $V_g$ is so high that the slope of the $I_d(V_g)$ curve decreases significantly from its maximum value corresponding to maximum transconductance, $g_{m,max}$) [81].

Fig. 6 illustrates pulsed mobility extracted (to be discussed in section V-1, part A) from the rise (i.e., trapping-free) and fall (i.e., after trapping) time portions showing similar effective mobility values. Even after 100 μs of charging time, the falling $I_d$-$V_g$ curve appears to be parallel to the rising curve suggesting no significant impact due to remote coulomb scattering from the trapped electrons (Fig. 6, inset), which confirms the applicability of Eq. (3) to this particular gate stack. The negligible effect of the trapped electrons on intrinsic mobility can be understood when one considers that the trapped charges are located in the bulk of the high-κ [76, 79], relatively far from the channel.

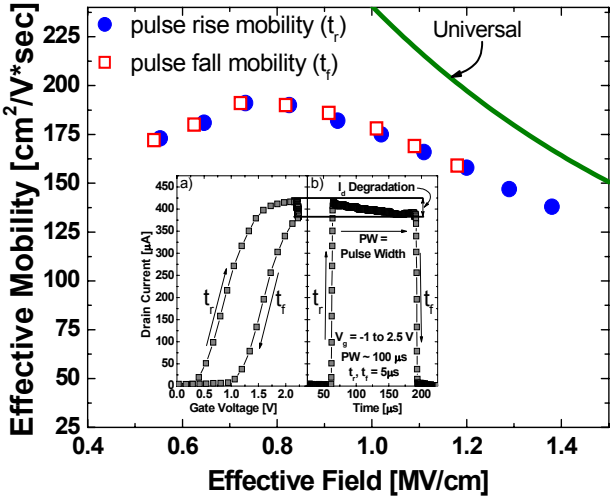



**Fig. 6.** Similar mobility values extracted from the rise (trap-free) and fall (after trapping) portions of the single pulse measurement (inset, a) demonstrating that remote coulomb scattering is negligible in high-κ gate stacks due to bulk trapping beyond the 1 nm $SiO_2$-like interfacial layer.

Therefore, similar pulse data in Fig. 3 can be used as an example of measurements where Eq. (3) is applicable: $\Delta V_t$ obtained from the data in Fig. 3(b) using Eq. (3) is equal to the hysteresis value extracted from Fig. 3(a). A precise expression for $\Delta V_t$, which takes into account variation of the mobility value with changing threshold voltage, is given in [83]. With this extraction procedure for $\Delta V_t$, the onset of FTCE can be evaluated [33]. Fig. 7 demonstrates the two extremes, with ($t_p > \tau_c$) and without ($t_p << \tau_c$) FTC, for a sample with significant trapping, as illustrated in Fig. 1. By applying pulses with a $t_p$ magnitude between these extreme values, the onset of trapping, $\tau_c$, can be determined.

For any pulsed I-V measurement, the pulse rise time plus its width represents the charging time, $t_p$. To ensure the absence of FTCE, the pulse charging time must be shorter than the onset of the trapping time, $\tau_c$. This is schematically illustrated in Fig. 1 (inset), which includes two extreme cases of $I_{d,sat}$ current measured with ultra-short ($t_p << \tau_c$) and long pulse times. Fig. 8 shows an example of the effect of the pulse rising time (charging time) on $I_d$ [73]. Dependence on the pulse rising times reflects on the charging at higher $V_g$ values. Significant charging during the pulse rising time may result in FTCE being underestimated. Therefore, a measurement capability

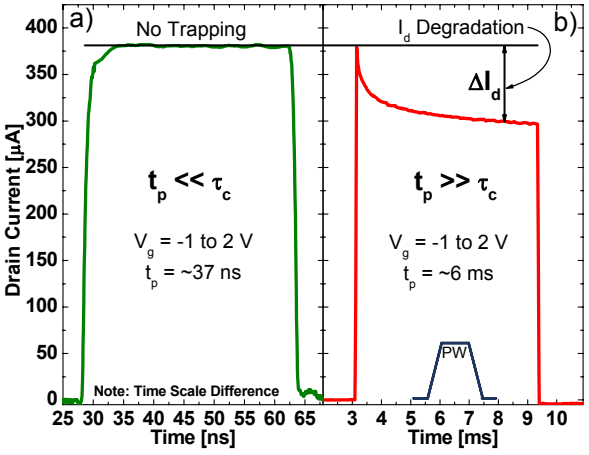



**Fig. 7.** Pulse $I_d$ dependence on the charging time $t_p$ when (a) $t_p$ « $\tau_c$ (no electron trapping), and (b) $t_p$ » $\tau_c$ (electron trapping is proportional to $\Delta I_d$).

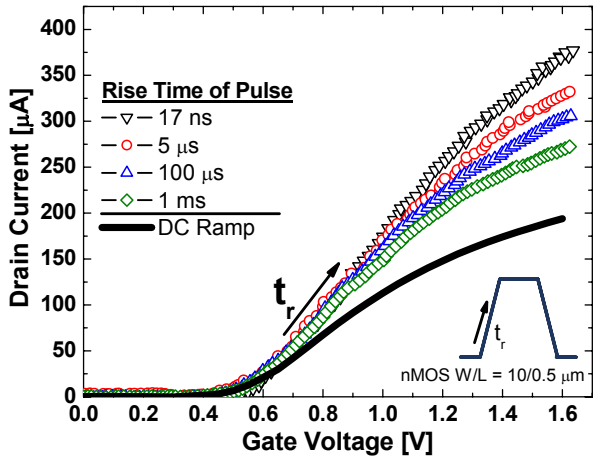



**Fig. 8.** Single pulsed I-V measurements on high-κ demonstrating the impact of the pulse rise time on charging. A fast enough rise time (i.e., short $t_r$) ensures a "trap-free" drain current.

that ensures a trapping-free characteristic throughout the entire pulse measurement is required to guarantee no FTCE. In addition, highly scaled interfacial layers in high-κ gate stacks may exhibit very fast trapping, which would require pulse measurements below the microsecond regime (Fig. 8). This can be achieved by using the ultra-short pulsed I-V set-up in Fig. 4(b). Furthermore, this is a potentially powerful measurement technique for characterizing high-κ gate stacks on silicon-on-insulators when self-heating effects should also be eliminated to achieve intrinsic device performance [80].

Another approach, which uses the pulsed $I_d$-$V_g$ hysteresis, can be employed when the limitations of being able to use eq. (3) have been exceeded (Fig. 9) [81]. This approach effectively negates the propagation delay by intentionally introducing a phase delay time between

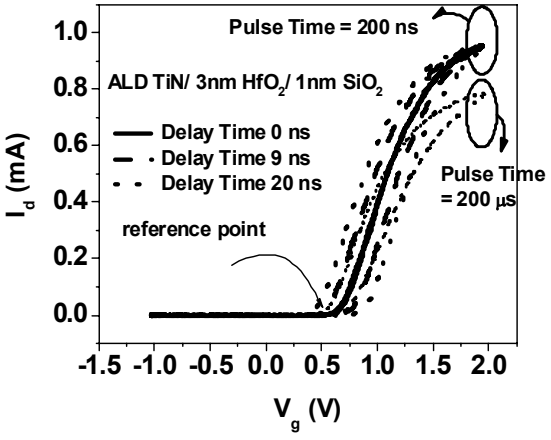



**Fig. 9.** The effect of phase delay time between the two input channels of the oscilloscope on the measured hysteresis of the $I_d$-$V_g$ curves in a single pulse measurement.

the two channels of the oscilloscope. To obtain the accurate phase delay time to compensate for the propagation delay, $I_d$-$V_g$ curves generated by "short" and "long" triangle pulses with equal rise and fall times, should be compared (Fig. 9). Three different phase delay times ranging from zero to 20 ns were used in both short (thick curves) and long (thin curves) pulses. It can be seen that the $I_d$-$V_g$ curves generated by the short pulses are strongly affected by the phase delay times, which result in different $I_d$-$V_g$ hysteresis values. On the other hand, the complete overlap of the long pulse curves obtained with different delay times indicates that the phase delay times in the ns range have no effect on the pulse in the μs range. Therefore, by varying the phase delay time in the short pulse measurement to match the $I_d$-$V_g$ curves of the short and long pulses within the voltage range for $V_g$ less than $V_t$ (where no FTCE takes place), the correct phase delay time that compensates the signal delay due to different propagation paths for the given pulse measurement set-up can be determined.

### *A. Impact of Dielectric Properties on Fast Transient Charge Trapping*

Typical high-κ gate stack structures are comprised of two layers: an interfacial layer and a high-κ layer (Fig. 1). During gate stack fabrication, the interfacial layer can be engineered or it can grow spontaneously [33, 78, 92, 93]. The FTCE can be influenced by these two layers as well as by the amount of hafnium in the high-κ layer.

Effects of the interfacial layer thickness, physical thickness of the high-κ dielectric, and its Hf content on the fast electron trapping process were evaluated by using a combination of the ultra-fast pulse technique described above (covering the range up to 100 ns) and the conventional "single" pulse (covering the range between 100 ns to 6 ms) [30, 76, 94]. The effect of interfacial layer thickness is demonstrated in Figs. 10-12. Since the trap sites in the high-κ layer are filled by tunneling from the inversion layer through the interfacial layer (Fig. 1), a thinner interface leads to a stronger tunneling current and, hence, greater electron trapping. Accordingly, critical time (the pulse width at which the onset of trapping occurs), $\tau_c$, decreases and the $V_t$ shift increases for thinner interfacial oxides (Fig. 10). The impact of electron trapping on DC mobility is shown in

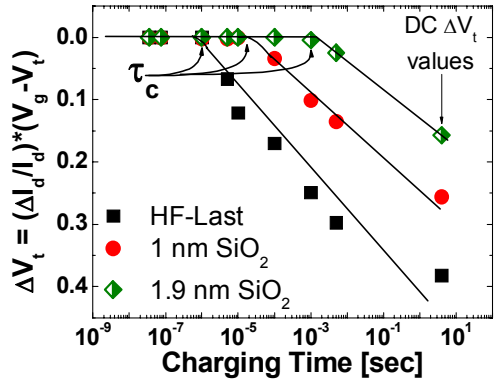



**Fig. 10.** Normalized $\Delta V_t$ for varying IL thicknesses. Thicker IL increases the tunneling distance (see Fig. 1) to available traps, thereby increasing $\tau_c$.

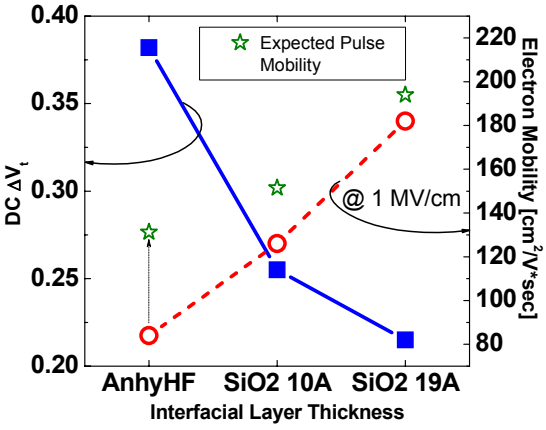



**Fig. 11.** Correlation of $V_t$ shift (trapped charge) to the extracted DC mobility illustrating degraded mobility as the IL becomes thinner.

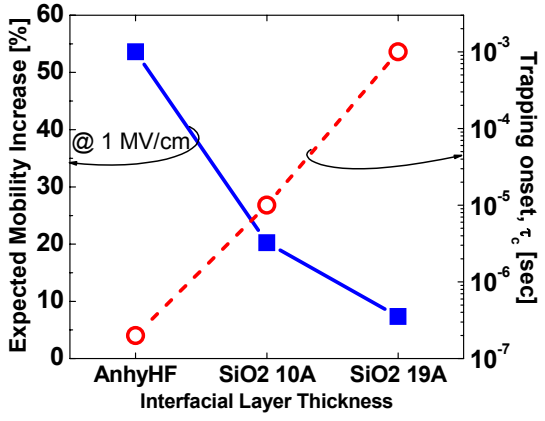



**Fig. 12.** Expected mobility increase (thinner IL → larger pulse/DC $I_{d,lin}$ ratio) as a function of interfacial layer thickness compared with the onset of the critical time, $\tau_c$.

Fig. 11 where the DC mobility increases as the $\Delta V_t$ values, calculated based on the $\Delta I_d$ [83, 91], diminish in proportion to the thickness of interfacial layer.

A mobility increase (which may be expected if the fast charge trapping is eliminated), called "expected mobility," was estimated from the ratio of $I_{d,lin}$ values measured in the pulse and DC regimes (Figs. 11 and 12).

For samples of different $HfSi_xO_y$ (20% $SiO_2$) physical thicknesses of 3, 5, and 7 nm, all with a TiN electrode, the interfacial layer was fixed at ~1 nm $SiO_2$. As the physical thickness of the dielectric increases, the total number of traps accessible at the given applied bias also increases, or the filled trap location shifts towards the device channel, resulting in a greater $V_t$ shift [76] (Fig. 13) that correlates with the degradation of the electron mobility (Fig. 14).

Hafnium content has an apparent influence on both the electron trapping and $\tau_c$ (Figs. 15 and 16). The $\Delta V_t$ increases with the Hf content indicating that electron traps may be associated with the Hf atoms.

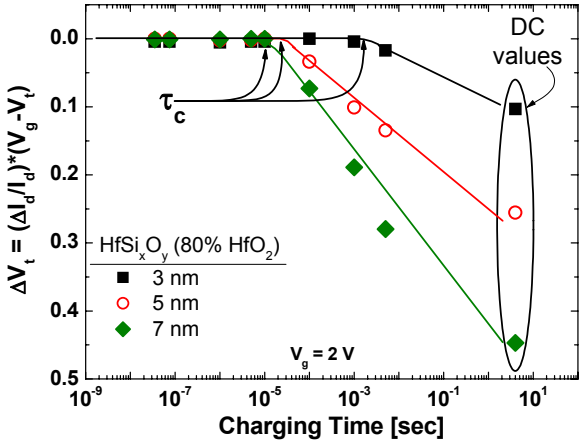



**Fig. 13.** $\Delta V_t$ for various high-κ physical thicknesses. Physically thicker high-κ is subject to faster and more severe charge trapping.

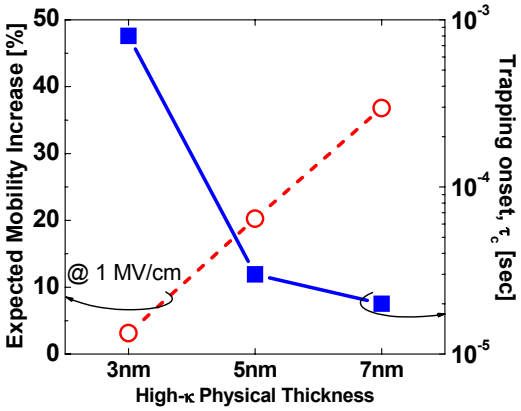



**Fig. 14.** Expected mobility increase (thinner high-k → larger pulse/DC $I_{d,lin}$ ratio) as a function of high-κ layer thickness compared with the onset of the critical time, $\tau_c$.

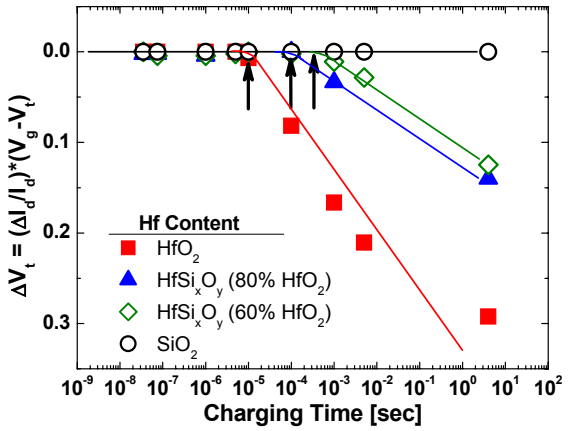



**Fig. 15.** Normalized $\Delta V_t$ for various hafnium contents. More Hf results in faster and greater charge trapping.

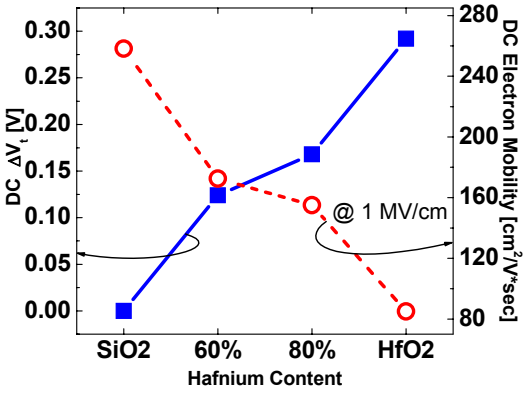



**Fig. 16.** An increase in DC $\Delta V_t$ and the corresponding decrease in DC mobility as the Hf content increases.

*B. Factors Controlling $V_t$ shift*

In the pulsed I-V measurement, the effect of the trapped charge on $\Delta V_t$ is primarily determined by the $V_g$ pulse conditions. The $V_g$ pulse amplitude affects both the magnitude of the injection current and the point of injection (the charge trapping location) in the dielectric. To understand the major factors controlling $\Delta V_t$—charge supply or trapping location with respect to the gate electrode—the pulse width was fixed at 100 μs and the pulse $V_g$ (i.e., pulse height) was varied to study the bias dependence [73].

It has been demonstrated that the fast trapping process, with a characteristic time of about 100 μs, is independent of temperature, implying that the pre-existing traps are filled by the resonant capture of the tunneling electron injected from the substrate [20, 74]. The charges trapped by this process are well-localized within the dielectric thickness, with their location being determined by the Fermi energy of the channel electrons and the trap energy, whose value is close to the $HfO_2$ conduction band edge, Fig. 1 (presumably, a neutral or single-charged negative oxygen vacancy) [4, 7, 9-11, 16]. Therefore, we assume for simplicity that the traps are characterized by a single energy value that is close to the bottom of the conduction band [4, 20, 74]. For longer stress times, over 1 second, the trapped charge distribution widens due to slow temperature-activated electron capture processes [50, 74].

The obtained dependences of $\Delta V_t$ vs. injected charge, Fig. 17, show no correlation, indicating that fast transient charging is not a charge supply-driven phenomenon. To evaluate the impact of the position of the trapped charge on $\Delta V_t$, band diagrams were constructed, as shown in the examples in Fig. 18, based on the physical thicknesses and κ values of each layer in the different bi-layer stacks under investigation. The band diagrams were generated for various $V_g$ pulses using the software developed by Boise State University [95]. Then, at the given $V_g$, the location of the trapped charge is defined by the resonance between the Fermi level in the substrate and the energy level of the pre-existing traps in the Hf-based dielectric [50, 74]. Knowing the distance of the trapped charge from the gate electrode allows the trap charge density to be calculated by

$$N_{trap} = \frac{\varepsilon_o \cdot \kappa \cdot \Delta V_t}{q \cdot x} \quad (4)$$

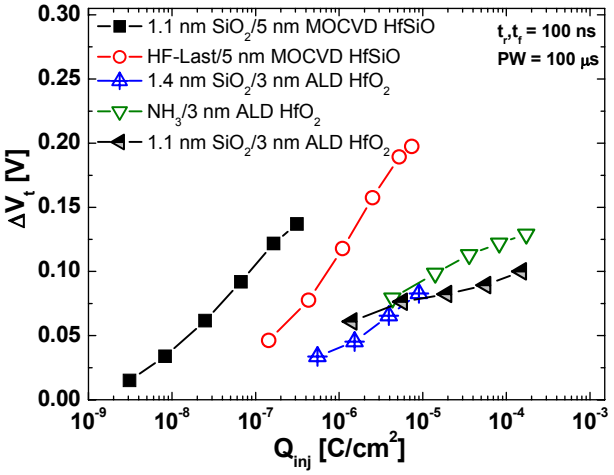



**Fig. 17.** $\Delta V_t$ vs. the injected charge, $Q_{inj}$ illustrating no correlation between the $\Delta V_t$ and injected charge.

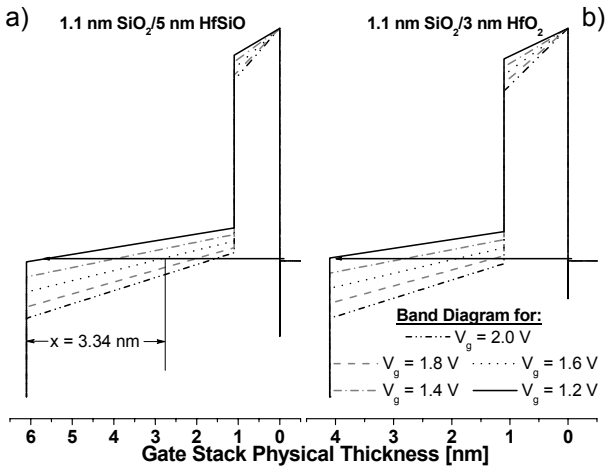



**Fig. 18.** The gate stack energy band diagrams for (a) 1.1 nm $SiO_2$/5 nm HfSiO and (b) 1.1 nm $SiO_2$/3 nm $HfO_2$ for various pulsed $V_g$ values. An example of the resonant electron trapping location with respect to the Fermi level for $V_g$ = 1.6 V is shown.

where $\Delta V_t$ is the extracted threshold voltage shift, $x$ is the experimentally extracted distance from the gate electrode (example, Fig. 18(a)), $q$ is the fundamental electron charge, $\varepsilon_o$ is the permittivity of free space, and κ is the dielectric constant of the high-κ layer. (For more details on the assumptions and limitations of this trap density extraction procedure, see [73].)

By changing $V_g$, one can obtain x and thus the trap density profile across the thickness of the high-κ film using Eq. (4). While the position x at each given pulse voltage may not be defined exactly, the measurements still allow the relative distribution of x values to be extracted in a self-consistent way. Fig. 19 shows the

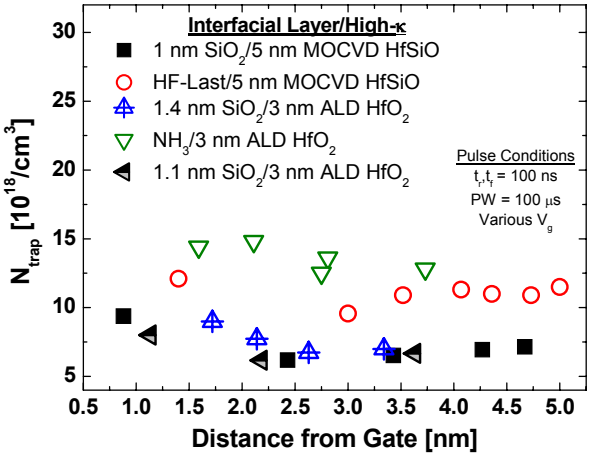



Fig. 19. Defect density profile of different high-κ gate stacks calculated using the resonant trap location distance referenced from the gate electrode (Fig. 18) for the corresponding $V_g$ pulse value.

defect profiles for several gate stacks. Within the referenced assumptions, uniform trap density profiles were obtained in all gate stacks analyzed in this study. As follows, the observed increase of $\Delta V_t$ with the pulse amplitude is due to the trapped charge being closer to the substrate rather than the amount of the trapped charge being greater.

In summary, this approach probes each sample through its high-κ thickness by changing the measurement pulse voltage, thereby changing the band bending (i.e., resonant trapping point), which allows trap density information to be directly extracted at each point in the given sample [73].

### *C. The Effect of FTC on Channel Mobility*

In the linear regime, the FTCE can significantly impact mobility [31, 63, 64, 66, 79, 83, 91, 92, 96-98]. In a conventional DC sweep of the $I_d$-$V_g$ measurement, the threshold voltage shifts as the measurement progresses, thereby decreasing the drive current at each bias sweep point resulting in decreased mobility. Several FTC correction techniques discussed in the literature can correct for this effect [31, 63, 79, 83]. One technique that requires only two measurements and minimal data analysis was presented in [79]. In this approach, pulsed $I_d$-$V_g$ is combined with North Carolina State University's CVC [99] and mob2d [100] modeling parameter extraction software. To extract mobility, mob2d performs a non-linear, least squares fit to experimental pulsed $I_d$ data in conjunction with the EOT and substrate doping supplied from CVC. EOT and substrate doping are negligibly impacted by FTC [101]. Therefore, the result is a trap-free mobility extraction. Fig. 20 illustrates the impact of trapped charge in the DC mobility data compared to the trap-free, pulsed-based extraction for the $I_d$-$V_g$ data in the inset where the pulse-based mobility is higher than its DC-based counterpart [32, 80]. Fig. 21 compares the pulse and DC mobility extractions using CVC and mob2d for high-κ gate stacks with different interfacial layer (IL) thicknesses. The sample with a 1.9 nm $SiO_2$ interfacial layer exhibits essentially the same DC and pulsed mobility since fast transient charging is negligible in thick interfaces (quite similar DC and pulsed $I_d$-$V_g$ curves – not shown). As the interface becomes thinner, the difference between the pulsed and

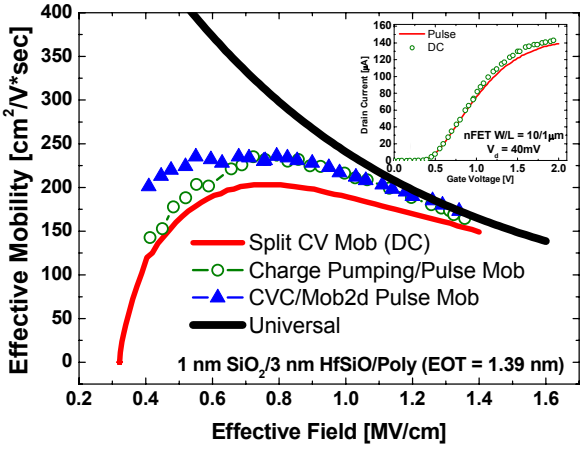



**Fig. 20.** Comparison of DC mobility to the novel pulse mobility technique for the $I_d$-$V_g$ data in the inset. The mobility values extracted using the proposed mob2d pulse methodology and the direct measurement of $N_{inv}$ technique [32] show excellent agreement.

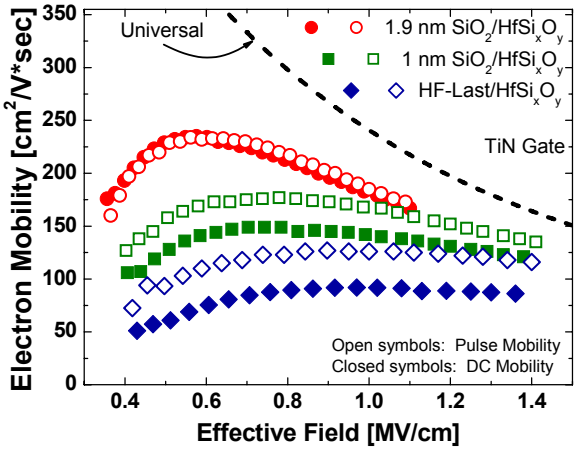



**Fig. 21.** Application of the pulse mobility extraction method [80] to gate stacks with interfacial layers (IL) of varying thicknesses and fixed $HfSiO_x$ dielectric layer.

DC mobility for a given gate stack becomes greater. The overall degradation in the pulsed (intrinsic) mobility as the interface layer becomes thinner can be attributed to poorer interfacial layer quality [102] and greater effects of soft optical phonons [64] and crystallinity [21, 103].

*D. Fast Transient Trapped Charge Relaxation*

Reports have shown that, in addition to FTC, high-κ gate dielectrics also demonstrate fast relaxation of the trapped charge, although on a slightly longer time scale [88, 104]. Fig. 22 illustrates this fast relaxation phenol-menon. After a two-level $V_g$ pulse (Fig. 22 inset: the high level is in strong inversion, and the low level is just above $V_t$) the drain current recovers due to relaxation (charge detrapping) at this low $V_g$ level in ~ 150 μs. Fig. 23 demonstrates that the trapped charge can return to the DC measurement results in as little as 250 μs.

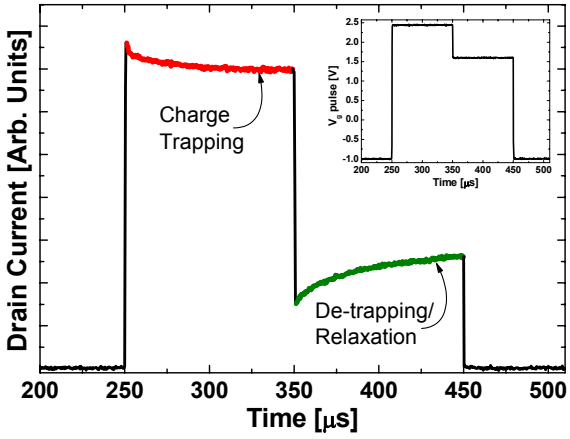



**Fig. 22.** Illustration of fast transient charge trapping ($I_d$ decay) and detrapping ($I_d$ recovery) for the $V_g$ pulse in the inset.

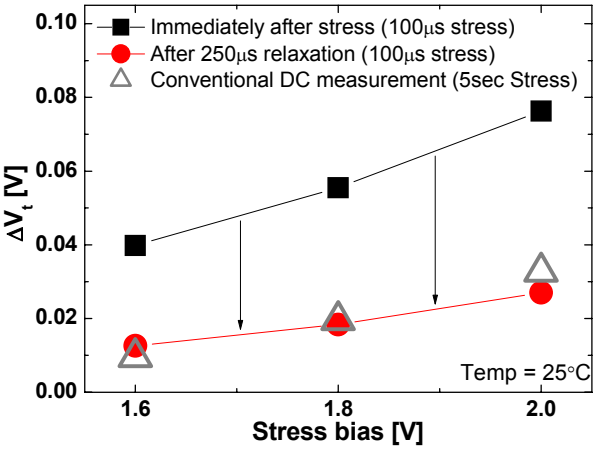



**Fig. 23.** $V_t$ shifts immediately after the 100 μs stress and after 250 μs of post-stress relaxation compared to conventional "stress and sense" approach.

## 2. Implications of Fast Transient Trapping and Detrapping During Stress Measurements

Note that since fast trapping and recovery can occur in high-κ gate stack transistors, it significantly impacts positive bias temperature instability with an adverse effect on the lifetime projection [87, 88]. Fast recovery can occur between the stress and "sense" (i.e., monitoring parameter measurement) of conventional constant voltage stress with interspersed DC $I_d$-$V_g$ measurements ($V_t$ extraction) due to the interval between the removal of the stress and the subsequent "sense" $I_d$-$V_g$

measurement. This can lead to significant underestimation of the $V_t$ shift [22, 25, 32, 84, 89, 90, 105, 106]. Therefore, the time delay between the stress and measurement must be shortened.

### *A. Effect of Relaxation and Its Impact on the Lifetime Projection*

Several techniques have been introduced in the literature to mitigate the effects of fast relaxation [88, 90, 107]. One of particular interest employs the pulsed I-V methodology [88, 90]. Fig. 24 illustrates the measurement schematic for the pulsed approach vs. conventional DC stress and sense. As Fig. 24(b) shows, the pulsed I-V is measured immediately in the downward pulse from the stress condition, thereby removing any relaxation [88]. To study the impact of fast relaxation on the extraction of $V_t$, the $I_d$ of the rising trace on the inverted triangular pulse can be extracted after modulating the fall time of the downward portion, which can effectively quantify the relaxation time [88]. The results are shown in Fig. 25 where the quantity of the trapped charge, reflected in the $V_t$ shift, is similar to the results of the conventional DC approach as the relaxation time increases [88]. Moreover, the slopes (i.e., power law exponents) change significantly with changes in the relaxation time. Therefore, it is worthwhile to separate the effects of the fast relaxation on the time evolution of degradation with stress.

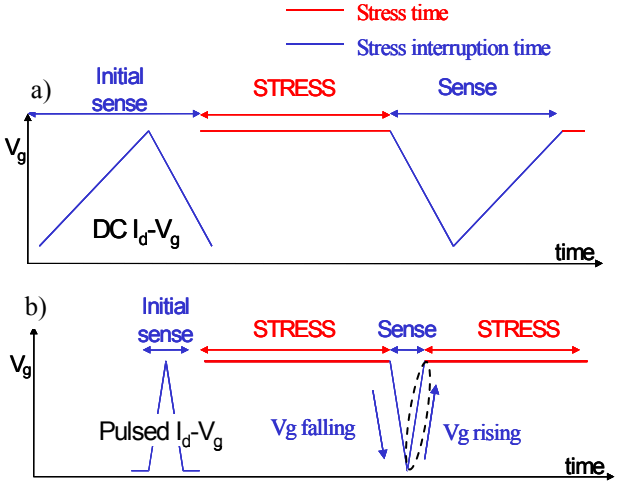



**Fig. 24.** The schematic comparison of stress-sense schemes using the stress-interrupted DC $I_d$-$V_g$ method and single pulse method.

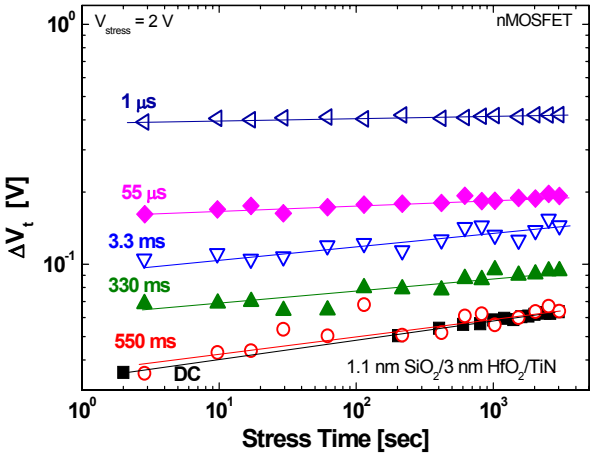



**Fig. 25.** $\Delta V_t$ dependence on stress time when extracting $V_t$ from the rising portion of $V_g$ (see Fig. 24(b)) for different pulse times.

### *B. Separation of Fast and Slow Trapping*

In addition to fast transient mechanisms, slow trapping and/or trap generation can impact $V_t$ instability in high-κ transistors when constant voltage stress is measured [22, 25, 30, 34, 84, 88, 89, 105]. The oxygen vacancy defects responsible for the FTCE have also been found to exhibit a temperature-activated slow migration of trapped electrons to unoccupied traps [50, 74]. Fig. 26 illustrates these two components over a long time scale [50]. A temperature-independent feature is detected in fast measurement times (pulsed I-V regime), indicating a direct tunneling mechanism to the neutral or single-charged negative oxygen vacancy fast transient traps. Then, at longer stress times, a temperature effect is seen when a larger $\Delta V_t$ is extracted at the higher temperature. The fast relaxation detraps in a similar manner [50].

To remove the effect of the FTC so that only the slow migration and/or trap generation can be studied, the previously mentioned pulsed I-V combined with constant voltage stress and subsequent data analysis was used [88]. A physical model-based subtraction of the initial $V_t$ (contains only the fast relaxation portion) from each subsequent $V_t$ point in the time dependence effectively removes the fast transient detrapping component [88]. Fig. 27 shows parallel curves after the initial data point subtraction provides a “universal” slope, which suggests that the dependence of the power law exponent on pulse time is due to fast transient charge detrapping [87]. In addition, Fig. 28 further confirms this universality because different measurement techniques have a very similar

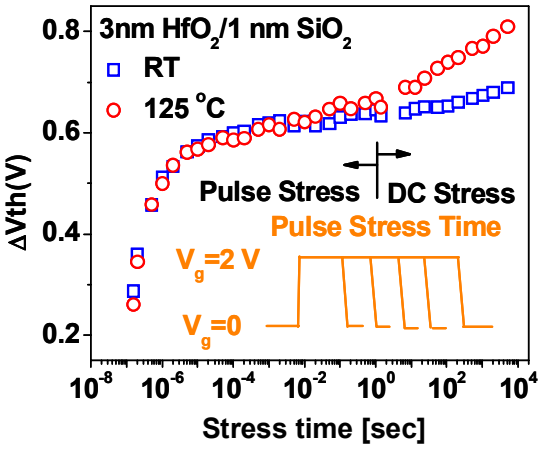



**Fig. 26.** Fast (temperature-independent) and slow (temperature-dependent) charge trapping processes in typical $HfO_2$ gate stacks where the fast process pseudo-saturates within 100 μs and transitions to the slow process around $10^{\circ}$ sec of stressing.

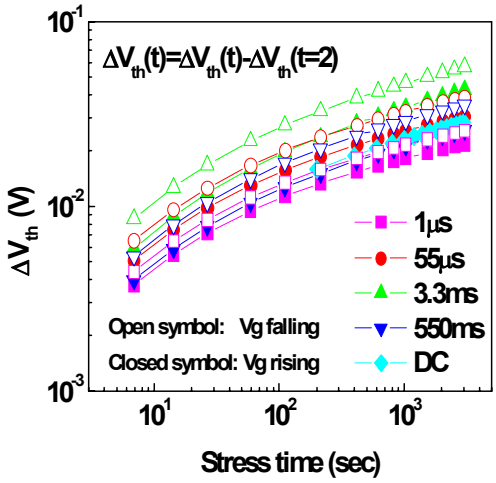



**Fig. 27.** The power law dependence after removal of the FTC portion of the $V_t$ shift (i.e., subtraction of the first $\Delta V_t$ point from all subsequent points) demonstrating that all curves fall on an intrinsic curve regardless of the sense measurement time.

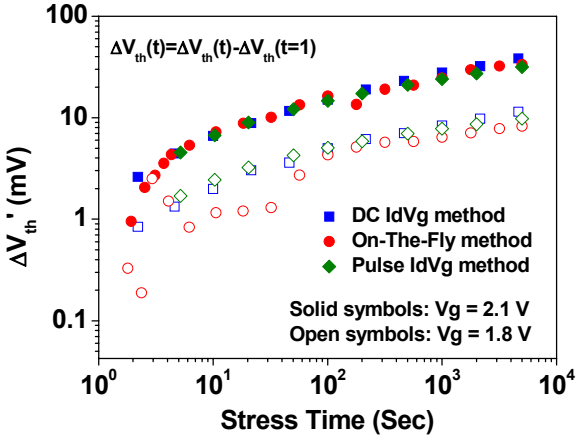



**Fig. 28.** The correlation of $\Delta V_t$ measured using different characterization methods.

slope (power law exponent) after removing the fast transient effects when measured on the same high-k gate dielectric stack [87].

## VI. Conclusions

Several pulsed I-V measurement configurations have been critically evaluated. The ultra-short pulsed I-V method is found to be the benchmark for determining truly trap-free characteristics of high-κ gate dielectric devices. The pulsed I-V methodology is shown to be capable of obtaining "intrinsic" (i.e., trap-free) performance of hafnium-based gate dielectrics. To evaluate reliability, the pulsed-based approach is required to extract device lifetime, which can be impacted by the fast transient phenomena. However, to ascertain the trap-free results requires a rigorous evaluation of the measurement configuration along with its corresponding analysis. Failing to calibrate the measurement set-up properly (or employing a set-up that is too slow) results in an underestimation of the $V_t$ shift, effective mobility, and trap density.

## References

[1] R. M. Wallace and G. D. Wilks, "Alternative Gate Dielectrics for Microelectronics," in *MRS Bulletin*, 2002, pp. 186-191.

[2] G. Bersuker, B. H. Lee, and H. R. Huff, "Novel Dielectric Materials for Future Transistor Generations," *International Journal of High Speed Electronics and Systems,* vol. 16, pp. 221-239, 2006.

[3] G. Bersuker, P. Zeitzoff, G. A. Brown, and H. R. Huff, "Dielectrics for Future Transistors," *Materials Today,* pp. 26-33, 2004.

[4] P. Broqvist and A. Pasquarello, "Oxygen vacancy in monoclinic $HfO_2$: A consistent interpretation of trap assisted conduction, direct electron injection, and optical absorption experiments," *Applied Physics Letters,* vol. 89, p. 262904, 2006.

[5] P. Broqvist and A. Pasquarello, "First principles investigation of defects at interfaces between silicon and amorphous high-[kappa] oxides,"

*Microelectronic Engineering,* vol. 84, pp. 2022-2027, 2007.

[6] E.-A. Choi and K. J. Chang, "Charge-transition levels of oxygen vacancy as the origin of device instability in $HfO_2$ gate stacks through quasiparticle energy calculations," *Applied Physics Letters,* vol. 94, p. 122901, 2009.

[7] J. L. Gavartin, D. M. Ramo, A. L. Shluger, G. Bersuker, and B. H. Lee, "Negative oxygen vacancies in $HfO_2$ as charge traps in high-k stacks," *Applied Physics Letters,* vol. 89, p. 082908, 2006.

[8] M. Jo, H. Park, M. Chang, H.-S. Jung, J.-H. Lee, and H. Hwang, "Oxygen vacancy induced charge trapping and positive bias temperature instability in HfO2nMOSFET," *Microelectronic Engineering,* vol. 84, pp. 1934-1937, 2007.

[9] D. M. Ramo, J. L. Gavartin, A. L. Shluger, and G. Bersuker, "Intrinsic and defect-assisted trapping of electrons and holes in $HfO_2$: an ab initio study," *Microelectronic Engineering,* vol. 84, pp. 2362-2365, 2007.

[10] D. M. Ramo, J. L. Gavartin, A. L. Shluger, and G. Bersuker, "Spectroscopic properties of oxygen vacancies in monoclinic $HfO_2$ calculated with periodic and embedded cluster density functional theory," *Physical Review B (Condensed Matter and Materials Physics),* vol. 75, p. 205336, 2007.

[11] D. M. Ramo, A. L. Shluger, J. L. Gavartin, and G. Bersuker, "Theoretical Prediction of Intrinsic Self-Trapping of Electrons and Holes in Monoclinic $HfO_2$," *Physical Review Letters,* vol. 99, p. 155504, 2007.

[12] J. Robertson, K. Tse, D. Liu, and K. Xiong, "Oxygen vacancies in high-k oxides "*Microelectronic Engineering,* vol. 84, pp. 2028-2031, 2007.

[13] K. Tse, D. Liu, K. Xiong, and J. Robertson, "Oxygen vacancies in high-k oxides," *Microelectronic Engineering,* vol. 84, pp. 2028-2031, 2007.

[14] H.-C. Wen, H. R. Harris, C. D. Young, H. Luan, H. N. Alshareef, K. Choi, D.-L. Kwong, P. Majhi, G. Bersuker, and B. H. Lee, "On oxygen deficiency and fast transient charge-trapping effects in high-κ dielectrics," *IEEE Electron Device Letters,* vol. 27, pp. 984-987, 2006.

[15] J. F. Zhang, C. Z. Zhao, M. B. Zahid, G. Groeseneken, R. Degraeve, and S. De Gendt, "An Assessment of the Location of As-Grown Electron Traps in $HfO_2$/HfSiO Stacks," *IEEE Electron Device Letters,* vol. 27, pp. 817-820, 2006.

[16] J. Robertson, K. Xiong, and S. J. Clark, "Band gaps and defect levels in functional oxides," *Thin Solid Films,* vol. 496, pp. 1-7, 2006.

[17] R. Degraeve, F. Crupi, D. H. Kwak, and G. Groeseneken, "On the defect generation and low voltage extrapolation of $Q_{BD}$ in $SiO_2$/$HfO_2$ stacks," in *2004 VLSI Techology Symposium*, 2004, pp. 140-141.

[18] J. H. Sim, R. Choi, Y. H. Lee, C. Young, P. Zeitzoff, D. L. Kwong, and G. Bersuker, "Trapping/de-trapping gate bias dependence of Hf-silicate dielectrics with poly and TiN gate electrode," *Jap. J. of Applied Physics Part 1-Regular Papers Short Notes & Review Papers,* vol. 44, pp. 2420-2423, Apr 2005.

[19] J. H. Sim, B. H. Lee, R. Choi, S. C. Song, and G. Bersuker, "Hot carrier degradation of HfSiON gate dielectrics with TiN electrode," *IEEE Transactions on Device and Materials Reliability,* vol. 5, pp. 177-182, Jun 2005.

[20] G. Bersuker, J. H. Sim, C. S. Park, C. D. Young, S. Nadkarni, R. Choi, and B. H. Lee, "Intrinsic Threshold Voltage Instability of the $HfO_2$ NMOS Transistors," in *International Reliability Physics Symposium*, 2006, pp. 179-183.

[21] G. Bersuker, J. H. Sim, C. D. Young, R. Choi, B. H. Lee, P. Lysaght, G. A. Brown, P. Zeitzoff, M. Gardner, R. W. Murto, and H. R. Huff, "Effects of Structural Properties of Hf-Based Gate Stack on Transistor Performance," in *2004 Spring Meeting of the Material Research Society*, 2004, pp. 31-35.

[22] G. Bersuker, J. H. Sim, C. D. Young, R. Choi, P. M. Zeitzoff, G. A. Brown, B. H. Lee, and R. W. Murto, "Effect of pre-existing defects on reliability assessment of high-κ gate dielectrics," *Microelectronics Reliability,* vol. 44, pp. 1509-1512, Sep-Nov 2004.

[23] R. Choi, B. H. Lee, C. D. Young, J. H. Sim, and G. Bersuker, "Temperature effects of constant bias stress on n-channel FETs with Hf-based gate dielectric," *Jap. J. of Applied Physics Part 1-Regular Papers Short Notes & Review Papers,* vol. 44, pp. 2201-2204, Apr 2005.

[24] R. Choi, S. Rhee, J. C. Lee, B. H. Lee, and G. Bersuker, "Charge trapping and detrapping characteristics in hafnium silicate gate stack under

static and dynamic stress," *IEEE Electron Device Letters,* vol. 26, pp. 197-199, 2005.

[25] R. Choi, C. D. Young, G. Bersuker, B. Hun Lee, and Y. Zhao, "Characterization and reliability measurement issues in devices with novel gate stack devices," *Thin Solid Films,* vol. 504, pp. 223-226, 2006.

[26] E. P. Gusev and C. P. D. Emic, "Charge detrapping in $HfO_2$ high-κ gate dielectric stacks," *Applied Physics Letters,* vol. 83, pp. 5223-5225, 2003.

[27] H. R. Harris, R. Choi, B. H. Lee, C. D. Young, J. H. Sim, K. Mathews, P. Zeitzoff, P. Majhi, and G. Bersuker, "Comparison of NMOS and PMOS stress for determining the source of NBTI TiN/HfSiON devices," in *43rd Annual IEEE Intl. Reliability Physics Symp. Proc.*, 2005, pp. 80-83.

[28] T. Kauerauf, R. Degraeve, F. Crupi, B. Kaezer, G. Groeseneken, and H. Maes, "Trap generation and progressive wearout in thin HfSiON," in *43rd Annual IEEE Intl. Reliability Physics Symp. Proc*, 2005, pp. 45-49.

[29] T. Kauerauf, R. Degraeve, E. Cartier, B. Govoreanu, P. Blomme, B. Kaczer, L. Pantisano, A. Kerber, and G. Groeseneken, "Towards understanding degradation and breakdown of $SiO_2$/high-k stacks," in *IEEE Intl. Electron Devices Meeting Tech. Digest*, 2002, pp. 521-524.

[30] A. Kerber, E. Cartier, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke, "Characterization of the $V_T$ instability in $SiO_2/HfO_2$ gate dielectrics," in *41st Annual IEEE Intl. Reliability Physics Symp. Proc.*, 2003, pp. 41-45.

[31] A. Kerber, E. Cartier, L. A. Ragnarsson, M. Rosmeulen, L. Pantisano, R. Degraeve, Y. Kim, and G. Groeseneken, "Direct measurement of the inversion charge in MOSFETs: application to mobility extraction in alternative gate dielectrics," in *VLSI Symposium Technical Digest*, 2003, pp. 159-160.

[32] J. Mitard, X. Garros, L. P. Nguyen, C. Leroux, G. Ghibaudo, F. Martin, and G. Reimbold, "Large-scale Time Characterization and Analysis of PBTI in $HfO_2$/Metal Gate Stacks," in *International Reliability Physics Symposium*, 2006, pp. 174-178.

[33] C. D. Young, R. Choi, J. H. Sim, B. H. Lee, P. Zeitzoff, Y. Zhao, K. Matthews, G. A. Brown, and G. Bersuker, "Interfacial layer dependence of $HfSi_xO_y$ gate stacks on $V_t$ instability and charge trapping using ultra-short pulse in characterization," in *43rd Annual IEEE Intl. Reliability Physics Symp. Proc.*, 2005, pp. 75-79.

[34] C. D. Young, D. Heh, S. V. Nadkarni, R. Choi, J. J. Peterson, J. Barnett, B. H. Lee, and G. Bersuker, "Electron Trap Generation in High-κ Gate Stacks by Constant Voltage Stress," *IEEE Transactions on Device and Materials Reliability,* vol. 6, pp. 123-131, 2006.

[35] C. D. Young, S. Nadkarni, D. Heh, H. R. Harris, R. Choi, J. J. Peterson, J. H. Sim, S. A. Krishnan, J. Barnett, E. Vogel, B. H. Lee, P. Zeitzoff, G. A. Brown, and G. Bersuker, "Detection of Electron Trap Generation Due to Constant Voltage Stress on High-κ Gate Stacks," in *International Reliability Physics Symposium*, 2006, pp. 169-173.

[36] S. A. Krishnan, J. J. Peterson, C. D. Young, G. Brown, R. Choi, R. Harris, J. H. Sim, P. Zeitzoff, P. Kirsch, J. Gutt, H. J. Li, K. Matthews, J. C. Lee, B. H. Lee, and G. Bersuker, "Dominant SILC mechanisms in HfO2/TiN gate nMOS and pMOS transistors," in *43rd Annual IEEE Intl. Reliability Physics Symp. Proc*, 2005, pp. 642-643.

[37] B. H. Lee, C. D. Young, R. Choi, J. H. Sim, G. Bersuker, C. Y. Kang, R. Harris, G. A. Brown, K. Matthews, S. C. Song, N. Moumen, J. Barnett, P. Lysaght, K. S. Choi, H. C. Wen, C. Huffman, H. Alshareef, P. Majhi, S. Gopalan, J. J. Peterson, P. Kirsh, H.-J. Li, J. Gutt, M. Gardner, H. R. Huff, P. Zeitzoff, R. W. Murto, L. Larson, and C. Ramiller, "Intrinsic Characteristics of High-k Devices and Implications of Fast Transient Charging Effects (FTCE)," in *IEEE Intl. Electron Devices Meeting Tech. Digest*, 2004, pp. 859-862.

[38] C. L. Cheng, K. S. Chang-Liao, C. H. Huang, and T. K. Wang, "Effects of HfOxNy gate-dielectric nitrogen concentration on the charge trapping properties of metal-oxide-semiconductor devices," *Japanese Journal of Applied Physics Part 2-Letters & Express Letters,* vol. 43, pp. L1181-L1183, Sep 2004.

[39] J. A. Felix, M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, P. E. Dodd, E. P. Gusev, R. M. Fleming, and C. D'Emic, "Charge trapping and annealing in high-kappa gate dielectrics," *Ieee*

*Transactions on Nuclear Science,* vol. 51, pp. 3143-3149, Dec 2004.

[40] J. H. Kim, K. J. Choi, and S. G. Yoon, "Electrical and reliability characteristics of HfO2 gate dielectric treated in N-2 and NH3 plasma atmosphere," *Applied Surface Science,* vol. 242, pp. 313-317, Apr 2005.

[41] Y. Liu, A. Shanware, L. Colombo, and R. Dutton, "Modeling of charge trapping induced threshold-voltage instability in high-kappa gate dielectric FETs," *Ieee Electron Device Letters,* vol. 27, pp. 489-491, Jun 2006.

[42] R. O'Connor, G. Hughes, R. Degraeve, and B. Kaczer, "Charge trapping in MOSFETs with HfSiON dielectrics during electrical stressing," *Microelectronic Engineering,* vol. 77, pp. 302-309, Apr 2005.

[43] R. O'Connor, G. Hughes, R. Degraeve, B. Kaczer, and T. Kauerauf, "Reliability of HfSiON gate dielectrics," *Semiconductor Science and Technology,* vol. 20, pp. 68-71, Jan 2005.

[44] H. Wong, N. Zhan, K. L. Ng, M. C. Poon, and C. W. Kok, "Interface and oxide traps in high-kappa hafnium oxide films," *Thin Solid Films,* vol. 462-63, pp. 96-100, Sep 2004.

[45] K. Xiong, J. Robertson, and S. J. Clark, "Defect energy states in high-K gate oxides," *Physica Status Solidi B-Basic Solid State Physics,* vol. 243, pp. 2071-2080, Jul 2006.

[46] S. Zafar, A. Kumar, E. Gusev, and E. Cartier, "Threshold voltage instabilities in high-κ gate dielectric stacks," *IEEE Transactions on Device and Materials Reliability,* vol. 5, pp. 45-64, 2005.

[47] C.-T. Chan, C.-J. Tang, T. Wang, H. C.-H. Wang, and D. D. Tang, "Characteristics and physical mechanisms of positive bias and temperature stress-induced drain current degradation in HfSiON nMOSFETs," *IEEE Transactions on Electron Devices* vol. 54, pp. 1340-1346, 2006.

[48] J. A. Felix, J. R. Schwank, D. M. Fleetwood, M. R. Shaneyfelt, and E. P. Gusev, "Effects of radiation and charge trapping on the reliability of high-kappa gate dielectrics," *Microelectronics Reliability,* vol. 44, pp. 563-575, Apr 2004.

[49] S. Hall, O. Buiu, and L. Yi, "Direct observation of anomalous positive charge and electron-trapping dynamics in high-k films using pulsed-MOS-capacitor measurements " *IEEE Transactions on Electron Devices,* vol. 54, pp. 272-278, 2007.

[50] D. Heh, C. D. Young, and G. Bersuker, "Experimental Evidence of the Fast and Slow Charge Trapping/Detrapping Processes in High-k Dielectrics Subjected to PBTI Stress," *IEEE Electron Device Letters,* vol. 29, pp. 180-182, 2008.

[51] C. Y. Kang, R. Choi, S. C. Song, C. D. Young, G. Bersuker, B. H. Lee, and J. C. Lee, "Carrier recombination in high-k dielectrics and its impact on transient charge effects in high-k devices," in *Proceedings of the 44th Annual IEEE International Reliability Physics Symposium* San Jose, CA, 2006.

[52] C. Y. Kang, J. C. Lee, R. Choi, S. C. Song, C. D. Young, G. Bersuker, and B. H. Lee, "Transient bicarrier response in high-k dielectrics and its impact on transient charge effects in high-k complementary metal oxide semiconductor devices," *Applied Physics Letters,* vol. 88, p. 162905, 2006.

[53] Y. Lu, S. Hall, O. Buiu, and J. F. Zhang, "Real-time observation of charging dynamics in hafnium silicate films using MOS capacitance transients," *Microelectronic Engineering,* vol. 84, pp. 2390-2393, 2007.

[54] G. Puzzilli and F. Irrera, "Long time transients in hafnium oxide " *Microelectronic Engineering,* vol. 84, pp. 2394-2397, 2007.

[55] M. Rafik, X. Garros, G. Ribes, G. Ghibaudo, C. Hobbs, A. Zauner, M. Muller, V. Huard, and C. Ouvard, "Impact of TiN metal gate on NBTI assessed by interface states and fast transient effect characterization," in *IEEE International Electron Devices Meeting* Washington, DC, 2007, pp. 812-815.

[56] G. Reimbold, J. Mitard, M. Casse, X. Garros, C. Leroux, L. Thevenod, and F. Martin, "Electrical characterization of high K devices: Charges and traps effects on instability, reliability and mobility behaviour," in *207th Electrochemical Society Meeting*, 2005.

[57] G. Reimbold, J. Mitard, X. Garros, C. Leroux, G. Ghibaudo, and F. Martin, "Initial and PBTI-induced traps and charges in Hf-based oxides/TiN stacks " *Microelectronics Reliability,* vol. 47, pp. 489-496 2007.

[58] K. M. F. Shahil, M. N. Arafat, Q. D. M. Khosru, and M. R. Khan, "Quantum mechanical modeling

of charge trapping/detrapping phenomena in CMOS structures with high-K dielectric " in *4th International Conference on Electrical and Electronics Engineering* Mexico City, Mexico 2007, pp. 349-352.

[59] K. M. F. Shahil, M. N. Arafat, Q. D. M. Khosru, and M. R. Khan, "Study of charge trapping/ detrapping mechanism in $SiO_2/HfO_2$ stack gate dielectrics considering two-way detrapping," in *International Workshop on Electron Devices and Semiconductor Technology*, Beijing, China, 2007, pp. 117-120

[60] X. Yu, M. Yu, and C. Zhu, "The role of Nitrogen on charge-trapping-induced Vth instability in HfAION high-K gate dielectric with metal and poly-Si gate electrodes," *IEEE Transactions on Electron Devices,* vol. 54, pp. 1972-1977, 2007.

[61] Y. Zhao, C. D. Young, R. Choi, and B. H. Lee, "Pulsed characterization techniques capture high-k charge trapping behavior," *Semiconductor International,* vol. 29, pp. 47-51, 2006.

[62] Y. Zhao, C. D. Young, M. Pendley, K. Matthews, B. H. Lee, and G. A. Brown, "Effective Minimization of Charge Trapping in High-k Gate Dielectrics with an Ultra-Short Pulse Technique," in *Intl. Conf. on Solid State and Integrated Circuit Technology*, 2004, p. 407.

[63] W. Zhu, J.-P. Han, and T. P. Ma, "Mobility Measurements and Degradation Mechanisms of MOSFETs Made With Ultrathin High-k Dielectrics," *IEEE Transactions on Electron Devices,* vol. 51, pp. 98-105, 2004.

[64] W. J. Zhu and T. P. Ma, "Temperature dependence of channel mobility in $HfO_2$-gated NMOSFETs," *IEEE Electron Device Letters,* vol. 25, pp. 89-91, 2004.

[65] C. D. Young, D. Heh, A. Neugroschel, R. Choi, B. H. Lee, and G. Bersuker, "Electrical Characterization and Analysis Techniques for the High-k Era," *Microelectronics Reliability,* vol. 47, pp. 479–488, 2007.

[66] P. D. Kirsch, J. H. Sim, S. C. Song, S. Krishnan, J. J. Peterson, H.-J. Li, M. Quevedo-Lopez, C. D. Young, R. Choi, N. Moumen, P. Majhi, Q. Wang, J. G. Ekerdt, G. Bersuker, and B. H. Lee, "Mobility Enhancement of High-κ Gate Stacks Through Reduced Transient Charging," in *35th Annual European Solid-State Device Research Conference*, Grenoble, France, 2005, pp. 367-370.

[67] A. Morioka, H. Watanabe, M. Miyamura, T. Tatsumi, M. Saitoh, T. Ogura, T. Iwamoto, T. Ikarashi, Y. Saito, Y. Okada, Y. Mochiduki, and T. Mogami, "High mobility MISFET with low trapped charge in HfSiO films," in *VLSI Symposium Technical Digest*, 2003, pp. 165-166.

[68] M. A. Quevedo-Lopez, S. A. Krishnan, P. D. Kirsch, H.-J. Li, J. H. Sim, C. Huffman, J. J. Peterson, B. H. Lee, G. Pant, B. E. Gnade, M. J. Kim, R. M. Wallace, D. Guo, H. Bu, and T. P. Ma, "High Performance Gate First HfSiON Dielectric Satisfying 45 nm Node Requirements," in *IEEE Intl. Electron Devices Meeting Tech. Digest*, 2005, pp. 437-440.

[69] J. H. Sim, S. C. Song, P. D. Kirsch, C. D. Young, R. Choi, D. L. Kwong, B. H. Lee, and G. Bersuker, "Effects of ALD HfO2 thickness on charge trapping and mobility," *Microelectronic Engineering,* vol. 80, pp. 218-221, Jun 2005.

[70] C. Leroux, J. Mitard, G. Ghibaudo, X. Garros, G. Reimbold, B. Guillaumor, and F. Martin, "Characterization and modeling of hysteresis phenomena in high K dielectrics," in *IEEE Intl. Electron Devices Meeting Tech. Digest*, 2004, pp. 737-740.

[71] C. Shen, M. F. Li, X. P. Wang, Y. Yee-Chia, and D. L. Kwong, "A fast measurement technique of MOSFET $I_d$-$V_g$ characteristics," *IEEE Electron Device Letters,* vol. 27, pp. 55-57, 2006.

[72] C. D. Young, Y. G. Zhao, M. Pendley, B. H. Lee, K. Matthews, J. H. Sim, R. Choi, G. A. Brown, R. W. Murto, and G. Bersuker, "Ultra-short pulse current-voltage characterization of the intrinsic characteristics of high-kappa devices," *Jap. J. of Applied Physics Part 1-Regular Papers Short Notes & Review Papers,* vol. 44, pp. 2437-2440, Apr 2005.

[73] C. D. Young, Y. Zhao, D. Heh, R. Choi, B. H. Lee, and G. Bersuker, "Pulsed $I_d$-$V_g$ Methodology and Its Application to Electron-Trapping Characterization and Defect Density Profiling," *IEEE Transactions on Electron Devices,* vol. 56, pp. 1322-1329, 2009.

[74] G. Bersuker, J. Sim, C. S. Park, C. D. Young, S. Nadkarni, C. Rino, and L. Byoung Hun, "Mechanism of Electron Trapping and Characteristics of Traps

in $HfO_2$ Gate Stacks," *IEEE Transactions on Device and Materials Reliability,* vol. 7, pp. 138-145, 2007.

[75] R. Degraeve, A. Kerber, P. Roussell, E. Cartier, T. Kauerauf, L. Pantisano, and G. Groeseneken, "Effect of bulk trap density on $HfO_2$ reliability and yield," in *IEEE Intl. Electron Devices Meeting Tech. Digest*, 2003, pp. 935-938.

[76] C. D. Young, G. Bersuker, G. A. Brown, P. Lysaght, P. Zeitzoff, R. W. Murto, and H. R. Huff, "Charge trapping and device performance degradation in MOCVD hafnium-based gate dielectric stack structures," in *42nd Annual IEEE Intl. Reliability Physics Symp. Proc*, 2004, pp. 597-598.

[77] G. Ribes, M. Muller, S. Bruyere, D. Roy, M. Denais, V. Huard, T. Skotnicki, and G. Ghibaudo, "Characterization of Vt instability in hafnium based dielectrics by pulse gate voltage techniques," in *European Solid-State Device Research Conference*, 2004, pp. 89-92.

[78] L. Pantisano, E. Cartier, A. Kerber, R. Degraeve, M. Lorenzini, M. Rosmeulen, G. Groeseneken, and H. E. Maes, "Dynamics of threshold voltage instability in stacked high-k dielectrics: role of the interfacial oxide," in *VLSI Symposium Technical Digest*, 2003, pp. 163-164.

[79] C. D. Young, P. Zeitzoff, G. A. Brown, G. Bersuker, L. Byoung Hun, and J. R. Hauser, "Intrinsic mobility evaluation of high-κ gate dielectric transistors using pulsed $I_d$-$V_g$," *IEEE Electron Device Letters,* vol. 26, pp. 586-589, 2005.

[80] K. A. Jenkins, J. Y.-C. Sun, and J. Gautier, "Characteristics of SOI FET's under pulsed conditions," *IEEE Transactions on Electron Devices,* vol. 44, pp. 1923-1930, 1997.

[81] D. Heh, C. D. Young, R. Choi, and G. Bersuker, "Extraction of the Threshold Voltage Shift by the Single Pulse Technique," *IEEE Electron Device Letters,* vol. 28, pp. 734-736, 2007.

[82] S. C. Song, Z. Zhang, C. Huffman, S. H. Bae, J. H. Sim, P. Kirsch, P. Majhi, N. Moumen, and B. H. Lee, "Integration issues of high-k and metal gate into conventional CMOS technology," *Thin Solid Films* vol. 504, pp. 170-173, 2006.

[83] G. Bersuker, P. Zeitzoff, J. H. Sim, B. H. Lee, R. Choi, G. Brown, and C. D. Young, "Mobility evaluation in transistors with charge-trapping gate dielectrics," *Applied Physics Letters,* vol. 87, p. 042905, Jul 2005.

[84] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, "Review on high-κ dielectrics reliability issues," *IEEE Transactions on Device and Materials Reliability,* vol. 5, pp. 5-19, 2005.

[85] A. Kerber, E. Cartier, L. Pantisano, R. Degraeve, T. Kauerauf, Y. Kim, A. Hou, G. Groeseneken, H. E. Maes, and U. Schwalke, "Origin of the threshold voltage instability in $SiO_2$/$HfO_2$ dual layer gate dielectrics," *IEEE Electron Device Letters,* vol. 24, pp. 87-89, Feb 2003.

[86] T. Yang, M. F. Li, C. Shen, C. H. Ang, Z. Chunxiang, Y. C. Yeo, G. Samudra, S. C. Rustagi, and M. B. Yu, "Fast and slow dynamic NBTI components in p-MOSFET with SiON dielectric and their impact on device life-time and circuit application," in *VLSI Symposium Technical Digest*, 2005, pp. 92-93.

[87] D. Heh, R. Choi, and G. Bersuker, "Comparison of On-The-Fly, DC $I_d$-$V_g$, and Single-Pulse Methods for Evaluating Threshold Voltage Instability in High-κ nMOSFETs," *IEEE Electron Device Letters,* vol. 28, pp. 245-247, 2007.

[88] D. Heh, R. Choi, C. D. Young, B. H. Lee, and G. Bersuker, "A Novel Bias Temperature Instability Characterization Methodology for High-κ nMOSFETs," *IEEE Electron Device Letters,* vol. 27, pp. 849-851, 2006.

[89] B. H. Lee, R. Choi, J. H. Sim, S. A. Krishnan, J. J. Peterson, G. A. Brown, and G. Bersuker, "Validity of constant voltage stress based reliability assessment of high-κ devices," *IEEE Transactions on Device and Materials Reliability,* vol. 5, pp. 20-25, Mar 2005.

[90] C. Shen, T. Yang, M. F. Li, X. Wang, C. E. Foo, G. S. Samudra, Y. C. Yeo, and D. L. Kwong, "Fast $V_{th}$ Instability in $HfO_2$ Gate Dielectric MOSFETs and Its Impact on Digital Circuits," *IEEE Transactions on Electron Devices,* vol. 53, pp. 3001-3011, 2006.

[91] G. Bersuker, P. Zeitzoff, J. H. Sim, B. H. Lee, R. Choi, G. A. Brown, and C. D. Young, "Mobility Evaluation in High-K Devices," in *IEEE Intl. Integrated Reliability Workshop Final Report*, 2004, pp. 141-144.

[92] G. Bersuker, J. Barnett, N. Moumen, B. Foran, C. D.

Young, P. Lysaght, J. Peterson, B. H. Lee, P. M. Zeitzoff, and H. R. Huff, "Interfacial layer-induced mobility degradation in high-k transistors," *Jap. J. of Applied Physics Part 1-Regular Papers Short Notes & Review Papers,* vol. 43, pp. 7899-7902, Nov 2004.

[93] G. Bersuker, C. S. Park, J. Barnett, P. S. Lysaght, P. D. Kirsch, C. D. Young, R. Choi, B. H. Lee, B. Foran, K. v. Benthem, S. J. Pennycook, P. M. Lenahan, and J. T. Ryan, "The effect of interfacial layer properties on the performance of Hf-based gate stack devices," *Journal of Applied Physics,* vol. 100, p. 094108, 2006.

[94] C. D. Young, A. Kerber, T. H. Hou, E. Cartier, G. A. Brown, G. Bersuker, Y. Kim, J. Gutt, P. Lysaght, J. Bennett, C. H. Lee, S. Gopalan, M. Gardner, P. M. Zeitzoff, G. Groeseneken, R. W. Murto, and H. R. Huff, "Charge Trapping and Mobility Degradation in MOCVD Hafnium Silicate Gate Dielectric Stack Structures," in *203rd Fall Meeting of the Electrochemical Society, Physics and Technology of High-K Gate Dielectrics - II*, Orlando, FL, 2003, pp. 347-362.

[95] R. G. Southwick and W. B. Knowlton, "Stacked Dual Oxide MOS Energy Band Diagram Visual Representation Program," *IEEE Transactions on Device and Materials Reliability,* vol. 6, pp. 136-145, 2006.

[96] M. A. Negara, K. Cherkaoui, P. K. Hurley, C. D. Young, P. Majhi, W. Tsai, D. Bauza, and G. Ghibaudo, "Analysis of electron mobility in $HfO_2$/TiN gate metal-oxide-semiconductor field effect transistors: The influence of $HfO_2$ thickness, temperature, and oxide charge," *Journal of Applied Physics,* vol. 105, p. 024510, 2009.

[97] M. A. Negara, K. Cherkaoui, P. Majhi, C. D. Young, W. Tsai, D. Bauza, G. Ghibaudo, and P. K. Hurley, "The influence of HfO2 film thickness on the interface state density and low field mobility of n channel HfO2/TiN gate MOSFETs," *Microelectronic Engineering,* vol. 84, pp. 1874-1877, 2007.

[98] D. V. Singh, P. Solomon, E. P. Gusev, G. Singco, and Z. Ren, "Ultra-fast Measurements of the Inversion Charge in MOSFETs and Impact on Measured Mobility in High-k MOSFETs," in *IEEE Intl. Electron Devices Meeting Tech. Digest*, San Francisco, CA, 2004, pp. 863-866.

[99] J. R. Hauser and K. Ahmed, "Characterization of Ultrathin Oxides Using Electrical C-V and I-V Measurements," in *Intl. Conf. on Characterization and Metrology for ULSI Technology*, 1998, pp. 235-239.

[100] J. R. Hauser, "Extraction of experimental mobility data for MOS devices," *IEEE Transactions on Electron Devices,* vol. 43, pp. 1981-1988, Nov 1996.

[101] C. D. Young, P. Zeitzoff, G. Bersuker, and R. Choi, "Comparison of Trap-free Mobility Extraction Techniques for High-κ Gate Dielectrics," in *International Workshop on Electrical Characterization and Reliability for High-κ Devices*, 2004, pp. 73-81.

[102] G. Bersuker, P. Zeitzoff, J. Barnett, N. Moumen, B. Foran, C. D. Young, J. J. Peterson, and P. Lysaght, "Interface-Induced Mobility Degradation in High-k Transistors," *Japanese Journal of Applied Physics,* vol. 43, pp. 7899-7902, 2004.

[103] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake, and N. Fukushima, "Additional Scattering Effects for Mobility Degradation in Hf-silicate Gate MISFETs," in *IEEE Intl. Electron Devices Meeting Tech. Digest*, 2002, pp. 621-624.

[104] R. Choi, S. C. Song, C. D. Young, G. Bersuker, and B. H. Lee, "Charge trapping and detrapping characteristics in hafnium silicate gate dielectric using an inversion pulse measurement technique," *Applied Physics Letters,* vol. 87, p. 122901, Sep 2005.

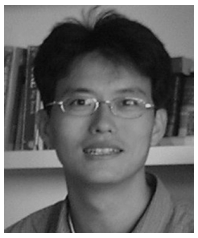
[105] B. H. Lee, C. Young, R. Choi, J. H. Sim, and G. Bersuker, "Transient charging and relaxation in high-k gate dielectrics and their implications," *Jap. J. of Applied Physics Part 1-Regular Papers Short Notes & Review Papers,* vol. 44, pp. 2415-2419, Apr 2005.

[106] G. Ribes, M. Rafik, and D. Roy, "Reliability issues for nano-scale CMOS dielectrics," *Microelectronic Engineering,* vol. 84, pp. 1910-1916, 2007.

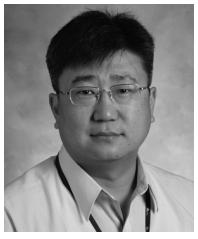
[107] M. Denais, C. Parthasarathy, G. Ribes, Y. Rey-Tauriac, N. Revil, A. Bravaix, V. Huard, and F. Perrier, "On-the-fly characterization of NBTI in ultra-thin gate oxide PMOSFET's," in *IEEE Intl. Electron Devices Meeting Tech. Digest*, 2004, pp. 109-112.

**Chadwin D. Young** received his B.S. degree in Electrical Engineering from the University of Texas at Austin in 1996. He then went on to receive a M.S. and Ph.D. from the North Carolina State University in 1998 and 2004, respectively. He has held several internships during this time until 2001 when he joined SEMATECH. Here, he completed his dissertation research on high-k gate stacks. He now continues this research at SEMATECH as a project engineer working on electrical characterization and reliability methodologies for the evaluation of high-k gate stacks, and has authored or co-authored 150+ journal and conference papers. He is currently serving on the management committee of the 2010 International Integrated Reliability Workshop as the General Chair, and as a Guest Editor for IEEE Transactions on Device and Materials Reliability.

**Dawei Heh** received his B.S. in Physics from National Taiwan University, Taiwan in 1996. He received his M.S. and Ph. D. in Electrical Engineering from the University of Maryland at College Park, Maryland in 2001 and 2005, respectively. He worked in the CMOS and Novel Devices Group at NIST on studying reliability and breakdown mechanisms of ultra-thin dielectrics when he was pursuing his Ph. D. degree. He worked as a research engineer in the electrical characterization and reliability group at SEMATECH from 2005 to 2009 and now he works with National Nano Device Laboratories (NDL) in Taiwan. His research includes characterization and development of new measurement techniques for high-k, memory, high-speed channel, and non-planner devices etc. He is also working on the simulation of electrical characteristics of high-speed channel devices.



**Rino Choi** received his Bachelor of Science and Master of Science degree in the Department of Inorganic Materials Engineering of the Seoul National University in 1992 and 1994, respectively. He received the Ph.D. in Materials Science and Engineering Program in 2004 from the University of Texas at Austin. He worked for Daewoo Motors Company from 1994 to 1999, where he worked as a development and test engineer. Since 1999, he studied various high-k dielectrics and published more than 100 journal and conference papers. After his completion of his Ph.D, he worked on the electrical characterization and reliability of advanced gate stacks at SEMATECH. Since September, 2007, he is with the School of Materials Science and Engineering, Inha University, Korea.



**Byoung Hun Lee** received a B.S. (1989) and a M.S. (1992) in Physics from Korea Advanced Institute of Science and Technology and Ph.D (2000) in electrical and computer engineering from the University of Texas at Austin. He worked at Samsung semiconductor (1992-1997), IBM (2001-2007) and SEMATECH (2007-2008). He has authored and co-authored more than 350 journal and conference papers in the various semiconductor research areas including NEMS, gate oxide reliability, SOI device and process, strained silicon devices, and high-κ/ metal gate process and devices. In 2008, he joined the department of Nanobio Materials and Electronics at Gwangju Institute of Science and Technology. His current research interest includes NEMS-CMOS hybrid technology, extreme low power technology, graphene process and gate stack technology.

**Gennadi Bersuker** completed his M.S. and Ph.D. in Physics at the Leningrad State University and Kishinev State University, respectively. After graduation, he joined Moldavian Academy of Sciences, and then worked at Leiden University and the University of Texas at Austin. Since 1994, he has been working at SEMATECH on electrical characterization of Cu/low-k interconnect, high-k gate stacks and advanced CMOS process development. He has been involved in organizing, chairing, or serving as a committee member in a number of technical conferences, including IRW, IRPS, IEDM, ULSI-TFT, ISAGST, LEC, NGCM, APS. He is a SEMATECH Fellow and has published over 200 papers on the electronic properties of dielectrics and semiconductor processing and reliability.