Metal Insulator Gate Geometric HEMT: Novel Attributes and Design Consideration for High Speed Analog Applications

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***Abstract*—Improvement in breakdown voltage (BV_{ds}) and speed of the device are the key issues among the researchers for enhancing the performance of HEMT. Increased speed of the device aspires for shortened gate length (L_g), but due to lithographic limitation, shortening L_g below sub-micrometer requires the inclusion of various metal-insulator geometries like T-gate onto the conventional architecture. It has been observed that the speed of the device can be enhanced by minimizing the effect of upper gate electrode on device characteristics, whereas increase in the BV_{ds} of the device can be achieved by considering the finite effect of the upper gate electrode. Further, improvement in BV_{ds} can be obtained by applying field plates, especially at the drain side. The important parameters affecting BV_{ds} and cut-off frequency (f_T) of the device are the length, thickness, position and shape of metal-insulator geometry. In this context, intensive simulation work with analytical analysis has been carried out to study the effect of variation in length, thickness and position of the insulator under the gate for various metal-insulator gate geometries like T-gate, Γ-gate, Step-gate etc., to anticipate superior device performance in conventional HEMT structure.**

***Index Terms*—InAlAs/InGaAs HEMT, metal-insulator geometries, breakdown voltage, cut-off frequency and maximum frequency of oscillations**

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I. INTRODUCTION

High electron mobility transistors (HEMTs) consisting of InAlAs/InGaAs heterostructure, lattice matched to InP show promising characteristics due to its large conduction band discontinuity [1] and a large Γ-L valley separation [2]. However, some analog applications of HEMTs are still limited by the reduced breakdown voltage of these devices, which limits their power applications. In general, this problem is related to the properties of InAlAs/InGaAs material systems, in particular due to enhanced impact ionization effects in the narrow bandgap (0.73 eV) of $In_{0.53}Ga_{0.47}As$ or tunneling due to low Schottky barrier height (0.66 eV) of $In_{0.52}Al_{0.48}As$ [3-10]. Thus, ever since its development, significant efforts have been made to improve the speed and breakdown voltage of the device.

The speed of the device can be improved by shortening the gate length (L_g), but shortening the L_g below sub-micrometer range requires various complex lithographic techniques [11-22]. This state-of-art performance requires careful attention to the technological details of gate formation, layer design, and MBE growth by multilevel resist process using e-beam lithography forming various metal insulator geometries like T-gate, Γ-gate etc. These geometries are usually fabricated in such a way that the device performance is mainly affected by the lower part of the T-gate geometry as shown in Fig. 1 with negligible effect of upper part for enhanced performance.

High breakdown voltage (BV_{ds}) is amongst the

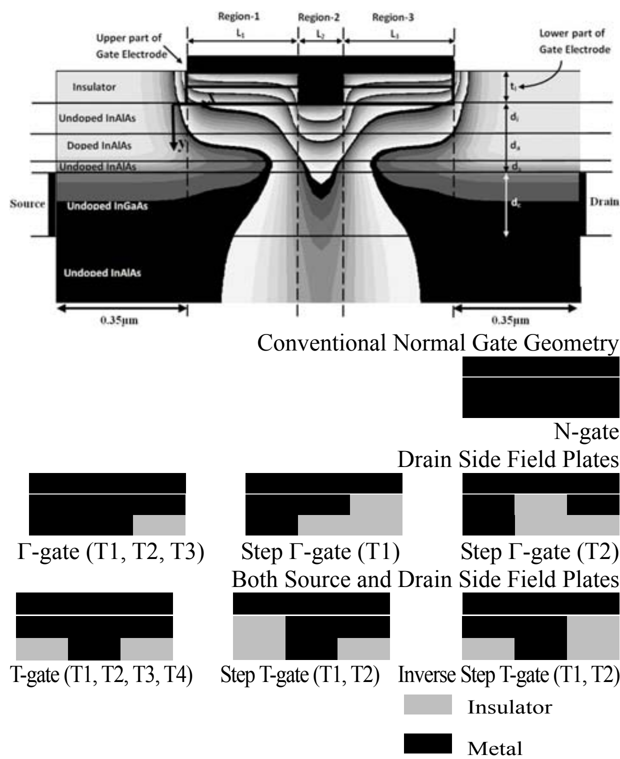

Fig. 1. Cross-sectional view of different Metal-Insulator Geometric Pulsed doped High Electron Mobility Transistor acting field plates of different shapes on drain side and on both source and drain side.

primary requirements for achieving higher device reliability and the essence of achieving this in HEMT is to have an increasing depletion width at the surface of the channel from the drain to the Schottky gate. This increase in depletion depth can be accounted in terms of additional charges trapped at the surface of the channel, resulting in a lower electric field peak at the drain-side-edge of the gate and hence, higher BV_{ds}. By considering the finite effect of upper gate electrode as shown in Fig.1 on the device characteristics as in Field Plates (FP) between gate-drain spacing (Γ-gate) (which is usually ignored in T-gate geometries with passivation layer), increase in BV_{ds} [23-30] can be seen owing to increase in depletion depth as a combined effect of both the upper gate electrode and the lower gate in T-gate geometry.

Inclusion of FP modulates the electric field profile in such a way that three peaks are obtained in various Γ-gate instead of two peaks as in normal gate device due to the effect of different region of gate in Γ-gate geometry as shown in Fig. 1 with lower electric field peak in the region near the drain end. But this additional depletion region formed at the surface of the channel due to trapped charges leads to increase in gate-drain capacitance and channel resistance thereby reducing the gain/cut-off frequency (f_T) of the device. Thus, to have desired characteristics without the emergence of these anomalies, the effect of upper part of the gate should be negligible [23-30], thereby showing a trade-off between the emergence of gate-drain capacitance and channel resistance and the increased breakdown voltage. Device optimization is thus required to tailor the field profile to improve the BV_{ds} and f_T of the device.

The important parameters affecting BV_{ds} and f_T of the device are the length, thickness, position and shape of metal-insulator geometry under the gate forming various metal-insulator gate geometries like T-gate, Γ-gate, Step-gate etc., with same lithographic length. All these parameter variations have been analyzed by performing analytical analysis supported by simulation work [31]. Generalized analytical models for HEMT [30, 32-34] have been used to obtain the analytical results for various metal-insulator geometries by considering different values of insulator thickness and permittivity in various regions of the device under consideration. Taking into account, the present lithographic scenario and controlled thermal reflow treatment [11] on multi-resist process for fabrication, a gate geometry has been considered, which upon playing with the insulator thickness and dielectric constant of the material forming the gate-dielectric system can give an account of various metal-insulator geometries in which the effect of FP can be made possible either on source side (SFP), or drain side (DFP) or on both source and drain end (BFP). Since, the electric field suppression at the drain end is the prime requirement for increased BV_{ds}, the electric field suppression using SFP is not desirable and hence only those geometries having DFP and BFP have been given extensive consideration in this work. Analytical analysis have been performed for DFP and BFP devices and characteristics like drain current (I_d), transconductance (g_m), total trans-capacitance (C_T), f_T and maximum frequency of oscillations (f_{max}) have been obtained to predict enhanced speed and reliability of the device in metal-insulator geometric HEMT in comparison to conventional HEMT structure.

II. THEORETICAL CONSIDERATIONS

The basic *HEMT* structure used in the analysis as

shown in Fig. 1 consists of undoped *InGaAs* layer to form the 2DEG channel; an *InAlAs* undoped spacer-layer of thickness d_s; a *Si*-doped *InAlAs* layer of thickness d_a to provide 2DEG sheet charge density; and an undoped *InAlAs* Schottky enhancement layer of thickness d_i. The gate geometry is such that the whole structure is divided into three regions -1, 2 and 3 respectively having different insulator (with permittivity ε_{Iz}) thicknesses (t_{Iz}) between gate and the semiconductor, where z = 1, 2 and 3 corresponding to region 1, 2 and 3 respectively. The comprehensive effect of the variation in the length, thickness and position of the insulator between the upper part of the gate electrode and the semiconductor giving rise to various innovative structures, have been studied and are shown in Fig. 1.

Generalized analytical model for HEMT [30, 32-34] has been used to obtain the analytical results. The expression of drain current in different region for different metal-insulator gate geometric HEMT is given by

$$I_{ds}\Big|_z = \frac{Wq\mu_o}{C_z B_z^{\,2}} \frac{\left(f\left[y(V_{1z})\right]-f\left[y(V_{0z})\right]\right)}{\left(L_z + \dfrac{\mu_o\left(V_{1z}-V_{oz}\right)}{v_{sat}}\right)} \quad (1)$$

Where $f(y) = A_z^{\,2} y + \dfrac{y^2}{2} + \dfrac{4A_z y^{3/2}}{3}$ and

$y(V_z) = \left(\beta_z k_2\right)^2 + 4\beta_z\left(1+\beta_z k_3\right)\left(V_{gs} - V_{off}\big|_z - k_1 - V_z - I_{ds}R_s\right)$

in which $A_z = -\beta_z k_2$, $B_z = 2\left(1+\beta_z k_3\right)$,

$C_z = -4\beta_z\left(1+\beta_z k_3\right)$, $\beta_z = \dfrac{\varepsilon_o.\varepsilon_S}{q\left(d_T + \dfrac{\varepsilon_S.t_{Iz}}{\varepsilon_{Iz}}\right)}$ and $V_{off}\big|_z$ is the threshold voltage and d_T (= $d_s + d_a + d_i$). The threshold voltage for planar doped/delta doped structure for different gate regions can be expressed as

$$V_{off}\Big|_z = \phi_b - \Delta E_c - \frac{q.N_d.d_a^{\,2}}{2.\varepsilon_o.\varepsilon_s}\left(1+\frac{2.d_i}{d_a}\right) - \frac{q.N_d.t_{Iz}.d_a}{\varepsilon_o.\varepsilon_{Iz}} \quad (2)$$

The gate to source capacitance and gate to drain capacitance obtained from the model can be represented as series and parallel combination of insulator capacitance (C_{I1}, C_{I2} and C_{I3}) and depletion capacitances (C_{R1}, C_{R2} and C_{R3}) in various regions as shown in Fig. 2 to obtain the resultant capacitance for various metal-insulator geometries under consideration. Using the

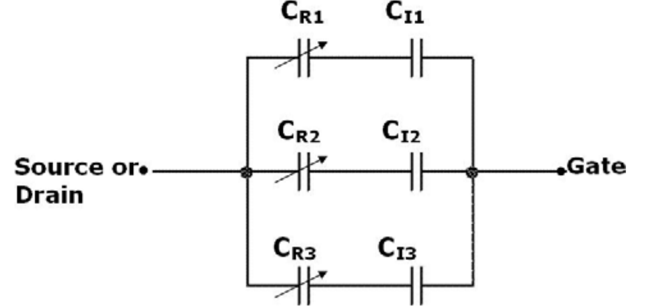

Fig. 2. The circuit representation of gate capacitance of different Metal-Insulator Geometric Pulsed doped High Electron Mobility Transistor.

drain current model evaluated in the above section, gate-source capacitance and gate-drain capacitance is calculated in various regions and is given by [30, 32-34]

$$C_{gs}\Big|_z = \frac{-q^2W^2\mu_o}{I_{ds}^{\,2}}\frac{\partial I_{ds}}{\partial V_{gs}}\Big|_{V_{gd}}\left(f_1\left[y(V_z)\right]-f_1\left[y(V_{z-1})\right]\right)-C.f_2\left[y(V_z)\right].dy_g(V_z)+C.f_2\left[y(V_{z-1})\right].dy_g(V_{z-1})$$

$$C_{gd}\Big|_z = \frac{-q^2W^2\mu_o}{I_{ds}^{\,2}}\frac{\partial I_{ds}}{\partial V_{gd}}\Big|_{V_{gs}}\left(f_1\left[y(V_z)\right]-f_1\left[y(V_{z-1})\right]\right)-C.f_2\left[y(V_z)\right].dy(dV_z)+C.f_2\left[y(V_{z-1})\right].dy(dV_{z-1}) \quad (3)$$

where $dy_g(V) = 1 - \dfrac{\partial V}{\partial V_{gs}}\Big|_{V_{gd}} - R_s\dfrac{\partial I_{ds}}{\partial V_{gs}}\Big|_{V_{gd}}$,

$dy(dV) = -dV - g_m R_s$ and

$$f_1(y) = \frac{1}{C_z B_z^{\,4}}\left(A_z^{\,4} y + \frac{8A_z^{\,3} y^{3/2}}{3} + 3A_z^{\,2} y^2 + \frac{8A_z y^{5/2}}{5} + \frac{y^3}{3}\right)$$

$$f_2(y) = \frac{qW\,n_s\big|_z}{C}\left(\frac{qW\,n_s\big|_z\,\mu_o}{I_{ds}} - \frac{1}{E_c}\right)$$

III. Device Realization and Characterization

Various proposed structures have been created by dividing the region between the gate and the high band gap semiconductor (*InAlAs*) into six different regions, rectangular in shape of dimensions $L_g/3 \times t_I$ where L_g is the gate length of the normal gate device and t_I is the thickness of the insulator. These regions are considered to be either metallic or insulating in nature to obtain the desired metal-insulator geometries as shown in Fig. 1. The results obtained for g_m, C_T, f_T, f_{max} and f_{max}/f_T obtained at maximum value of g_m are tabulated in Table-1 & 2. The conventional gate (N-gate) device is

considered to be of 300 *nm* gate length and other shorter gate length devices used for improving speed are treated as combination of different metal-insulator geometries with passivation layer of SiO_2 for improving various reliability concerns of the device. Furthermore, to minimize the effect of parasitic resistance, analytical and simulation analysis have been performed by considering the source and drain electrode to be vertical in geometry. Various models included in simulation are the CONMOB, FLDMOB and QUANTUM model. The simulated (symbols) [31] and analytical results (solid lines) are compared with each other in this effort and are found to be in good agreement thereby proving the validity of the proposed analytical model.

1. Drain side Field Plates (DFP)

Analysis of FP on drain side for different lengths, thicknesses and shapes of metal-insulator gate geometries have been performed by considering nine different gate geometries listed in Table-1, having lithographic length of 300 *nm* but leading to FP of length 100 *nm* and 200 *nm*. The variation of g_m & I_d, f_T and C_T with gate voltage (V_{gs}) are shown in Fig. 3, 4(a) and 4(b) respectively for 200 *nm* and 300 *nm* gate length devices for the nine different metal-insulator geometric HEMT devices as shown in Fig. 1. Fig. 5 shows the electric field (EF) profile of all these devices at sufficient gate and drain bias (V_{gs} = -3.0 *V* & V_{ds} = 5.0) thereby enabling all

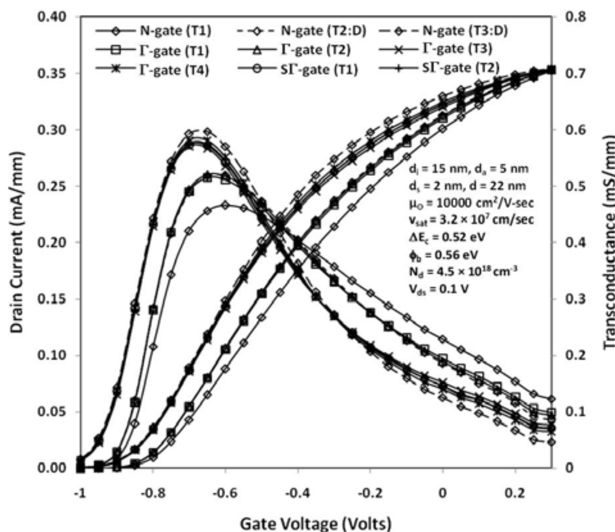

Fig. 3. Variation of drain current and transconductance with gate voltage for various metal-insulator geometric structures acting as field plate on drain side. (Solid) analytical (symbol) simulated [31].

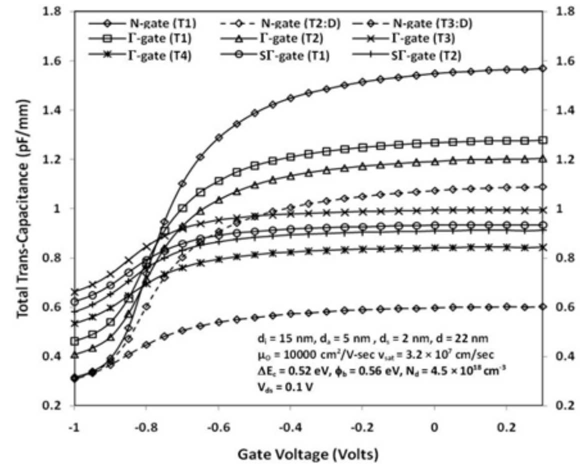

Fig. 4(a)

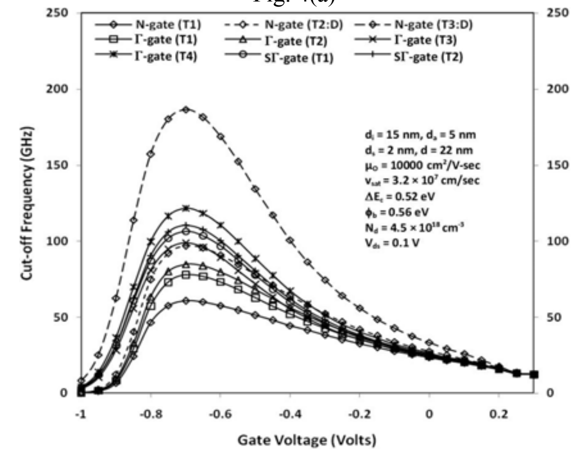

Fig. 4(b)

Fig. 4. (a) Variation of total Trans-capacitance with gate voltage for various metal-insulators geometric structures acting as field plate on drain side. (Solid) analytical (symbol) simulated [31]. (b) Variation of total cut-off frequency with gate voltage for various metal-insulators geometric structures acting as field plate on drain side. (Solid) analytical (symbol) simulated [31].

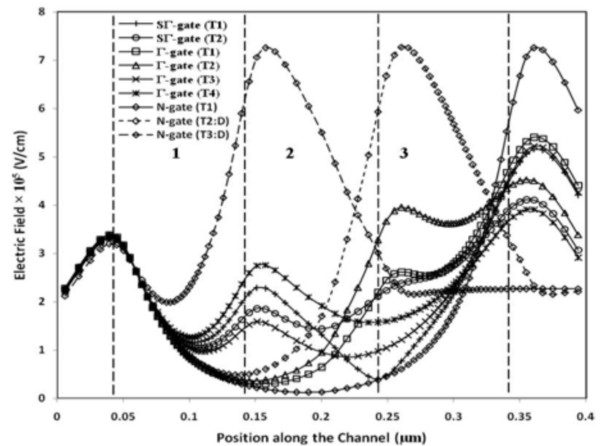

Fig. 5. Variation of Electric field with the position along the channel for various metal-insulators geometric structures acting as field plate on drain side. (Solid) analytical (symbol) simulated [31].

the three regions comprising the channel to reach their threshold values and also causes the EF at the drain end to be larger in magnitude as compared to that obtained at the source end. The results obtained for g_m, C_T, f_T, f_{max} and f_{max}/f_T ratio at V_{ds} = 0.1 V and V_{gs} corresponding to maximum value of g_m have been tabulated in Table 1(a). The results obtained from the table demonstrate that g_m increases from N-gate (T1) to Γ-gate (T1) followed by relative increment in Γ-gate (T2), N-gate (T2: D), Γ-gate (T3), SΓ-gate (T1), SΓ-gate (T2), Γ-gate (T4) and N-gate (T3: D). This shows that introduction of insulator between the N-gate device leads to increase in g_m, and maximum value of g_m is seen when the effect of upper part of gate electrode is negligible. Further, it is seen that the increase in length of insulator underneath the upper part of gate electrode (L_{fp}) has larger effect than the increase of insulator thickness (t_I). SΓ-gate geometry having higher t_I towards drain side has larger value of g_m in comparison to what is obtained when having higher value of t_I in the middle. Γ-gate geometry as compared to step gate profile shows larger enhancement in g_m.

The enhancement in g_m in different devices are due to reduction in channel resistance, which can be explained by considering various regions as various devices connected in series. The device having insulator in between gate and semiconductor have a larger threshold voltage (V_{th}) than the device having gate electrode in immediate contact with the semiconductor. The combination of these devices leads to different V_{th} in different regions; however it's the lowest value that accounts the V_{th} of the overall structure. As a result, the device having insulator in between, keep on gaining the carrier concentration with the variation of V_{gs}, until the other device switches from OFF to ON state. When the device having gate electrode in immediate contact with the semiconductor, switched from OFF to ON state, these carriers start flowing right away under the influence of drain voltage, thus resulting in a sharp increase in I_{ds} from its normal value thereby increasing the slope of the I_{ds}-V_{gs} characteristics and hence g_m of the device. Increasing t_I enhances the carrier concentration in the channel or even maximizes it if the effect of upper gate electrode is negligible, thus raising the g_m further. Increasing L_{fp} increases the peak value of g_m. The variation in characteristics of SΓ-gate with variation of position of insulator with larger thickness is due to the

Table 1(a). Device Characteristics for Drain Side Field Plates

Device	L_g *(nm)*	$t_{I1}/t_{I2}/t_{I3}$ *(nm)*	V_g *(Volts)*	g_m *(S/mm)*	C_T *(pF/mm)*	f_T *(GHz)*	f_{max} *(GHz)*	f_{max}/f_T
N-gate(T1)	300	0/0/0	-0.60	0.47	1.29	57.7	105.5	1.83
Γ-gate(T1)	200	0/0/10	-0.65	0.51	1.07	76.9	168.5	2.19
Γ-gate(T2:D)	200	0/0/20	-0.65	0.52	0.99	83.7	182.2	2.18
N-gate(T2)	200	0/0/∞	-0.65	0.52	0.86	95.6	198.8	2.08
Γ-gate(T3:D)	100	0/10/10	-0.70	0.57	0.92	98.9	205.2	2.08
SΓ-gate(T1)	100	0/20/10	-0.70	0.57	0.86	106.5	225.2	2.12
SΓ-gate(T2)	100	0/10/20	-0.70	0.58	0.83	110.4	236.0	2.14
Γ-gate(T4)	100	0/20/20	-0.70	0.58	0.76	121.6	267.4	2.20
N-gate(T3)	100	0/∞/∞	-0.65	0.60	0.52	181.4	362.0	2.00

Table 1(b). Electric field peaks for Drain Side Field Plates

Device	L_g *(nm)*	$t_{I1}/t_{I2}/t_{I3}$ *(nm)*	$V_{th1}/V_{th2}/V_{th3}$ *(-ve)(Volts)*	E_{p1} *(KV/cm)*	E_{p2} *(KV/cm)*	E_{p3} *(KV/cm)*	E_{p4} *(KV/cm)*
N-gate(T1)	300	0/0/0	0.83/0.83/0.83	339	-	-	702
Γ-gate(T1)	200	0/0/10	0.83/0.83/2.03	338	-	261	541
Γ-gate(T2:D)	200	0/0/20	0.83/0.83/3.23	338	-	395	453
N-gate(T2)	200	0/0/∞	0.83/0.83/ -. --	338	-	727	-
Γ-gate(T3:D)	100	0/10/10	0.83/2.03/2.03	334	159	-	522
SΓ-gate(T1)	100	0/20/10	0.83/3.23/2.03	332	229	-	515
SΓ-gate(T2)	100	0/10/20	0.83/2.03/2.03	313	186	241	411
Γ-gate(T4)	100	0/20/20	0.83/3.23/3.23	331	276	-	391
N-gate(T3)	100	0/∞/∞	0.83/ -. -- /-. --	319	725	-	-

increase of depletion width V_{ds} underneath the FP.

There are three distinct peaks seen in g_m variation with V_{gs} for the concerned devices of L_g = 300 *nm*, 200 *nm* and 100 *nm* respectively. However, the variation of t_I has negligible effect on g_m, but it could lead to reduction in C_T as shown in Fig. 4(a), thereby increasing f_T of the device. The results obtained from Fig. 4(a & b), tabulated in Table 1(a) show that C_T decreases in N-gate (T1) followed by Γ-gate (T1), Γ-gate (T2), N-gate (T2: D), Γ-gate (T3), SΓ-gate (T1), SΓ-gate (T2), Γ-gate (T4) and N-gate (T3: D) and same is the order for the increase in f_T and f_{max} for different devices under consideration. The variation in C_T can be explained from the circuit shown in Fig. 2. For normal gate structures there is nothing between the upper gate electrode and the semiconductor, as a result, there is only a parallel combination of depletion capacitances in the device. But for the other devices, there is a region having an insulator between the upper gate electrode and the semiconductor. This lowers the effect of V_{gs} on depletion of carriers thus decreasing the depletion capacitance (C_R) in that region. The series combination of C_R with insulator capacitance (C_I) results in the further lowering of the gate capacitance in that region. The parallel combination of this gate capacitance with other regions lowers the overall capacitance (C_T) of the device. Increasing L_{fp} leads to enhancement in C_R in two regions in place of one that further reduces the C_T of the device. Increase in t_I decreases the C_R as well as C_I thus reduces the C_T of the device. The variation in characteristics of SΓ-gate with variation in position of insulator layer is due to the increase of depletion width as an effect of V_{ds} underneath the FP. It is found from the analysis that with the increase in V_{ds} and t_I, the enhancement in the device saturates due to saturation in insulator capacitance ($C_I \propto 1/t_I$). With increase in V_{ds}, the device performance saturation is achieved at smaller values of t_I due to lower C_T value obtained at higher V_{ds}. Results also show that device with L_g = 100 *nm* and L_{fp} = 200 *nm* has larger impact of FP in reducing the C_T than the devices with L_g = 200 *nm* and L_{fp} = 100 *nm*.

From Table 1(a), it is quite clear that although N-gate has maximum enhancement in f_T and f_{max} in comparison to metal-insulator geometries but these geometries have higher enhancement in f_{max}/f_T ratio desired for analog applications. Furthermore, to improve the reliability issue, the effect of upper gate electrode should be finite as can be seen from Fig. 5. Fig. 5 shows four different peaks in the electric field profile in the channel viz. E_{p1} (source side of gate edge), E_{p2} (100 *nm* from E_{p1}), E_{p3} (100 *nm* from E_{p2}) and E_{p4} (100 *nm* from E_{p3}). The value of electric field obtained at these peaks is tabulated in Table 1(b). Results obtained from the table shows that E_{p4} has the maximum value in the channel at V_{gs} = -3.0 *V* and V_{ds} = 5.0 *V* and the value of E_{p4} decreases in N-gate (T1)/ N-gate (T2: D)/ N-gate (T3: D) followed by Γ-gate (T1), Γ-gate (T3), SΓ-gate (T1), Γ-gate (T2), SΓ-gate (T2) and Γ-gate (T4). This suggests that increase in t_I decreases the peak at the gate edge near drain side but raises the peak in the middle, whereas, increase in L_{fp} suppresses both these peaks.

The formation of peaks in the electric field profile and variation in these peaks can be explained by dividing the whole channel into various regions as shown in Fig. 1. For N-gate (T1) device, in all the three regions, metal is in direct contact with semiconductor and have almost same V_{th}. So there are only abrupt variations in the channel at the edges of gate electrode leading to formation of two peaks E_{p1} and E_{p4}. For Γ-gate (T1) device, region- 1 & 2 have metal is in direct contact with semiconductor, whereas, the region-3 have insulator in between metal and semiconductor. So, region- 1 & 2 have same V_{th}, almost equivalent to the V_{th} of the overall device, whereas, the region-2 have higher V_{th} leading to higher value of minimum channel potential [V_c (min)] and lower value of electric field in that region. Furthermore, equilibrium between these regions has been established and due to variation in V_{th} in these regions, minimum channel potential in first two regions has also been raised thereby minimizing electric field at the gate edge of source end. Moreover, the abrupt variation between region- 2 & 3 leads to formation of peak E_{p2} in the channel. For Γ-gate (T2) device, t_I have been increased resulting in higher V_{th} in that region compared to Γ-gate (T1) device leading to gradual variation at the gate edge on drain side thereby reducing the value of E_{p4}. However, due to greater abruptness between the region- 2 & 3, this effect also leads to increase in value of E_{p3}. But the E_{p3} is still lesser than the E_{p4} so increase in insulator thickness enhances the performance of Γ-gate HEMT device. It is found from the analysis that the value of E_{p4} and E_{p3} are strongly

dependent on the V_{ds} and t_I. The effect of increase in t_I increases the E_{p3} and decreases the E_{p4} whereas the effect of increase in V_{ds} increases the E_{p4} and decreases the E_{p3}. So the device design required for higher BV_{ds} should have higher value of E_{p4} in comparison to E_{p3}. However, at lower V_{ds} a situation may arise where E_{p3} can become greater than E_{p4} and in that case SΓ-gate can be used to further optimize the device. In some cases while optimizing, both E_{p3} and E_{p4} are found to be lesser than E_{p1} thereby raising the requirement for source side electric field profile optimization. Increasing the t_I can even eliminate the E_{p4} completely and can even raises the E_{P3} to E_{p4} in N-gate (T2) device. Under such circumstances, maximum value of f_T is obtained from N-gate (T2) device. In Γ-gate (T3) device, metal is in direct contact with semiconductor in region-1, whereas, region-2 & 3 have insulator between metal and semiconductor, thus raising the potential in region- 2 & 3 thereby lowering the value of E_{p4} as compared to what is obtained in N-gate (T1) device. This is attributed to the larger length of region having higher V_{th} in comparison to region having lower V_{th}. The equilibrium has to be established between these regions which reduces both the value of E_{p4} and E_{p2} in comparison with the values obtained forΓ-gate (T1) device. Similarly, the effect of increase in t_I and L_{fp} can be seen in Γ-gate (T4) device.

In SΓ-gate (T1) device, metal is in direct contact with semiconductor in region-1 and in region- 2 & 3 there is an insulator in between metal and the semiconductor, and t_I in region- 2 is of double the thickness in region- 3. As there is larger abruptness between region- 1 & 2, so, E_{p2} is larger than that for Γ-gate (T3). The abruptness between the regions B & C can also lead to peak in electric field profile (E_{p3}), but at particular V_{gs}, V_{ds} and t_I this peak can even vanish in this device. This abruptness in region- 2 and 3 also reduces the value of E_{p4} in comparison to Γ-gate (T3). Although E_{p4} in this case is larger in comparison to Γ-gate (T4), but E_{p2} has reduced much more in comparison to Γ-gate (T4) that make this geometry useful at lower drain voltage when the value of middle peaks become greater than the peak at drain end. This happens due to the use of higher value of t_I in the design for higher BV_{ds}. SΓ-gate (T2) device have increase in t_I from source to drain reducing abruptness at the edge of region- 1 & 2 and 2 & 3, thus reducing both the peaks E_{p2} and E_{p3}.

2. Both Drain and Source Side Field Plates (BFP)

Analysis of FP on both drain and source side for length, thickness and shape of metal-insulator gate geometries have been performed by considering six different gate geometries listed in Table 2, having lithographic length of 300 *nm* but leading to FP of length 100 *nm* on both source and drain side. The variation of g_m and I_d, f_T and C_T with V_{gs} are shown in Fig. 6, 7(a) and 7(b) respectively for L_g=100 nm and 300 nm devices for these six different metal-insulator geometric HEMT devices. Fig. 8 shows the electric field profile of all these devices at V_{gs} = -3.0 V and V_{ds} = 5.0 V. The results obtained for g_m, C_T, f_T, f_{max} and f_{max}/f_T ratio at V_{ds} = 0.1 V and V_{gs} corresponding to maximum value of g_m have been tabulated in Table 2(a). The results obtained from the table demonstrate that g_m increases in N-gate (T1) followed by increase in T-gate (T1), IST-gate, ST-gate, T-gate (T2) and N-gate (T3: C). However, C_T decreases in N-gate (T1) followed by decrease in T-gate (T1), IST-gate, ST-gate, T-gate (T2) and N-gate (T3: C) and same is the order of increase in f_T and f_{max}. Comparing the results in Table 1(a) & 2(a), it is found that BFP offers larger enhancements in device characteristics in comparison to DFP due to decrease in depletion width at the source end even in the absence of V_{ds}. Furthermore,

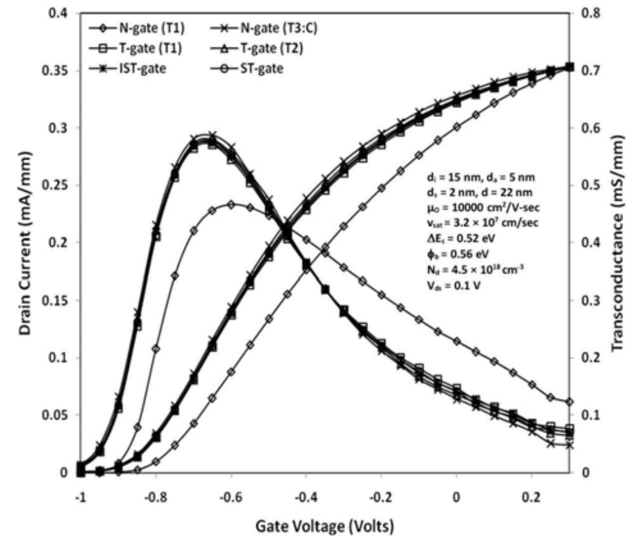

Fig. 6. Variation of drain current and transconductance with gate voltage for various metal-insulator geometric structures acting as field plate on both drain and source side. (Solid) analytical (symbol) simulated [31].

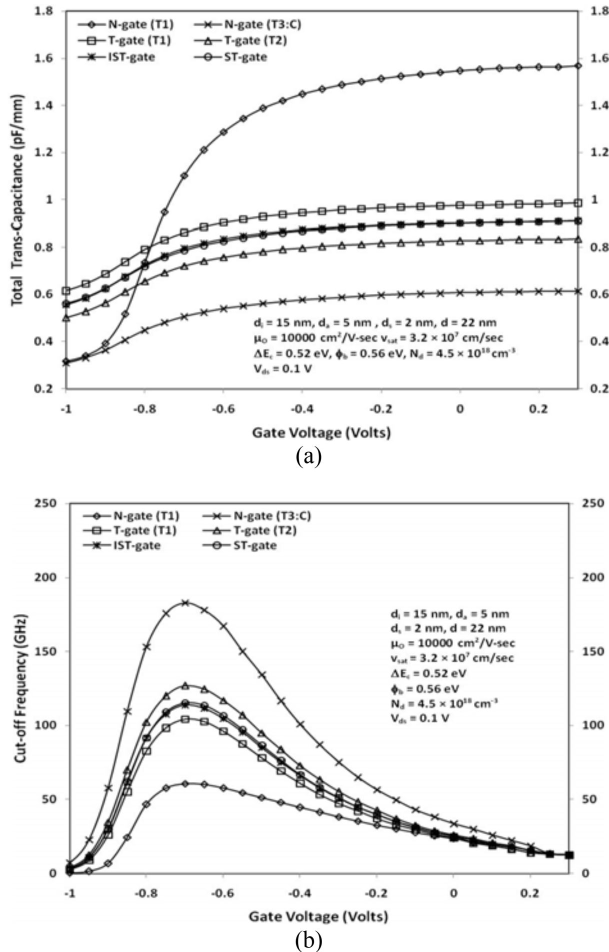

Fig. 7. (a) Variation of total Trans-capacitance with gate voltage for various metal-insulators geometric structures acting as field plate on both drain and source side. (Solid) analytical (symbol) simulated [31]. (b) Variation of total cut-off frequency with gate voltage for various metal-insulators geometric structures acting as field plate on both drain and source side. (Solid) analytical (symbol) simulated [31].

from Fig. 8 it is clear that BFP suppress the field at both drain and source end, whereas, DFP suppress the field only at the drain end. Results tabulated in Table 2(b) also shows that as there is lesser field at the source end so the inclusion of insulator layer of even small thickness i.e., 10 nm t_I, suppresses the source side field (E_{p1}) completely. Comparing the results for IST-gate and ST-gate geometry from Table-2(a), it is found that increase of the t_I at drain end is more beneficial than increase of the t_I at source end in suppressing the electric field and this fact is reemphasized by Fig. 8 and Table-2(b). Increase of t_I uniformly on both source and drain side

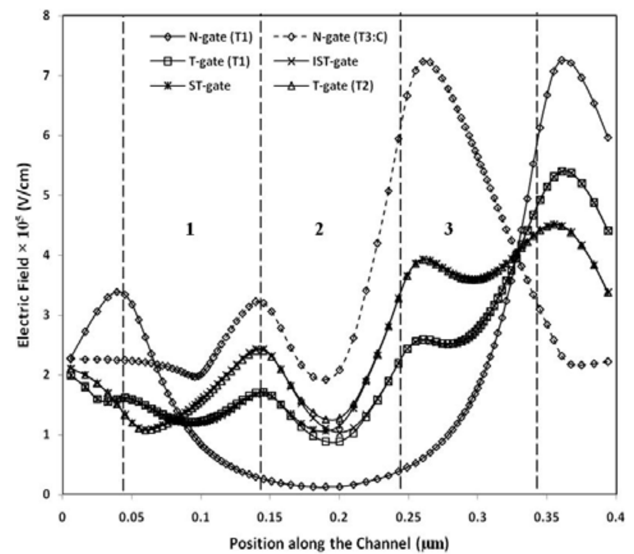

Fig. 8. Variation of Electric field with the position along the channel for various metal-insulators geometric structures acting as field plate on both drain and source side. (Solid) analytical (symbol) simulated [31].

Table 2(a). Device Characteristics for both Drain and Source Side Field Plates

Device	L_g *(nm)*	$t_{I1}/t_{I2}/t_{I3}$ *(nm)*	V_{gs} *(Volts)*	g_m *(S/mm)*	C_T *(pF/mm)*	f_T *(GHz)*	f_{max} *(GHz)*	f_{max}/f_T
N-gate(T1)	300	0/0/0	-0.60	0.47	1.29	57.7	105.5	1.83
T-gate(T1)	100	10/0/10	-0.65	0.57	0.89	102.7	226.2	2.20
IST-gate	100	20/0/10	-0.65	0.57	0.81	111.6	240.1	2.15
ST-gate	100	10/0/20	-0.65	0.58	0.81	113.5	240.2	2.12
T-gate(T2)	100	20/0/20	-0.65	0.58	0.74	124.5	271.0	2.18
N-gate(T3:C)	100	∞/0/∞	-0.65	0.59	0.52	178.1	356.8	2.00

Table 2(b). Electric field peaks for both Drain and Source Side Field Plates

Device	L_g *(nm)*	$t_{I1}/t_{I2}/t_{I3}$ *(nm)*	$V_{th1}/V_{th2}/V_{th3}$ *(-ve)(Volts)*	E_{p1} *(KV/cm)*	E_{p2} *(KV/cm)*	E_{p3} *(KV/cm)*	E_{p4} *(KV/cm)*
N-gate(T1)	300	0/0/0	0.83/0.83/0.83	339	-	-	721
T-gate(T1)	100	10/0/10	2.03/0.83/2.03	-	171	259	539
IST-gate	100	20/0/10	3.23/0.83/2.03	-	243	258	539
ST-gate	100	10/0/20	2.03/0.83/3.23	-	169	393	451
T-gate(T2)	100	20/0/20	3.23/0.83/3.23	-	241	392	451
N-gate(T3:C)	100	∞/0/∞	-. -- /3.23/ -. --	-	322	724	-

has larger effect in increasing both g_m and f_T than device with different t_I on both source and drain side. In that case also, by considering the finite effect of upper gate electrode on both source and drain side, the f_{max}/f_T ratio enhances and f_T and f_{max} decreases.

IV. CONCLUSIONS

Intensive simulation work with analytical analysis has been carried out to study the effect of variations in length, thickness and position of the insulator under the gate for various metal-insulator gate geometries like T-gate, Γ-gate, Step-gate etc., to anticipate superior device performance in conventional HEMT structure with same lithographic length. Analysis has been performed for DFP and for BFP. Analytical results are compared with simulated results and are found to be in good agreement with each other, thus proving the validity of the analytical model. Variation of t_I has negligible effect on g_m, but it could lead to reduction on C_T, thereby increasing the f_T of the device. C_T decreases in N-gate (T1) followed by reduction of C_T in Γ-gate (T1), Γ-gate (T2), N-gate (T2: D), Γ-gate (T3), T-gate (T1), SΓ-gate (T1), SΓ-gate (T2), IST-gate, ST-gate, Γ-gate (T4), T-gate (T2), N-gate (T3: C) and N-gate (T3: D) and same is the order of increase in f_T and f_{max}. Increase in t_I decreases the peak at the gate edge near drain side but raises the peak in the middle and can be even suppressed using Step-gate geometries. BFP offers larger enhancements in device characteristics in comparison to DFP. Furthermore, BFP suppress the field at both drain and source end, whereas, DFP suppress the field only at the drain end. However f_T and f_{max} decreases by considering the finite effect of upper gate electrode on both source and drain side but it enhances the f_{max}/f_T ratio which is desired for analog applications.

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