Level Up/Down Converter with Single Power-Supply Voltage for Multi-VDD Systems

Ji Yeon An, Hyoun Soo Park, and Young Hwan Kim

***Abstract*—For battery-powered device applications, which grow rapidly in the electronic market today, low-power becomes one of the most important design issues of CMOS VLSI circuits. A multi-V_{DD} system, which uses more than one power-supply voltage in the same system, is an effective way to reduce the power consumption without degrading operating speed. However, in the multi-V_{DD} system, level converters should be inserted to prevent a large static current flow for the low-to-high conversion. The insertion of the level converters induces the overheads of power consumption, delay, and area. In this paper, we propose a new level converter which can provide the level up/down conversions for the various input and output voltages. Since the proposed level converter uses only one power-supply voltage, it has an advantage of reducing the complexity in physical design. In addition, the proposed level converter provides lower power and higher speed, compared to existing level converters.**

***Index Terms*—Level converter, multi-V_{DD} system, low-power**

I. INTRODUCTION

As the use of the mobile electronic devices increases very rapidly, low-power becomes a very important circuit design issue. Fig. 1 shows the consumer portable power consumption trend [1]. As shown in the figure, both of the dynamic and static powers are increasing continuously. In CMOS VLSI circuits, lowering the power-supply voltage (V_{DD}) is an effective way of the low-power design, because it results in a quadratic reduction in dynamic power consumption and an exponential reduction in leakage power consumption [2]. However, lowering the V_{DD} of the whole system degrades the operating speed. To reduce power consumption while avoiding the speed degradation, a multi-V_{DD} system approach that uses more than one V_{DD} in the same system was proposed [3]. In the multi-V_{DD} system, we apply low-V_{DD} (V_{DDL}) to the logic gates on the non-critical paths, while applying high-V_{DD} (V_{DDH}) to the logic gates on the critical paths. Generally, although multi-V_{DD} can be applied at the gate level, the voltage island approach, applying the multi-V_{DD} system at the large macro level [4], is more widely used nowadays.

When the logic '1' signal of the V_{DDL} block drives the V_{DDH} block, however, a multi-V_{DD} system has a large static current through the weakly turned-on PMOS transistor of the V_{DDH} block, as shown in Fig. 2. To prevent this current, the level converter which converts the V_{DDL} signal to the V_{DDH} signal is necessary. On the other hand, when the V_{DDH} block drives the V_{DDL} block, it is not necessary to put the level converter between the two blocks from the viewpoint of physical design. However, a cell characterized with the different voltages

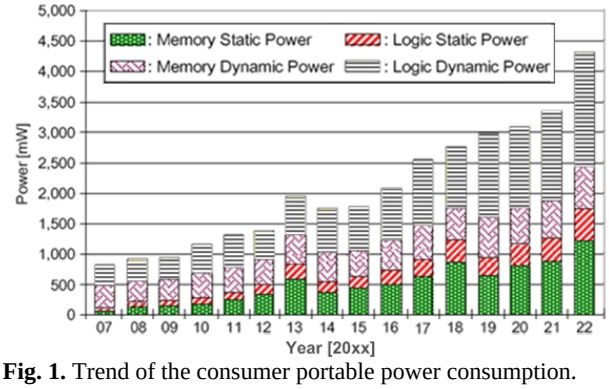

Fig. 1. Trend of the consumer portable power consumption.

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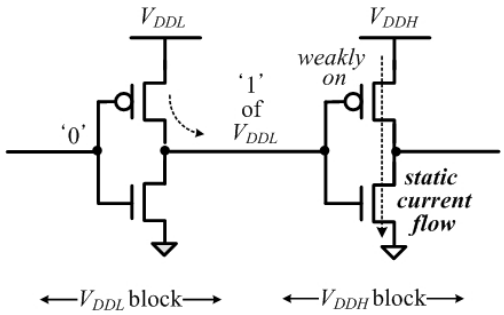

Fig. 2. A static current flow through a V_{DDH} block due to the weakly turned-on PMOS.

for input and output pins is necessary for the accurate static timing analysis. Thus, this specially-identified cell like a level converter which has a down-converting function may be used in the multi-V_{DD} system for the purpose of safe timing closure. However, the use of level converters induces the overheads in terms of power consumptions, delay, and area [3]. Besides the insertion of the level converters may increase the complexity when doing the placement and routing in physical design. Therefore, one of the main challenges in a multi-V_{DD} system is to reduce the overheads caused by inserting the level converters.

In this paper, we propose a new level converter which has the level up/down-conversions and provides the flexibility in physical design by using one power-supply voltage. In addition, it has the advantages of low-power and high-performance compared to existing level converters.

The rest of this paper is organized as follows. A detailed description on the proposed level converter is given in section II, and the experimental results are given in section III. Finally, section IV concludes this paper.

II. PROPOSED LEVEL CONVERTER

Several level converters which provide the up-converting function have been proposed in some literatures. Each level converter has the strengths and weaknesses. For example, among the existing level converters, pass-transistor half latch [5] provides low-power and high-speed. However, since the pass-transistor half latch requires V_{DDH} and V_{DDL} power-supply voltages, the placement and routing are difficult in physical design. Another level converter, PMOS cross-coupled level converter (CCLC) [3] has been widely used to prevent the static current. However, CCLC also has the layout problem in physical design due to the use of the dual power-supply voltages and its operation speed is relatively slow. On the other hand, in order to solve the layout problem, single-supply diode-voltage-limited level converter (SSLC) [6] which uses only high power-supply voltage was proposed. Fig. 3 shows the advantage of using the level converter with single power-supply voltage. The level of power-supply voltage is same with that of next domain's input. Reducing the number of power-supply voltages makes the placement and routing much easier than the level converter with the dual power-supply voltages. However, SSLC does not have the best performance compared to the existing level converters [5].

The proposed level converter has all advantages (single power-supply voltage, low-power, and high speed) of the previous level converters as mentioned above. Additionally, it provides the down-converting function as well as up-converting function. Fig. 4 represents the schematics of the pass-transistor half latch, CCLC, SSLC and the proposed level converter. In the figure, shaded gates are operated by a V_{DDL} signal and others are operated by a V_{DDH} signal. Underlined node has a V_{DDL} signal and others have V_{DDH} signals. In the proposed level converter, the transistor M1, NMOS pass transistor, is always turned on because the gate of M1 is connected with the V_{DDH} (logic '1') which can make the transistor M1 turn on. By using the threshold voltage drop of the transistor M1, we can provide $V_{DDH} - V_{TH,\mathrm{M1}}$ to node x. This voltage acts as a virtual V_{DDL} (logic '1') and can make the transistor M2 turn on. However, the leakage current of transistor M1 can boost up to above ideal value at node x, $V_{DDH} - V_{TH,\mathrm{M1}}$, which limits the ability of the proposed level converter to block the

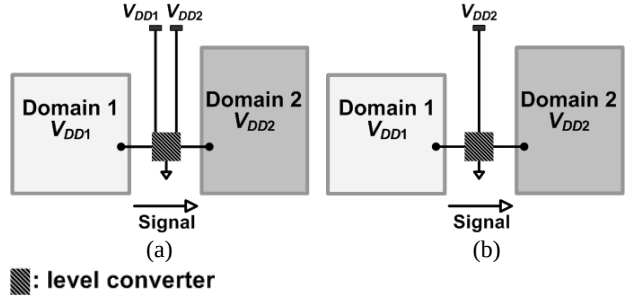

Fig. 3. An example of voltage island with the level converter. By using one power-supply voltage for level converters, the complexity for placement and routing can be reduced. Level converters using (a) two power-supply voltages and (b) single power-supply voltage.

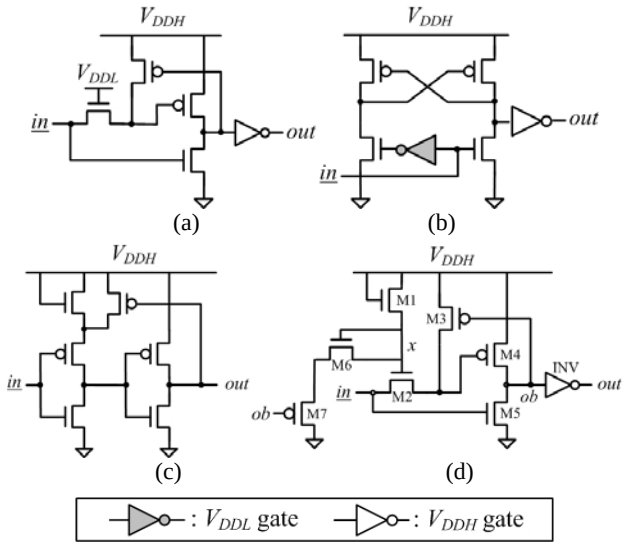

Fig. 4. Schematics of the existing and proposed level converters. (a) Pass-transistor half latch [5], (b) PMOS cross-coupled level converter [3], (c) Single-supply diode-voltage-limited level converter [6], and (d) Proposed level converter.

reverse current flow (to be explained later) when input at node *in* is logic '1'. In case of logic '0' input, there is no reverse current flow, because the tuned off M2 cuts off the path of reverse current. We use transistors M6 and M7 to maintain the voltage level at node *x*. The voltage level is determined by the resistance ratio of transistors M1, M6, and M7. Specifically, M7 can be driven by the signal of *ob* (output bar), and then only turned on when the input is logic '1' due to reducing the leakage current. In this case, M6 has a role to minimize the sensitivity in controlling the resistance ratio of M1, M6 and M7.

In case that the proposed level converter performs an up-converting function, we should consider the reverse current problem. When the input at node *in* is logic '1' of V_{DDL}, if the voltage of node *x* exceeds $V_{DDL} + V_{TH,M2}$, then the reverse current flows. The reverse current is defined as a current that flows from V_{DDH} of the level converter backward to V_{DDL} of the preceding logic blocks. In case of the proposed level converter, the voltage of node *x* is $V_{DDH} - V_{TH,M1}$, and hence the no reverse current flows if the following constraint is satisfied.

$$V_{DDH} - V_{TH,M1} < V_{DDL} + V_{TH,M2}. \quad (1)$$

In (1), assume that the threshold voltages of all the transistors are same and the value of V_{DDL} can be represented the product of α (which is an arbitrary constant below 1) and V_{DDH}, and then we can simply represent above constraint as follows.

$$V_{DDH} - V_{TH} < \alpha V_{DDH} + V_{TH}. \quad (2)$$

To prevent the reverse current problem, we have to choose the values of V_{DDH}, α, and V_{TH} which can satisfy the above constraint. Typically, V_{DDL} is selected 70% of V_{DDH} [5], thus we set α to 0.7. Fig. 5 represents the SPICE waveforms of the proposed level converter's low-to-high conversion for the various input and output voltages. To obtain the waveforms, each transistor was optimized. In the figures, underlined node *in* denotes V_{DDL} input signals and node *out* denotes the level converted V_{DDH} output signals. V_{DDL} input signals are 0.85 V, 0.7 V, and 0.55 V, which are the 70% of V_{DDH} (1.2 V, 1.0 V, and 0.8 V).

In case of using the level converter which provides the down-converting function, V_{DDH} and V_{DDL} exchange each other so that input at node *in* has higher value than the output at node *out*. Since the node *in* has higher value than the node *x*, there are no reverse current as mentioned earlier. Fig. 6 represents the SPICE waveforms of the proposed level converter's high-to-low conversion for the various input and output voltages. To obtain the

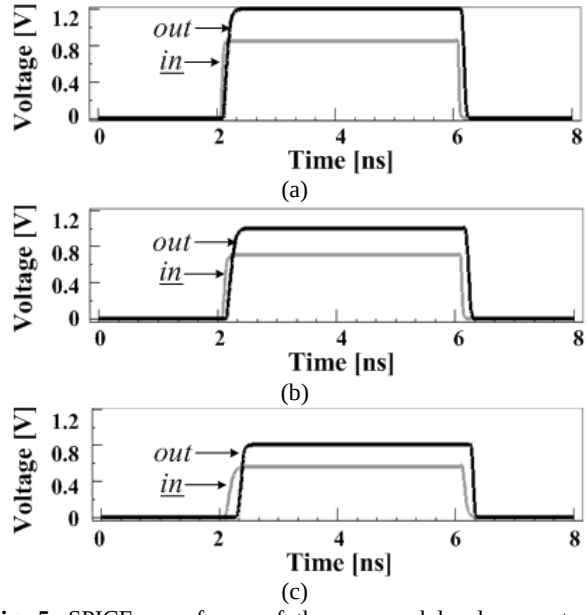

Fig. 5. SPICE waveforms of the proposed level converter's low-to-high conversions at node *in* and *out* for three different voltage levels. For low-to-high conversions, input has V_{DDL} level (gray lines) and output has the V_{DDH} level (black lines). Each voltage level of V_{DDL} is about 70% of V_{DDH}. (a) V_{DDL} = 0.85 V and V_{DDH} = 1.2 V, (b) V_{DDL} = 0.7 V and V_{DDH} = 1.0 V, and (c) V_{DDL} = 0.55 V and V_{DDH} = 0.8 V.

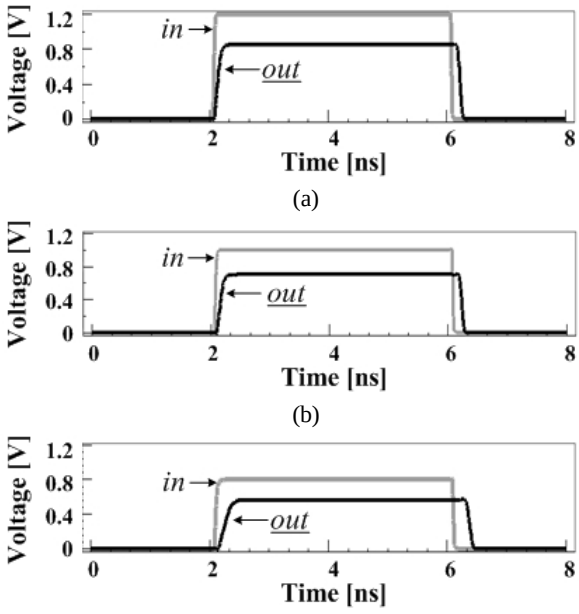

Fig. 6. SPICE waveforms of the proposed level converter's high-to-low conversions at node *in* and *out* for three different voltage levels. For high-to-low conversions, input has V_{DDH} level (gray lines) and output has the V_{DDL} level (black lines). Each voltage level of V_{DDL} is about 70% of V_{DDH}. (a) V_{DDH} = 1.2 V and V_{DDL} = 0.85 V, (b) V_{DDH} = 1.0 V and V_{DDL} = 0.7 V, and (c) V_{DDH} = 0.8 V and V_{DDL} = 0.55 V.

waveforms, each transistor was optimized. In the figure, node *in* denotes V_{DDH} input signals and underlined node *out* denotes the level converted V_{DDL} output signals. This high-to-low conversion uses the same values of V_{DDL} and V_{DDH} as the low-to-high conversion uses.

Fig. 5 and 6 show that the proposed level converter performs properly level up/down-conversions. Therefore, the proposed level converter can be used in the multi-V_{DD} system so that it can provide level converted signal to the different voltage domains.

III. Experimental Results

To evaluate and compare the performances of the level converters, we used the test bench of [7] and three existing level converters: pass-transistor half latch, SSLC, and CCLC. Since these existing level converters have only up-converting function, we performed the experiment for up-conversion. The experimental environment is as follows. We set V_{DDH} to 1.0V and V_{DDL} to 0.7V. Experiments were executed at the room temperature (25°C) and the clock frequency was set to 500MHz. We added 22fF and 3.77fF as an output load

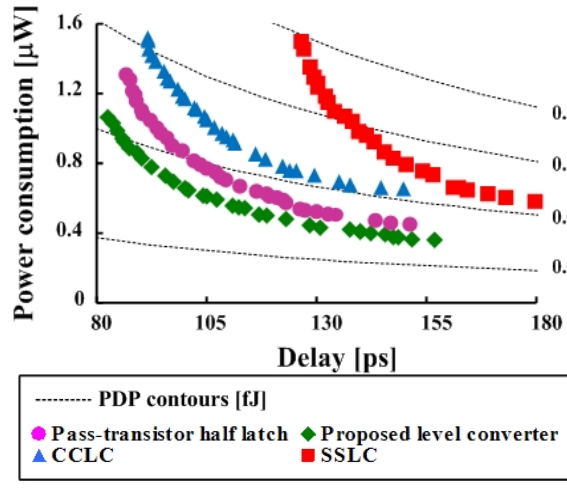

Fig. 7. Performances of the existing and proposed level converters in the power-delay space. Dashed lines represent the power-delay product (PDP, power × delay [fJ]).

capacitance and an input capacitance of each level converter, respectively. All the circuits were designed using the 45 nm Berkeley Predictive Technology Model (PTM), and all simulations were performed using Synopsys HSPICE with BSIM4 model at the schematic level. We set both the switching activity and the probability of the input signal to 0.5 for measuring the power consumption.

To compare the proposed level converter with the three benchmark circuits in performance, we need to plot the performance of the level converters on the power-delay space, where both of the power and the delay can be viewed [7]. For the comparison, we optimized the level converters on the power-delay space using the method presented in [8], as follows. Under the given delay constraint, we changed the gate widths of transistors using HSPICE's built-in optimizer in the direction to the minimum power consumption while maintaining the correct operation of level converter. For the optimization, the gate length was set to the minimum dimension. We continuously estimated the power consumption as changing the delay constraints. We iterated these procedures until we got all the necessary data, shown in Fig. 7. In the figure, the x-axis represents the larger value of the rising and falling delays. The y-axis represents the power consumption and the dashed lines represent the same values of the power-delay product (PDP). The figure indicates that the proposed level converter outperforms the existing level converters: the proposed level converter had lower power

Table 1. Performances of four level converters at the minimum PDP points

V_{DD} type	Level converter Name	Total power	Delay	Min.[1] PDP	Total gate width	Leakage power
		[μW]	[ps]	[fJ]	[μm]	[nW]
Dual	CCLC	0.691	127.0	**0.088**	1.75	17.12
	Pass-tr[2] half latch	0.461	133.3	**0.061**	1.125	10.91
Single	SSLC	0.631	165.7	**0.105**	3.175	10.36
	Proposed	0.400	148.5	**0.059**	1.475	8.597

[1]Min.: minimum [2]tr: transistor

consumption at the same delay, and had smaller delay at the same power consumption than the existing level converters. Table 1 represents the performance of each level converter at the minimum PDP point, obtained from Fig. 7, in terms of total power, delay, PDP, total gate width, and leakage power. In the table, the proposed level converter exhibits 3.3 ~ 43.8% less PDP than the existing level converters. In Table 1, the speed of the proposed level converter at the minimum PDP point is slightly slower than that of dual-V_{DD} LCs. However, the proposed level converter can compensate for the speed with better performances in terms of PDP, total power, total gate width, and leakage power.

IV. CONCLUSIONS

In this paper, we proposed a new level converter for a multi-V_{DD} system. The proposed level converter provides the level up/down conversions for the various input and output voltage levels. Since the proposed level converter uses only one power-supply voltage, it has the advantage of reducing the complexity during physical design. In addition, the proposed level converter has the advantages of low-power and fast operating speed. Experimental results show that the proposed level converter outperforms the existing level converters in all aspects of the power consumption, delay, and PDP. At the minimum PDP points, the proposed level converter exhibited 3.3 ~ 43.8% less PDP compared to the existing level converters.

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