

Inter-Pin Skew Compensation Scheme for 3.2-Gb/s/pin Parallel Interface

Jang-Woo Lee, Hong-jung Kim, Young-Jin Nam, and Changsik Yoo

Abstract—An inter-pin skew compensation scheme is proposed, which minimizes the inter-pin skew of parallel interface induced by unequal trace length and loading of printed circuit board (PCB). The proposed scheme measures the inter-pin skew and compensates during power-up with simple hardware. The proposed scheme is applied to 3.2-Gb/s/pin DDR4 SDRAM and implemented in a 0.18 m CMOS process. The inter-pin skew is compensated in 324-cycles of 400-MHz clock and the skew is compensated to be less than 24-ps.

Index Terms—Parallel interface, inter-pin skew, skew compensation, CMOS, DDR4 SDRAM

I. INTRODUCTION

The data rate of main memory system such as DDR3 and DDR4 SDRAM is exceeding 3-Gb/s/pin with 64-bit data (DQ) lines and 8 strobe (DQS) lines running in parallel. For sufficiently large data opening at receiver side, various timing uncertainties should be minimized such as set-up/hold time of receiver, clock jitter, inter-symbol interference (ISI), cross-talk, and so on. The inter-pin skew among 64 DQ and 8 DQS lines can play a critical role in determining the data opening at receiver side. The inter-pin skew due to unequal line length at FR4 PCB is different arrival times of data bits at the far end of the channels as shown Fig. 1. To minimize this inter-pin skew, the lengths of these 64 DQ and 8 DQS lines should be equal and the routing of these lines on PCB can be very complicated. If we can allow unequal

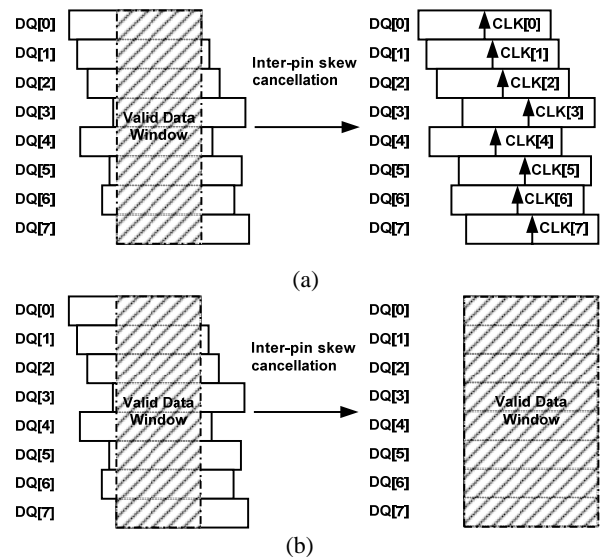


Fig. 1. Inter-pin skew compensation by (a) sampling position adjustment (b) data signal adjustment.

line lengths among these 72 lines and compensate the inter-pin skew with some circuitry, the routing on PCB would be very easy.

There have been several methods to compensate the inter-pin skew [1-4]. The XDR RAMBUS DRAM (RDRAM) is employing FlexPhase where the inter-pin skew is compensated by moving the sampling position of each DQ to the center of DQ eye as shown in Fig. 1(a) [3]. Because the sampling clocks have different phase for each DQ, there must be a re-timing circuit following the DQ sampling circuit, which can increase the latency of DQ receive path.

In this paper, the inter-pin skew is compensated by aligning the eye openings of all DQs as shown in Fig. 1(b). Because the sampling points of all DQs are same, there is no need for additional re-timing block. The detailed explanation of the proposed inter-pin skew compensation scheme and experimental results are given in the following sections.

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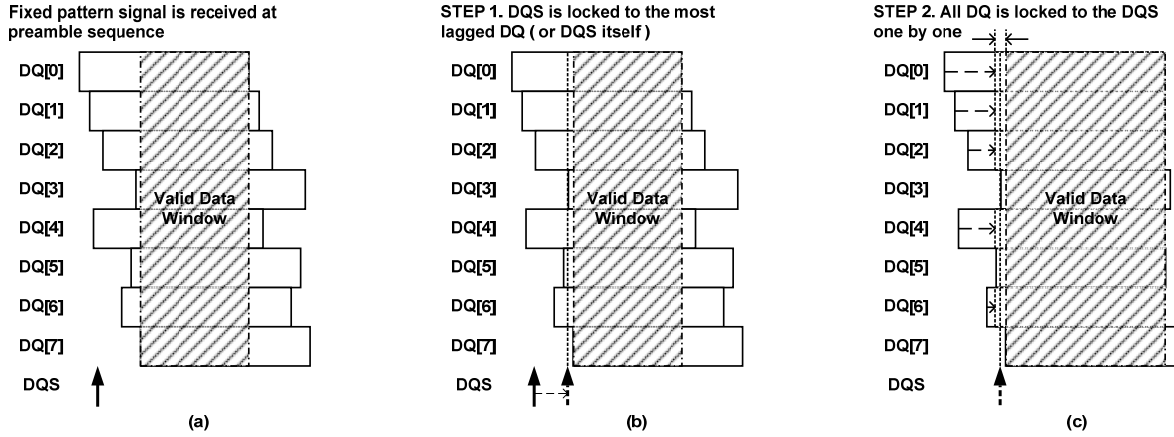


Fig. 2. Proposed inter-pin skew compensation algorithm.

II. INTER-PIN SKEW COMPENSATION

Among the data inputs (both DQ and DQS), the most lagged input is selected and used as a reference signal for the skew compensation. All the other data inputs are then aligned to the reference input. As shown in Fig. 2, the inter-pin skew is compensated in two steps. The first step in Fig. 2(b) delays the DQS to the most lagged data inputs. If the DQS is the most lagged one, then there is no need to delay the DQS. After this step, it is ensured that the DQS is the most lagged input and can be used as the reference signal for the skew compensation. The second step shown in Fig. 2(c) delays all the DQs so their edges are aligned to that of DQS.

In Fig. 3, the block diagram of the inter-pin skew compensation circuit is shown. All the inputs (DQ and

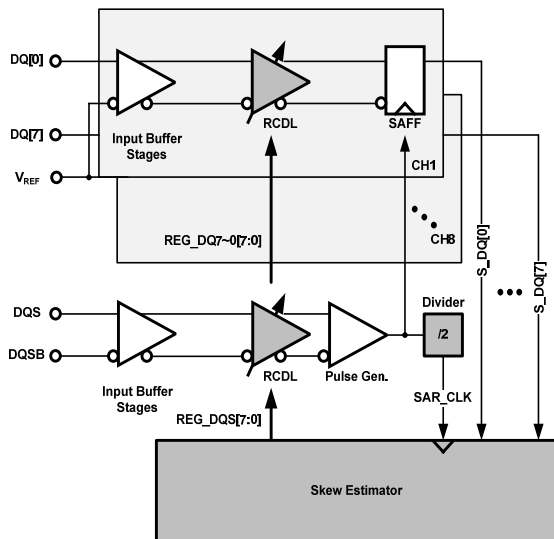


Fig. 3. Proposed inter-pin skew compensation block diagram.

DQS) have register controlled delay line (RCDL) which is used to compensate the inter-pin skew. The sense-amplifier flip-flop (SAFF) detects the phase error between DQ and DQS. The skew estimator measures the inter-pin skew using detected phase error and stores the skew compensation information in the register of delay line. For high speed operation, the RCDL consists of low swing current-mode logic (CML) delay cell. But the clock signal of SAFF requires full swing. Thus, low swing of RCDL is converted to full swing by pulse generator (Pulse Gen.). In Fig. 4, the block diagram of the proposed inter-pin skew estimator circuit is shown. During the first step, the NAND-gated output of all the SAFFs is used to control the RCDL of the DQS input path. If DQS leads a DQ, the output of the SAFF corresponding to that DQ pin would be LOW and therefore the NAND-gate output would be HIGH. By doing this, the first step operation can be completed in a very short time because there is no need to compare the

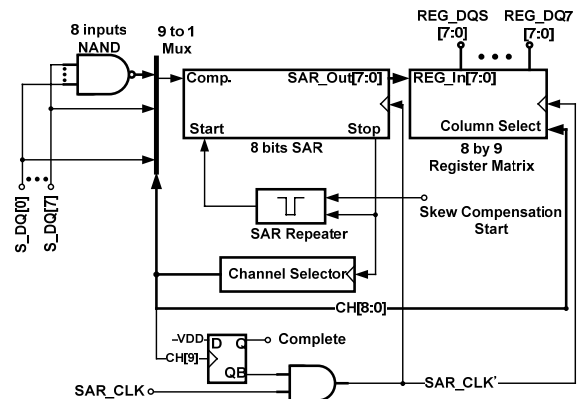


Fig. 4. Proposed Skew Estimator block diagram.

edge of DQS with those of DQs one by one. The delay of the RCDLs is locked by a binary search algorithm using 8 bits successive approximation register (SAR) to minimize the time required for inter-pin skew compensation [5]. For power and size saving, only one 8 bits SAR block is used for skew compensation. And repeat operation is allowed by SAR repeater and channel selector. If the operation of 8 bits SAR is complete, the 8 bits SAR is reset and restarted by SAR repeater and next channel is selected by channel selector.

The SAFFs used as a phase detector during inter-pin skew compensation are DQ sampling circuits for normal DRAM operation. Therefore, the hardware increase due to the inter-pin skew compensation is minimized. The additional circuit blocks required for inter-pin skew compensation are RCDLs and skew estimator using SAR for delay locking, which is much simpler than that of previous works [1-4].

The frequency of clock-like DQs and DQS during inter-pin skew compensation is 400 MHz for harmonic lock prevention of DLL and wide compensation range. In Fig. 5, the block diagram of the register controlled delay line (RCDL) circuit is shown. For influence of PVT and input data rate variations reduction, the -3 dB bandwidth of coarse delay cell (CDC) is fixed to 3.2 GHz by delay locked loop using 8 bits SAR before skew compensation operation. The delay of the RCDLs can be controlled upto two bit window for 3.2-Gb/s and the resolution of the delay control is 8 bits. The inter-pin skew is compensated by multiplexing and interpolation.

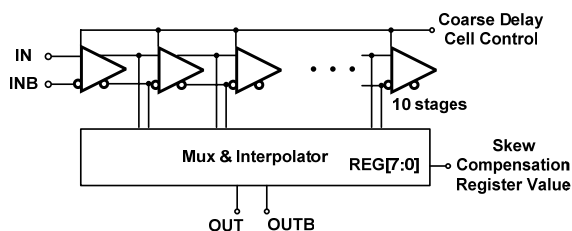


Fig. 5. Register Controlled Delay Line block diagram.

III. EXPERIMENTAL RESULTS

This proposed algorithm is implemented in a 0.18 μm CMOS process. The simulated waveform of DQs after the inter-pin skew compensation is shown in Fig. 6. The maximum setting inter-pin skew between DQs and DQS is 600 ps at the input of skew compensation block. The

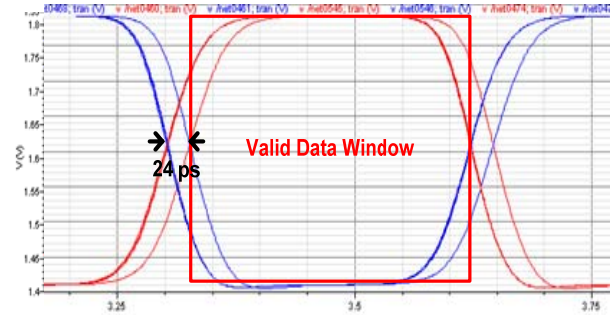


Fig. 6. Inter-pin skew compensated DQ waveforms at 3.2 Gb/s.

remaining skew is 24 ps after the inter-pin skew compensation, which is determined by the timing uncertainty of the SAFFs used for phase detection. The simulation results are summarized in Table 1.

Table 1. Performance summary (simulation results)

Process	0.18 μm CMOS
Skew Cancellation Methodology	Closed-loop DLL
Data Rate	3.2 Gbps
Skew Compensation Range	625 ps (= 2 Data-eyes)
Skew Compensation Resolution	Less than 24 ps (Decided by uncertainty window of SAFF) 324 cycles @400 MHz clock
Total Operation Time	
Chip Area (with output buffering circuit)	1030 μm x 2630 μm

IV. CONCLUSIONS

In this paper, an inter-pin skew compensation scheme is proposed which can greatly simplify the design of printed circuit board of multi-gigabit parallel interface. The additional hardware for inter-pin skew compensation is minimal because the circuit blocks for normal I/O operation are re-used.

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REFERENCES

[1] Sung HoWang, Jeongpyo Kim, Joonsuk Lee, Hyoung Sik Nam, Young Gon Kim, Jae Hoon Shim, Hyung Ki Ahn, Seok Kang, Bong Hwa Jeong, Jin Hong Ahn, and Beomsup Kim, "A 500-

Mb/s Quadruple Data Rate SDRAM Interface Using a Skew Cancellation Technique,” *IEEE J. Solid-State Circuits*, Vol.36, No.4, April 2001.

- [2] E. Yeung and M. Horowitz, “A 2.4 Gb/s/pin Simultaneous Bidirectional Parallel Link with Per-Pin Skew Compensation,” *IEEE J. Solid-State Circuits*, Vol.35, No.11, November 2000.
- [3] http://www.rambus.com/us/patents/innovations/detail/flexphase_timing.html
- [4] T. Sato, Y. Nishio, T. Sugano, and Y. Nakagome, “A 5-GB/s Data-Transfer Scheme with Bit-to-Bit Skew Control for Synchronous DRAM,” *IEEE J. Solid-State Circuits*, Vol.34, No.5, May 1999.
- [5] Guang-Kaai Dehng, June-Ming Hsu, Ching-Yuan Yang, and Shen-Iuan Liu, “Clock-Deskew Buffer Using a SAR-Controlled Delay Locked Loop,” *IEEE J. Solid-State Circuits*, Vol.35, No.8, August 2000.



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