# Mosfet Models, Quantum Mechanical Effects and Modeling Approaches: A Review

**Amit Chaudhry* and J. N. Roy****

***Abstract*—Modeling is essential to simulate the operation of integrated circuit (IC) before its fabrication. Seeing a large number of Metal-Oxide-Silicon Field-Effect-Transistor (MOSFET) models available, it has become important to understand them and compare them for their pros and cons. The task becomes equally difficult when the complexity of these models becomes very high. The paper reviews the mainstream models with their physical relevance and their comparisons. Major short-channel and quantum effects in the models are outlined. Emphasis is set upon the latest compact models like BSIM, MOS Models 9/11, EKV, SP etc.**

***Index Terms*—MOS models, quantum mechanical effects, BSIM**

## I. INTRODUCTION

CMOS technology has contributed significantly to the microelectronics industry thus playing an important role in the overall development of all the countries. This is primarily due to its vast applications in every sphere and in nearly every industry. The performance and density of a CMOS chip can be improved through device scaling which is inevitable as also propounded by Moore law which says that the transistor density on a CMOS chip doubles approximately after every one and a half years [1, 2]. Continuing with the Moore law, the gate length of the MOSFET will eventually shrink to 10 nm in 2015 [3]. This will make many new applications possible. Especially important are the commercial requirements of miniaturization such as mobile equipment etc.

Seeing the trend of down scaling, continuous improvements in the VLSI MOSFET device models are required so that the exact behavior of deep sub-micron and nanometer scaled MOSFETs can be described with accuracy.

MOSFET modeling is facing difficulties to achieve accurate description of such scaled down devices. The reason is that many complicated new phenomena are arising which are not easy to describe. One such phenomenon arising out of down scaling the MOSFET is the failure of classical physics in the at nanoscale levels in MOSFETs. As CMOS technology scales down aggressively, it approaches a point, where classical physics is not sufficient to explain the behavior of a MOSFET. At this classical physics limit, quantum mechanics has to be taken into account to accurately assess the overall performance of a MOSFET.

## II. MOSFET SCALING REQUIREMENTS AND IMPLICATIONS

MOSFET operates on the principle of creating an inversion layer using a gate voltage giving applications in analog and digital areas. It is basically a two-dimensional device. Its input voltage is applied to the poly silicon gate, substrate and source are generally grounded and at the drain a voltage is applied to extract the charge carriers.

For the last six decades, the semiconductor industry has been working hard to miniaturize the structure of the MOSFET because of accommodating more transistors on a single chip, thus performing multi tasks and also

Manuscript received Sep. 26, 2009; revised Dec. 27, 2009.
*Faculty of University Institute of Engineering and Technology, Panjab University, Chandigarh, India
**Senior Member IEEE and Vice President, Solar Semiconductor Private Limited, Hyderabad, India
E-mail : amit_chaudhry01@yahoo.com

resulting in the reduced cost of the chip production. The speed of the chip also improves ideally due to the smaller gate lengths. Despite some merits of scaling down, there are some implications which need to be addressed seriously while scaling down at extremely low gate lengths such as gate oxide scaling which results in leakage currents. The reduction of leakage currents is the main issue in MOSFET scaling [4, 5]. For the 90 nm technology node, the thickness of silicon oxide is of the order of sub 2 nm [6]. Quantum mechanical direct tunneling and Fowler-Nordhiem through the gate oxide leads to excessive power dissipation and loss of on-current density [7]. The quantum mechanical tunneling between the source and drain also takes place for scaled down MOSFET in sub-10 nanometer regions. This will ultimately retard the scaling process of the MOSFET and will make them unuseful for switching purpose as the leakage currents dominate the conduction currents as also given in [8].

## III. MOSFET MODELS

MOSFET models play an important part in the development of an efficient chip industry. These models have been continuously developed and improved over the past many years. These improvements resulted in the increase of the model parameters to cover additional effects. The MOSFET models are used by circuit simulators. The circuit designer's efficiency to develop a circuit depends mainly on the device model. The accuracy and simplicity of the model has a deep influence on the designing and fabrication of the circuit. Thus device models act as a bridge between the integrated circuit designers and those working for process technology development as shown in Fig. 1.

Any device model is categorized as numerical models and compact models. Numerical models are based on solving the partial differential equations describing the detailed physics of the device. These models are computationally intensive, complex and take a lot of computation time to solve the circuits. However, compact models describe the device in a simplified manner and also they are fast.

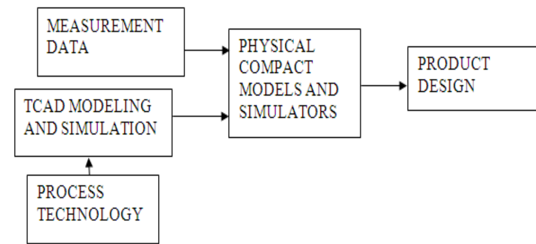


**Fig. 1.** Complete Flow of the Technology, Modeling and Design.

Some semiconductor industry standard compact models such as charge, potential and conductance based models are reviewed here:

### 1. Charge based MOSFET models

Charge based modeling approach is one of the basic and primitive modeling approaches. It is based on the computation of the inversion charge density in the MOSFET channel in terms of the terminal voltages i.e. gate and drain voltages [9]. These models are used in the initial version of the circuit simulator SPICE. These are also called as threshold voltage based models as they are based on defining all the parameters based on threshold voltage such as, drain current, voltage, drain saturation voltage etc. The most important advantage of this approach is its simplicity and flexibility to add features resulting from technology advancements. Additional parameters are introduced to take care of shrinking technology effects. The number of model parameters, therefore, increases as technology advancement takes place. This approach explains the behavior of the MOSFET in all regions of its operation such as weak, moderate and strong inversion separately and hence, it is also called a regional approach. So, these models require smoothe-ning parameters, these models are somewhat empirical in the interfacing regions and thus, the device behavior is not described accurately.

The prominent charge based models for the MOSFET are divided into mainly the first, second and third generation models depending on their level of complexity. The SPICE models Level 1, Level 2, Level 3 are called first generation SPICE Models [10, 11]. Level 1 model is used for gate lengths greater than 5 um [10]. Level 2 model (gate length < 5 um) [10] is much more complex than Level 1 model. It includes

mobility reduction due to high gate fields, threshold voltage reduction due to charge sharing in the channel and velocity saturation. Level 3 model (gate length <1 um) [10] is more empirical in nature. No additional effects as in Level 2 are added. The second generation models viz. BSIM1, HSPICE level 28, BSIM2 [10] are used for sub-half micron lengths. They have separate parameters for geometry dependence which are fitted with the parameters extracted for a particular dimension [10]. The third generation of charge based models is the advanced versions of the BSIM models. These are BSIM3, BSIM4 and BSIM5. These models are for deep sub-micron and nanometer scale MOSFETs. BSIM 4 [12] is an improvement over the BSIM 3 model. More physical effects have been taken in this model, such as, the inclusion of quantum behavior of the MOSFET like quantization of inversion layers empirically, quantum mechanical charge-layer-thickness model for both I-V and C-V characteristics. This model also includes the accurate gate direct tunneling model. It uses the approach of Lee and Hu [13] to model the gate direct tunneling current. BSIM 5 is used for sub-100 nm CMOS circuit simulation [14]. The poly-silicon gate depletion effects and empirical model of quantum mechanical effects are also included in this modeling approach.

MOS Model 9 [10] is a recent modeling approach by Phillips, Netherlands. This model is applicable at deep sub-micron region and attempts have been made to include the quantum mechanical effects also in this model.

## 2. Potential based MOSFET models

This model approach is based on accurate MOSFET device physics and therefore it is more accurate than the charge based models. Moreover, as the scaling continues to the nanoscale region, the charge based models become even more inaccurate in lower geometries as they are threshold voltage based which cannot be scaled down beyond a certain point.

It is based on the calculation of the potential in the channel of a MOSFET to determine the I-V and C-V characteristics. Most of the potential based models developed so far yield implicit relations of surface potentials. To solve them, difficult and complex iterative techniques are required. Due to these difficulties, the potential based approach to model MOSFETs has not found widespread use. Approximate solutions were also used earlier to calculate the surface potential in terms of gate to source voltage. These solutions lead to inaccurate model results. Now attempts are being made to find the exact solutions using the highly advanced software available. Therefore, it is expected that the next generation advanced compact MOSFET models would be surface-potential-based. The challenge is to develop practical and efficient surface-potential-based models which do not suffer from the limitations traditionally associated with this approach. Some of the models based on this approach are SP model by, Penn-state University, USA [15]. It requires up to 28 parameters. Quantum mechanical effects and poly-silicon gate depletion effect are also included in this model. The terminal voltages and other derived parameters, such as trans-conductance, can be accurately evaluated in all regions of MOSFET operation. Second model is HISIM (Hiroshoma-University, STARC IGFET MODEL [16-18] valid down to Sub-100 nm MOSFETs. Various short channel effects and quantum mechanical effects are included in this model.

## 3. Conductance based MOSFET model

This modeling approach is suitable for low power, short channel applications for analog design. It is known as EKV (Enz-Krummenacher-Vittoz) model [19] which has been developed by the Swiss Federal Institute of Technology, Switzerland. This model keeps substrate as the reference rather than the source as observed in the potential based and the charge based models. Due to its complexity, it is very less used for modeling purposes.

## 4. Models dedicated only to analyze quantum mechanical effects

First model is Hansch model [20]. It includes energy quantization empirically in the standard third generation charge based models. Second model is Vandort model [20] which is an improvement over the

hansch model in modeling equations. Another model which includes energy quantization empirically is the inversion charge model, a model based on the inversion electron concentration calculation involving the solution of surface potential in the channel [21].

In all the approaches mentioned above, attempts have been made to include the quantum mechanical effects in the MOSFET models. But most of the models that have come up are either empirical or semi empirical in nature. Therefore, there is a need for more physics based approach to accurately explain the behavior of the device, which takes into account the quantum mechanical effects in all the regions of operation.

It is therefore, clear that there is a need for developing suitable device models to account for quantum mechanical effects occurring at sub 100 nm gate lengths.

## IV. COMPARISON OF VARIOUS MOSFET MODELS

Table 1 shows the comparison summary of some of the advanced models discussed above. The table clearly shows that though most of the industry standard models include the quantum mechanical effects, yet these models are not capable of predicting the complete model at the sub 100 nm. This is because the models include quantum mechanical effects empirically or semi-empirically

**Table 1.** Comparison of Basic Two Compact Mosfet Models

| PROPERTY | Charge based models | Potential based models |
|---|---|---|
| Quantum Mechanical modeling approach | Basic model analytical, but an empirical correction of energy quantization effect has been done in relating band gap widening done with the inversion charge. | Basic model analytical, but an empirical correction of energy quantization effect has been done in relating band gap widening with the surface potential |

## V. QUANTUM MECHANICAL EFFECTS

As also discussed in section II, the major quantum mechanical effects occurring in a MOSFET at deep sub-micron and the nanometer scales are the gate oxide tunneling, energy quantization in substrate and poly-gate and source to drain tunneling.

### 1. Quantum mechanical tunneling from source to gate oxide

Due to aggressive technology scaling, the gate oxide thickness will be only around 2 nm in nanometer scale devices and thus called as ultra thin oxides. In the ultra thin oxide MOSFETs, the electrical field will be very high. Hence, the charge carriers in the channel will directly tunnel through the interface barrier to the gate oxide [22, 23].

### 2. Energy quantization in the substrate

As the MOSFET dimensions approach deep sub-micron and nanometer regions, the classical movement of the charge carriers is greatly affected by the non-classical behavior of electrons in the MOSFET. Due to aggressive scaling of the MOSFETs, the gate oxides are also scaled to nanometer regions. Also, the substrate doping is increased tremendously to negate the short channel effects at the deep sub-micrometer or nanometer scales. This results in very high electric fields in the silicon/silicon oxide interface and hence the potential at the interface becomes steep. This results in a potential well between the oxide field and the silicon potentials. During the inversion condition, the electrons are confined in this potential well. Due to confinement, the electron energies are quantized and hence the electrons occupy only the discrete energy levels. This results in the electrons residing in some discrete energy levels which are above the classical energy level by some fixed value of energy as shown in Fig. 2. This is more important as the oxide thickness becomes smaller with each technology generation.

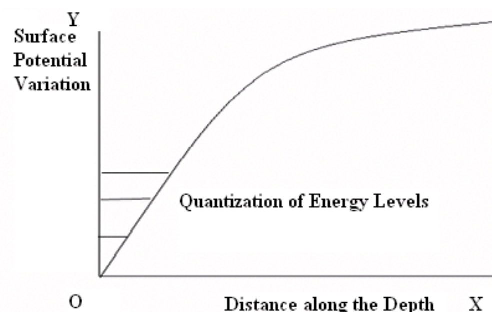


**Fig. 2.** Energy Quantization in the Substrate.

**3. Displacement of inversion charge density into the bulk**

Due to Energy Quantization, charge carrier density at the surface becomes less than the one expected from the classical analysis.

The charge distribution in case of classical charge distribution and Quantum Mechanical Charge distribution is shown in Fig. 3.

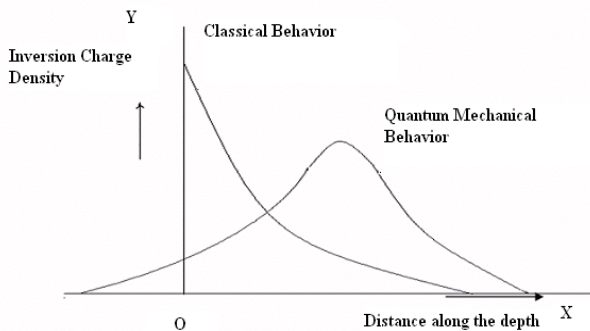


**Fig. 3.** Electron Concentration Distribution in the Silicon Substrate in Classical and Quantum Mechanical Cases.

**4. Poly-silicon gate depletion and poly-silicon gate energy quantization**

The depletion in the poly-silicon gate will cause a change in the effective oxide thickness and hence the effective gate capacitance [24]. The depletion region at the oxide/gate interface is also of quantum mechanical in nature and here also, the energy bands are split up or quantized [25].

**5. The quantum mechanical tunneling from source to drain in the substrate**

In sub 10nm channel length, the charge carriers are no longer restricted in the source potential well but start tunneling quantum mechanically through the barrier between the source and drain [26]. So, the gate voltage has no control over the MOSFET operation. This process is very important to model so as to continue with the scaling down process beyond 10 nm gate lengths.

**6. Threshold voltage and drain saturation voltage shift**

The shift in the surface potential due to the quantum mechanical effects changes the threshold voltage as the effective oxide thickness increases. Operating the MOSFET at such a low dimension will cause energy quantization in the oxide/substrate interface and also at the oxide/poly-silicon gate interface. The confining of the charged carriers in the potential well will raise the energy of the electrons because of the quantization of energy and electrons will occupy much higher energy levels for which a different potential is required to turn on the transistor. The energy quantization process will decrease the drain current also. The drain to source saturation voltage will fall under such conditions. So, it needs to be modeled.

It is therefore, important to account for the quantum mechanical effects in the design of nanometer scale MOSFETs. In this region, classical models are inadequate and lead to erroneous and misleading predictions of critical electrical behavior parameters, such as, the physical oxide thickness, threshold voltage, drive current, gate capacitance, etc.

## VI. QUANTUM MECHANICAL MOSFET MODELING APPROACHES

Accurate modeling of energy quantization in MOSFETs requires the solution of the Schrödinger and Poisson equations. One of the approaches to model the quantum mechanical problem is use approximations in solving these equations. These equations upon solving give the energies and the surface potentials which are caused by the energy quantization process in the substrate. These are then used to obtain the inversion charge densities further giving the accurate analytical equations for C-V and I-V analysis in sub 100 nm MOSFETs. Furthermore, analytical solutions are preferable because of their simplicity and fast computational speed. With these analytical solutions, it becomes easier to predict device scalability and circuit performance for future technology generations.

The other approach to tackle energy quantization problem is the numerical approach which deals with the actual self-consistent solution (i.e. compatible to a large extent with the solution of each other or with a minimum error in solution matching) of the Poisson's and the Schrödinger's equations. These can be solved in both one dimension and two dimensions.

The one-dimensional modeling primarily involves the analysis of the quantization of the energy levels and the variation of the surface potential only in the transverse direction i.e. along the depth of the channel or normal to the oxide/silicon interface. In this, the Poisson's and the Schrödinger's equations are solved only in one dimension. Traditional modeling approaches have been of one dimension self-consistent solving of Poisson's - Schrödinger's equations. This type of modeling approach is not sufficient to analyze the MOSFET at high drain voltages at which the two dimensional short channel effects such as drain induced barrier lowering etc. are prominent. Only very low drain voltages analysis can be done using one dimension modeling [27].

The two-dimensional modeling approach which is more complex, considers the quantization of the energy levels and the variation of the potential in the transverse as well as in the longitudinal directions. In this, the Poisson's and the Schrödinger's equations are solved in the direction normal to the oxide/silicon interface and also along the channel. Numerical solutions are obtained by solving Schrödinger equation and the Poisson equation using iterations. It is not used as an approach in standard circuit simulators because of its complexity and more computationally intensive due to iterative solutions but used as a reference because of its high accuracy.

As far as quantum mechanical oxide tunneling is concerned, the models available are either complex, numerical or lack theoretical details. The quantum mechanical direct source to drain tunneling in effective in sub-10 nm MOSFETs has never been modeled analytically previously as per the standard literature available. So, far only numerical models are available.

## VII. CONCLUSIONS

In this paper, a review of all MOSFET modeling approaches such as BSIM, SP, EKV etc. has been done, keeping in view the quantum mechanical effects occurring at the deep sub micron and the nanometer scale. Some issues and the approaches have also been given to tackle the problem of quantum mechanical effects in MOSFET modeling. In the end, it can be concluded that there is a strong need for an analytical model which accurately describes the MOSFET behavior at the nanometer scale in all regions of its operation.

## REFERENCES

[1] Schaller.R.R, "MOORE'S LAW: Past, Present and Future," *IEEE Spectrum*, pp.53-59, June, 1997.

[2] Moore.G. E, "Cramming more components onto integrated circuits," *Proceedings of the IEEE, Vol. 86, No.1*, pp.82-85, 1998.

[3] Zeitoff.P.M and Chung.J.E, "A perspective from the 2003 ITRS- MOSFET Scaling trends, Challenges and potential solutions," *IEEE Circuits and Devices Magazine*, pp.4-15, 2005.

[4] Zeitoff.P.M," Circuit, MOSFET and Front end Process Integration Trends and Challenges for the 180nm and below Technology Generations: An international Technology Roadmap for Semiconductor Perspective," *IEEE*, pp.23-28, 2001.

[5] Zeitoff.P.M, "Challenges and key potential technological innovations for scaling MOSFETs through the end of the roadmap," *IEEE*, pp.20-25, 2004.

[6] "International Technology Roadmap for Semiconductors (ITRS)," *Semiconductor Iinternational Association*, 2003.

[7] Wang. Y,"The Challenges for physical limitations in Si Microelectronics," *IEEE*, pp.25-30, 1998.

[8] Jing.W and Lundstrom.M, "Does source-to-drain tunneling limit the ultimate scaling of MOSFETs?," *Internationl Electron Device Meeting, Proceedings of*, pp.707-710, 2002.

[9] Chan. M, Xi. X, He. J, Cao. K.M, Dunga. M.V, Niknejad. A.M, Ko. P.K, Hu. C, "Practical compact modeling approaches and options for sub-.1 μm CMOS technologies," *Microelectronics Reliability, Journal of, Vol.43*, pp.399-404, 2003.

[10] Foty D, "MOSFET Modeling with SPICE, Principles and Practice," *Prentice Hall*, 1997.

[11] Foty D, "Perspectives on Analytical Modeling of Small Geometry MOSFETs in SPICE for Low Voltage/Low Power CMOS Circuit Design," *Analog Integrated Circuits and Signal Processing, Journal of, Vol.21*, pp.229-252, 1999.

[12] BSIM4.3.0 MOSFET Model- User's Manual - Department of Electrical Engineering and Computer Sciences,University of California, Berkeley, CA 94720.

[13] Lee W. C and Hu C.M, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling," *Electron Devices, IEEE Transactions on, Vol.48, No.7*, pp.1366-1373, July, 2001.

[14] Xi.X et al, "BSIM5 MOSFET Model," *IEEE*, pp.922-923, 2004.

[15] Gildenblat.G, Wang. H, Chen T.L, Gu. X, and Cai. X, "SP: An Advanced Surface-Potential-Based Compact MOSFET Model," *Solid state circuits, IEEE Journal of, Vol.39, No.9*, pp.1394-1406, Sept, 2004.

[16] Miura- Mattausch.M, Ueno.H, Mattausch. H.J,Ku-mashiro.S, Tamaguchi.T and Nakatama.N, "HiSIM: Self -Consistent Surface – Potential MOS model valid down to sub-100 nm technologies," MSM Workshop, April, 2002.

[17] HiSIM 1.1.1 User's manual, Semiconductor Technology Academic Research Centre (STARC)

[18] Suetake.M et al, "HiSIM: A drift Diffusion –Based Advanced MOSFET Model for Circuit Simulation with Easy Parameter Extraction," *IEEE*, pp.261-264, 2000.

[19] Enz C, Krummenacher F, Vittoz E, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuit Signal Processing, Journal of, Vol.8*, pp.83-114, 1995.

[20] Yu.Z, Dutton.R.W and Kiehl.R.A, "Circuit/Device Modeling at the Quantum level," *Electron Devices, IEEE Transactions on, Vol.47, No.10*, pp.1819-1825, Oct, 2000

[21] Cheng. Y, "ICM- An analytical inversion charge model for accurate modeling of thin gate oxide MOSFETs," *IEEE*, pp. 109-112, 1997.

[22] Lo. S, " Quantum –Mechanical Modeling of Electron tunneling Current from the Inversion Layer of Ultra- Thin – Oxide nMOSFET's," *IEEE Electron Device Letters, Vol.18, No.5*, pp.209-211, May, 1997.

[23] Yang . N, Henson. W.K, Hauser .J.R, Wortman. J.J, " Modeling Study of Ultrathin gate Oxides Using Direct tunneling Current and Capacitance – Voltage Measurements in MOS Devices," Electron Devices,IEEE Transactions on, Vol.46, No.7, pp. 1464-1471, July, 1999.

[24] Rios.R et.al, "An Analytical Polysilicon depletion effect model for MOSFETs," *IEEE Electron Device Letters, Vol.15*, pp.129-131, 1994.

[25] Spinelli. A.S, Pacelli. A and Lacaita. A.L, "Polysilicon Quantization Effects on the Electrical Properties of MOS Transistors," *Electron Devices, IEEE Transactions on, Vol.47, No.12*, pp.2366-2371, Dec, 2000.

[26] Oda. S and Ferry. D, "The Scaling limit of MOSFETs due to direct Source –Drain tunneling in silicon nanoelectronics, Taylor and Francis, Boca Raton, 2006

[27] Ip. B. K and Brews.J. R, "Quantum effects upon drain current in a biased MOSFET," *Electron Devices, IEEE Transactions on, Vol.45, No.10*, pp.2213-2221, 1998.

**Amit Chaudhry** was born in India, in 1976. Er. Amit Chaudhry completed his M.E.(Electronics) from Panjab Engineering College, Panjab University, Chandigarh in 2000. He joined Panjab University, University Centre for instrumentation and microelectronics October, 2002. He was responsible for teaching and research in VLSI and microelectronics to post graduate students. He has submitted his Phd (Microelectronics) thesis recently. His research areas include device modeling for sub 100nm MOSFETS. He is a life member of various societies in the area of microelectronics. Currently he is Assistant Professor(Microelectronics), University Institute of Engineering and Technology, Panjab University, Chandigarh. He has more than 10 publications in Journals/Conference proceedings. His research interests include device physics of nanometer MOSFETs, Semiconductor memory technology and design.

**Dr. J. N. Roy** completed his Ph.D. (Materials Science) from IIT-Kharagpur in 1984. He joined Semiconductor Complex Ltd. (SCL), now known as Semi-Conductor Laboratory (SCL) a VLSI & MEMS manufacturing and R&D facility, in Jan 1984. He was responsible for VLSI and MEMS related activities of the organization; including Process Technology Development, Design, Fabrication, Testing and Assembly. During the period between October 2004 and September 2006, he was with Panjab University as Professor (Microelectronics). Currently he is Vice President (R&D) of Solar Semiconductor Pvt. Ltd. and responsible for R&D, Engineering and technology related activities of the organization. He was a consultant to Analog Integration Corporation- USA. He has conducted short training courses for faculty, researchers and corporate houses. He has more than 60 publications in Journals/Conference proceedings. He is a senior member IEEE, Fellow INAE and Fellow IMS. He has received best innovator award from EDN-Asia. He is an INAE Distinguished Visiting Professor.