A New Approach for Accurate RTL Power Macro-Modeling

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***Abstract*—Register transfer level power macro-modeling is well known as a promising technique for accurate and efficient power estimation. This paper proposes effective approaches based on the table-based method for the RTL power macro-modeling. The new parameter *SD*, which characterizes the distribution of switching activities for each gate in the circuit, is one of the contributions. The new parameter *SD* has strong correlation with power consumption. We also propose an accurate table reference method considering the circuit characteristics. The table reference method is applicable for every table-based method and outputs more accurate power value. The experimental results show that the combination of the proposed methods reduces max error 30.36% in the best case, comparing conventional methods. The RMS error is also improved 1.70% in the best case.**

***Index Terms*—Power macro-model, power estimation, RTL, parameterization, table reference**

I. INTRODUCTION

Embedded system design is becoming more and more complicated since high performance is often required under various constraints. Especially portable systems are surrounded by strict constraints such as performance, power consumption, etc., and designers have to take into account such constraints to design the systems in short time.

To achieve both high design productivity and energy efficiency, the power estimation in high abstraction level is necessary. Usually, the power is estimated in gate level, but the estimation often takes long time. Then the power estimation in register transfer level (RTL) is an aggressive challenge for fast and accurate power estimation.

The RTL power macro-modeling for fast and accurate power estimation includes mainly two methods: the equation-based method and the table-based method. The equation-based method estimates the power consumption by the equation which represents the power model [1]. The equation-based method enables fast power estimation, but the estimation accuracy is low. In contrast, the table-based method is a major method for RTL power estimation [2-5]. The table-based method models power consumption with some parameters which characterize statistical information of input or output data. Once the power library called look-up table (LUT) is constructed, the power consumption is easily estimated by the table reference. On the other hand, several methods which combine the equation-based methods and the table-based methods also have been proposed [6, 7].

In this paper, we propose the new parameter ***SD*** for accurate power estimation. The new parameter ***SD*** characterizes the statistical information of the internal circuit activity. We also propose the new table reference method based on circuit characteristics. The new table reference method is applicable for every table-based method and outputs more accurate power value.

Rest of the paper is organized as follows: section II introduces an overview of RTL power macro-modeling, and section III proposes the new power estimation methods including the new parameter ***SD*** and the new table reference method. Section IV shows the experimental results and section V concludes this paper.

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II. RTL POWER MACRO-MODELING

1. Overview

This section shows an overview of the table-based RTL power macro-modeling. The power estimation flow of the table-based method is divided into two steps: the table construction step and the table look-up step. In the table construction step, the look-up table (LUT) which is a power library is constructed as shown in Fig. 1. The table construction step includes two parts: parameter extraction from input data (Parameterization) and power calculation by gate level simulation. The extracted parameters represent the input data characteristics, and the power consumption is estimated with these parameters. The combination of the parameter set and the calculated power value are regarded as one entry. The parameters P_{in}, D_{in}, S_{in}, and T_{in} shown in Fig. 1 are conventional parameters, and we choose them as an example. Exploring the best combination of the parameters and a development of new parameters are important for the accurate power estimation at the table construction step.

After the table construction step, the power estimation is available by the table reference. Fig. 2 shows the power estimation flow using the constructed LUT. In the table look-up step, the constructed LUT is referred with the parameters extracted from the input data for the power estimation. Then, one entry having the most proximal feature with the input data is selected by a metric called *distance*, and the corresponding power value is output as the estimated power. The distance is calculated for each entry and the entry having the shortest distance is selected. Thus the estimation accuracy would be improved by applying the table construction flow to various input data as much as possible previously. For more details of a distance calculation is found in subsection 3., section II.

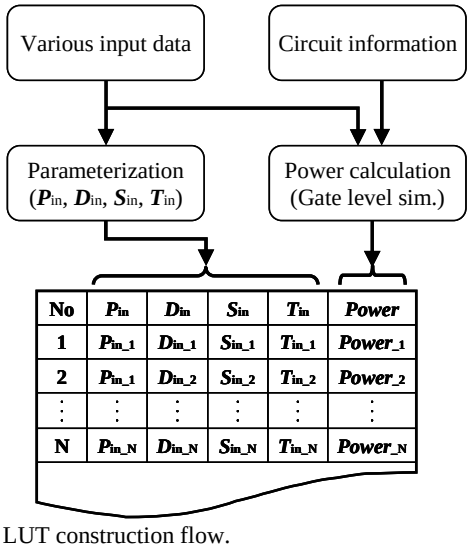


Fig. 1. LUT construction flow.

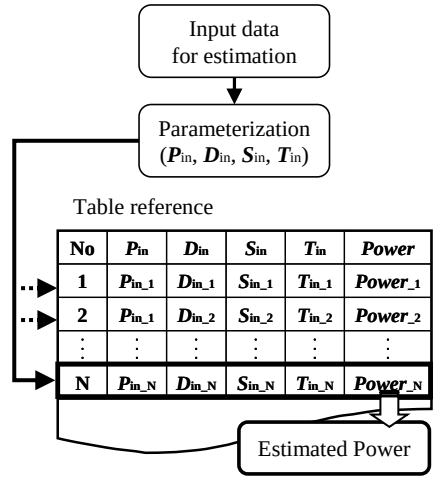


Fig. 2. Power estimation flow.

2. Macro-Model Parameters

To realize efficient RTL power macro-modeling, parameter selection is quite important, and various researches have been done [1-8].

Gupta, et al. [1, 2] uses four parameters: the average input signal probability P_{in}, the average input transition density D_{in}, the average output signal density D_{out}, and the average input correlation coefficient SC_{in}. P_{in} and D_{in} are defined as the probability of existing "1", and the probability of the signal transitions ("0" → "1" and "1" → "0") in input data, respectively. These models enable accurate power estimation. However, extracting D_{out} requires a logic simulator to calculate output data, and this operation often takes long time for very large scale circuits. To solve the problem, Bernacchia, et al. [3] proposed the two parameters extracted without logic simulation. The proposed parameters are the spatial correlation metric S_{in} and the temporal correlation metric T_{in}. These models improve estimation accuracy with the extracting parameters only from input data. More details are presented in [3].

As shown in Fig. 3, we assume data which is input to the circuit block. Let M, N, and x_{ij} shown in Fig. 3 be the number of primary input patterns to the circuit, the

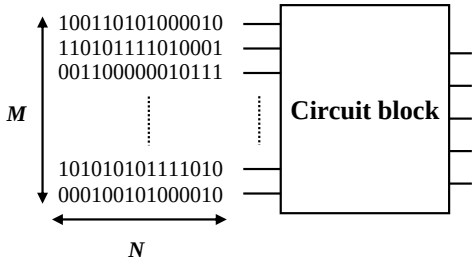


Fig. 3. RTL circuit block and input data.

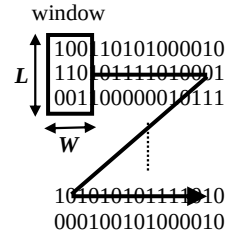


Fig. 4. Characterization of parameter ST_{in}.

length of input vectors, and bit ("0" or "1") of input pin ***j*** at input vector ***i***, respectively. Then parameter P_{in}, D_{in}, S_{in}, and T_{in}, which are major parameters for power macro-modeling, are defined as follows:

$$P_{in} = \frac{\sum_{j=1}^{M}\sum_{i=1}^{N} x_{ij}}{M \times N} \quad (1)$$

$$D_{in} = \frac{\sum_{j=1}^{M}\sum_{i=1}^{N-1} x_{ij} \oplus x_{(i+1)j}}{M \times (N-1)} \quad (2)$$

$$S_{in} = \frac{\sum_{j=1}^{M}\sum_{k=1}^{M}\sum_{i=1}^{N} x_{ij} \oplus x_{ik}}{N \times M \times (N-1)} \quad (3)$$

$$T_{in} = \frac{\sum_{j=1}^{M}\sum_{L-1}^{N-L+1} w_j \otimes x_j}{N \times M} \quad (4)$$

In our previous research, we proposed the spatial and temporal correlation coefficient ST_{in} [5]. The parameter ST_{in} characterizes both aspect of spatial and temporal from input data at the same time. The experimental result in [5] demonstrated that the ST_{in} enables to reduce parameter extraction time and LUT size, without losing estimation accuracy. The parameter ST_{in} is defined as a window which scans input data shown in Fig. 4.

Let ***L*** and ***W*** be the length and the width of the window, then the parameter ST_{in} which is defined as follows [5]:

$$ST_{in} = \frac{\sum_{i=(L-1)/2}^{M-(L-1)/2}\sum_{j=(W-1)/2}^{N-(W-1)/2} b_{ij} \oplus x_{lw}}{(N-W+1)\times(M-L+1)}, \quad (5)$$

where b_{ij} and x_{lw} are the center value of the window and its neighboring value (***l***: 1 to ***L***, ***w***: 1 to ***W***), respectively. The ST_{in} is extracted by checking the correlation between b_{ij} and x_{lw} in all input signal as shown in Fig. 4. Empirically, the optimal window size (***L***, ***W***) is known as (3, 3).

3. Power estimation from LUT

The table reference method in the table look-up step is also important for accurate power estimation. This section explains important metric *distance* to find out proximal entry from a LUT. This section describes one of the effective distance calculation proposed in our previous work [5].

Let n_p, p^i_{in}, and p^i_{LUT} be the number of parameter types, *i*-th parameter extracted from input data, and *i*-th parameter in one entry in the LUT, respectively. The distance *dist* is calculated as follows:

$$dist = \sqrt{\frac{1}{n_p}\sum_{i=0}^{n_p-1}(dp_i)^2} \quad (6)$$

where dp_i is a ratio for *i*-th parameter, and defined as follows:

$$dp_i = 1 - \frac{p^i{}_{in}}{p^i{}_{LUT}} \quad (7)$$

The distance is defined with a ratio in each parameter and RMS to define the *dist*. In the table look-up step, the entry in the LUT which has the shortest distance with the extracted parameters is selected, and the corresponding power value is output as the estimated power.

III. Accurate RTL Power Estimation

1. New parameter SD

In this section, we propose the new parameter ***SD*** called the switching probability distribution for more accurate power estimation. The parameter ***SD*** characterizes the switching activities of internal circuit [8].

Let V_{dd} and f be supply voltage and clock frequency, respectively. Dynamic power $P_{dynamic}$ of a CMOS circuit is calculated as follows:

$$P_{dynamic} = \sum_i C_i V_{dd}^2 \alpha_i \ , \qquad (8)$$

where C_i and α_i are capacitance and switching probability for the gate i. The switching probabilities of each gate α_i have the most influence on power consumption because α_i varies from the aspect of the input data into the circuit. For example, when we focus on one gate, having large capacitance, the gate consumes low power in case of low switching. The parameter ***SD*** characterizes where the gate have been switching frequently, and aims at improving the estimation accuracy.

Fig. 5 shows the switching distribution of c432 circuit from ISCAS85 benchmark. All gates on c432 circuit are arranged by the depth from the input pin side, and the gates which are on the same depth are placed randomly. The data is input from "input pin side," and the calculated data is output to "output pin side." High and dark parts are the places where the gates have been switching frequently. Obviously, the switching activity is depending on the place in the circuit in Fig. 5 and this inspires a concept of the new parameter ***SD***.

Let α_d, N_d, and N_{total} be the average switching probability at depth d, the number of gate at depth d, and the total number of gate in the circuit, respectively. The new parameter ***SD*** is defined as follows:

$$SD = \frac{\sum_{d=1}^{Depth} \alpha_d \cdot N_d}{N_{total}}, \qquad (9)$$

where ***Depth*** means maximum depth of the circuit.

The ***SD*** is obtained for each input data by gate level simulation in the table construction step. On the other hand, when we estimate power consumption with the ***SD***, the average switching probability α_d is necessary to calculate ***SD*** value. This means that the time consuming gate level simulation is necessary to calculate the ***SD*** for RTL power estimation. To obtain the corresponding ***SD*** value without gate level simulation, first, the ***SD*** value is estimated by the LUT reference with the parameters such as P_{in} and D_{in} except ***SD***. Then, the power consumption is obtained by the LUT reference with the parameter P_{in}, D_{in}, and the estimated ***SD*** again. The estimated ***SD*** affects the distance calculation in LUT reference, and realizes accurate power estimation.

Fig. 6 shows the correlation between the parameter ***SD*** and power consumption calculated in a gate level for c5315 of ISCAS85 benchmark. The correlations with power consumption of 8 circuits of ISCAS85 benchmark were 0.98 - 0.99. This preliminary experimental result denotes that the parameter ***SD*** has the strong correlation with power consumption. By using the parameter ***SD*** at the table reference, more accurate value is selected as the estimated power.

2. New LUT reference method

This section describes the new table reference method for more accurate power estimation in the table look-up step. Each parameter has different correlation with power consumption, and the correlation strength depends on target circuits.

Fig. 7 shows an example of the switching activities for AND gates, and Fig. 8 shows an example for OR gates. In RTL power macro-modeling, the number of switching gates is critical for accurate power estimation. When we

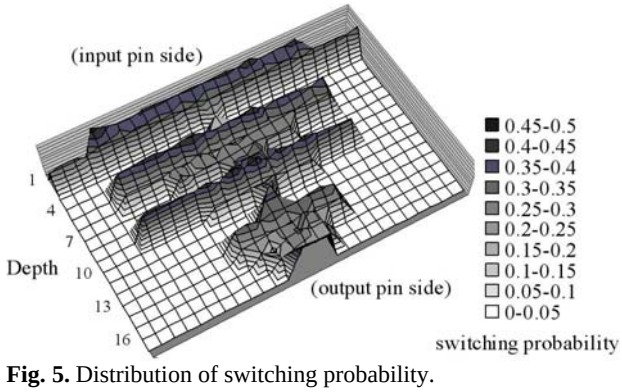


Fig. 5. Distribution of switching probability.

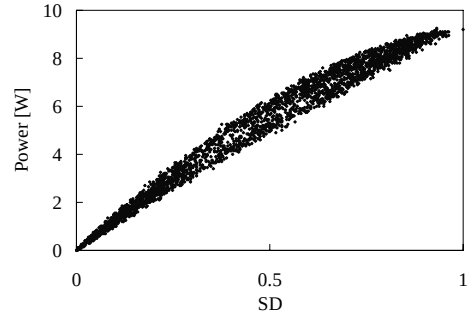
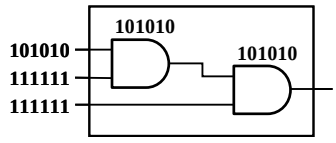
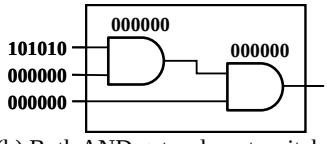


Fig. 6. Correlation between power and *SD*.

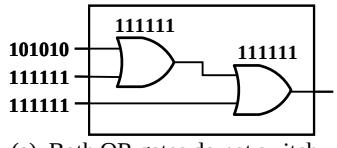


(a) Both AND gates switch every cycle.

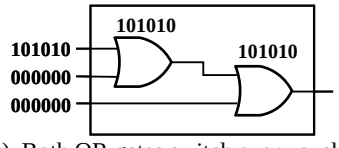


(b) Both AND gates do not switch.

Fig. 7. Switching activities for AND gates.



(a) Both OR gates do not switch.



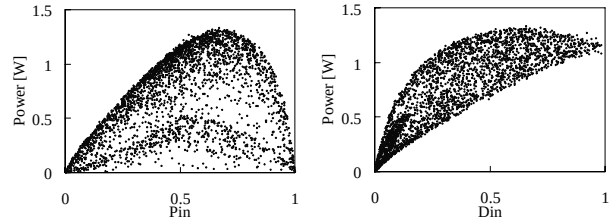
(b) Both OR gates switch every cycle.

Fig. 8. Switching activities for OR gates.

assume the input data shown in Fig. 7(a), both AND gates switch every cycle. After the input data are changed to the data as shown in Fig. 7(b), AND gates do not switch any more. However, in OR gates case, the switching behavior is completely different. In OR gates case shown in Fig. 8(a) both OR gates do not switch for the same input data as Fig. 7(a), but both OR gates switch every cycle shown in Fig. 8(b) for the input data which do not activate any AND gates.

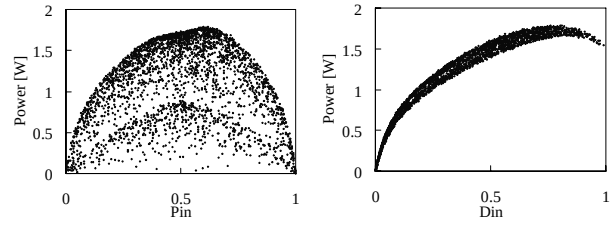
The power consumption is estimated with statistical information of input data in the table based method. The previous example shows that the statistical information of input data does not reflect switching activity directly, and we should consider the circuit characteristics at the same time.

The accurate power estimation needs the parameters having a strong correlation with the power consumption. Fig. 9 and Fig. 10 show the correlation between the parameter ($\boldsymbol{P_{in}}$ or $\boldsymbol{D_{in}}$) and power consumption for c880 and c1355 of ISCAS85 benchmark, respectively. Notice that strength of the correlation depends on target circuits. For example, Fig. 9(b) and Fig. 10(b) show the correlation between the parameter $\boldsymbol{D_{in}}$ and power. Obviously c1355 benchmark has stronger correlation than c880, and the



(a) $\boldsymbol{P_{in}}$ – Power (b) $\boldsymbol{D_{in}}$ – Power

Fig. 9. Correlation between parameters and power for c880.



(a) $\boldsymbol{P_{in}}$ – Power (b) $\boldsymbol{D_{in}}$ – Power

Fig. 10. Correlation between parameters and power for c1355.

parameter $\boldsymbol{D_{in}}$ on c1355 is reliable to power estimation.

Our idea for the table reference is based on the difference of the correlation strength. The parameter which has the strong correlation with the power should be respected in the table reference. We regard such difference of the correlation with the power consumption as the circuit characteristics.

Let $corr_i$ be a correlation coefficient between i-th parameter and the power consumption, proposed distance $dist_{prop}$ is defined as follows:

$$dist_{prop} = \sqrt{\frac{1}{n_p}\sum_{i=0}^{n_p-1}\left\{corr_i \cdot (dp_i)^2\right\}} \qquad (10)$$

Using $dist_{prop}$ for the table reference, the parameters having a strong correlation with the power tend to be weighted, and the estimation accuracy is drastically improved.

Let $\boldsymbol{\sigma_{param\_i}}$, $\boldsymbol{\sigma_{power\_i}}$, and $\boldsymbol{s_i}$ be the standard deviation of i-th parameter, the standard deviation of the power consumption, and the covariance between i-th parameter and the power consumption, respectively. Then the correlation coefficient $\boldsymbol{corr_i}$ between i-th parameter and the power consumption is defined as follos:

$$corr_i = \frac{s_i}{\sigma_{param\_i} \cdot \sigma_{power\_i}} \qquad (11)$$

IV. EXPERIMENTAL RESULTS

In order to demonstrate an efficiency of the proposed methods for RTL power macro-modeling, we perform the experiments with 8 circuits from ISCAS85 benchmark. Each benchmark circuit is logic circuit. For each logic circuit from ISCAS85 benchmark, we set the practical capacitances for all logic gates, and evaluate the methods by the errors between the gate level simulation result and the proposed RTL power estimation.

1. Experimental result of new parameter SD

This section shows the experimental results of new parameter ***SD***. We estimate the power consumption of the 8 logic circuits from ISCAS85 benchmark by 3 ways: gate level simulation, RTL power estimation with conventional parameter set (***P_{in}***, ***D_{in}***, ***ST_{in}***), and RTL power estimation with a parameter set (***P_{in}***, ***D_{in}***, ***SD***), which includes new parameter ***SD***. To perform RTL power estimation, each LUT is constructed by 3,000 input data sets. Then, we perform RTL power estimation for 1,000 input data sets, and calculate average RMS error between each RTL power estimation results and the gate level simulation result.

Fig. 11 shows a comparison of RMS error between the result from (***P_{in}***, ***D_{in}***, ***ST_{in}***) and the result from (***P_{in}***, ***D_{in}***, ***SD***). Fig. 11 shows that the new parameter ***SD*** improves RMS error in 7 cases. The average improvement rate of RMS error using (***P_{in}***, ***D_{in}***, ***SD***) is about 10% comparing with (***P_{in}***, ***D_{in}***, ***ST_{in}***). The average RMS error of the proposed method is 4.5% from 8 benchmark circuits.

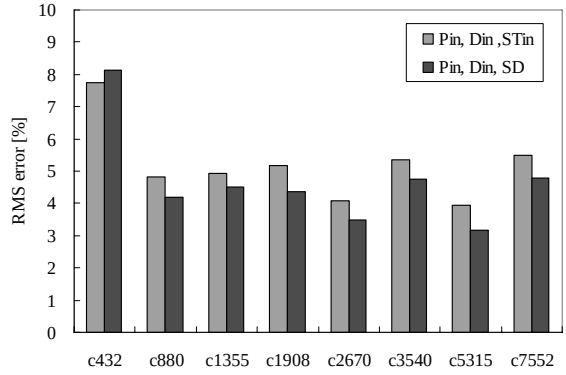


Fig. 11. Comparison of RMS error between (***P_{in}***, ***D_{in}***, ***SD***) and (***P_{in}***, ***D_{in}***, ***ST_{in}***).

2. Experimental result of new table reference method

This section shows an efficiency of new table reference method. We evaluate the table reference method using the new *distance* calculation comparing with conventional method described in Eq. (6) [5].

Table 1 shows correlation coefficients between the power consumption and each parameter for ISCAS85 benchmark circuits. As shown in Table 1, the correlation coefficient depends on the parameter and each circuit.

Table 2 shows a comparison of RMS and max error between conventional and proposed table reference methods for each benchmark circuit. The power is estimated by the RTL power macro-modeling with parameter set (***P_{in}***, ***D_{in}***, ***ST_{in}***). As shown in Table 2, the proposed method improves max error for almost all benchmarks, and maximally improved about 20% for c5315 benchmark. Table 2 also shows that the proposed method improved the RMS error for all benchmarks, and maximally improved the RMS error about 1%.

To analyze more details, we have made a histogram of the estimation error for the c5315 as shown in Fig. 12. The histogram indicates that the proposed method increases the quite good estimation results whose error

Table 1. Correlation coefficient with power consumption of each parameter for ISCAS85 benchmark circuits

Circuit	#Gate	Correlation coefficient with power			
		P_{in}	D_{in}	ST_{in}	SD
c432	160	0.090	0.966	0.795	0.997
c880	383	0.373	0.843	0.749	0.996
c1355	546	0.076	0.932	0.841	0.997
c1908	880	0.038	0.971	0.854	0.999
c2670	1,192	0.008	0.958	0.863	0.993
c3540	1,669	0.106	0.938	0.851	0.997
c5315	2,307	0.060	0.960	0.866	0.988
c7552	3,513	0.018	0.944	0.843	0.996

Table 2. Comparison of RMS and max error between conventional and proposed table reference methods using ***P_{in}***, ***D_{in}***, and ***ST_{in}***

Circuit	Conventional table reference method		Proposed table reference method	
	RMS [%]	Max [%]	RMS [%]	Max [%]
c432	7.39	42.57	7.10	42.57
c880	6.44	54.34	6.35	54.34
c1355	3.85	35.29	3.33	25.99
c1908	5.86	51.33	5.16	33.75
c2670	5.86	50.86	5.19	45.67
c3540	7.31	59.71	6.48	56.78
c5315	5.08	61.42	4.25	39.13
c7552	6.84	55.84	5.65	37.55

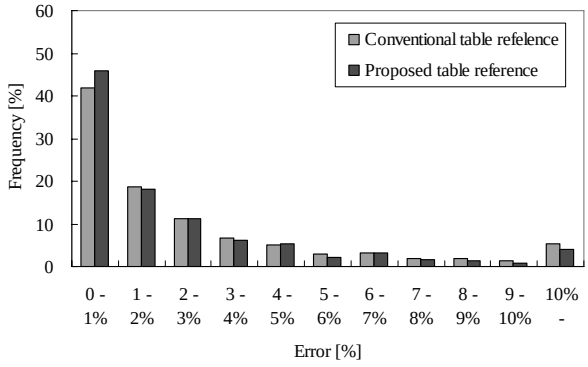


Fig. 12. Comparison of histogram of estimation error for c5315 using P_{in}, D_{in}, and ST_{in}.

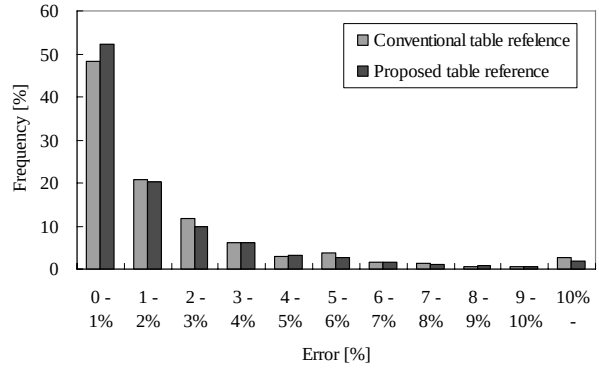


Fig. 13. Comparison of histogram of estimation error for c1355 using P_{in}, D_{in}, and SD.

rates are less than 1%. On the other hand, proposed method decreases the quite bad estimation results whose error rates are more than 10%. Therefore, proposed method improves quality of power estimation drastically.

To demonstrate an efficiency of the new parameter ***SD*** and the new table reference method, we applied the proposed table reference method to estimate the power consumption for the parameter set (P_{in}, D_{in}, SD).

Table 3 shows the comparison of RMS and max error between conventional and proposed table reference methods for each benchmark circuit. The power is estimated by the RTL power macro-modeling with parameter set (P_{in}, D_{in}, SD). This result provides that the proposed method also improves the max error for almost all benchmarks, and maximally improved about 50% for the c1355 benchmark. The RMS error is also improved for all benchmarks, and maximally improved about 1.5%.

Fig. 13 shows the error histogram for the c1355 in Table 3. The histogram indicates the proposed method increases quite good estimation results whose error rates are less than 1%. On the other hand, the proposed method decreases worse estimation results whose error rates are more than 4%. Therefore, the proposed method improves the quality of power estimation drastically.

From both experimental results for two parameter set (P_{in}, D_{in}, ST_{in}) and (P_{in}, D_{in}, SD), the proposed table reference method is able to applicable for various RTL power macro-modeling. Especially, as shown in Fig. 12 and Fig. 13, proposed method raises the level of whole estimation accuracy. Additionally, as shown in Table 2 and 3, combination of the new parameter ***SD*** and the new table reference method maximally reduces the max error about 30.36% and the RMS error about 1.70%.

Table 3. Comparison of RMS and max error between conventional and proposed table reference methods using P_{in}, D_{in}, and SD

Circuit	Conventional table reference method		Proposed table reference method	
	RMS [%]	Max [%]	RMS [%]	Max [%]
c432	7.47	73.89	7.29	73.89
c880	5.98	40.28	5.62	31.86
c1355	4.60	77.99	3.18	29.70
c1908	6.07	78.99	5.48	69.98
c2670	5.70	56.91	4.17	23.00
c3540	6.42	57.57	6.21	57.57
c5315	4.13	33.09	3.84	31.06
c7552	7.28	86.34	6.10	51.39

3. Scalability analysis of proposed method

Now a day, various RTL blocks have been designed, and the RTL block is wide variety of the number of gates. In this section, we analyze a scalability of proposed RTL power macro-modeling and the estimation accuracy. To perform the RTL power macro-modeling, the most time consuming part is the LUT construction. Fig. 14 shows the LUT construction time and the RMS error between

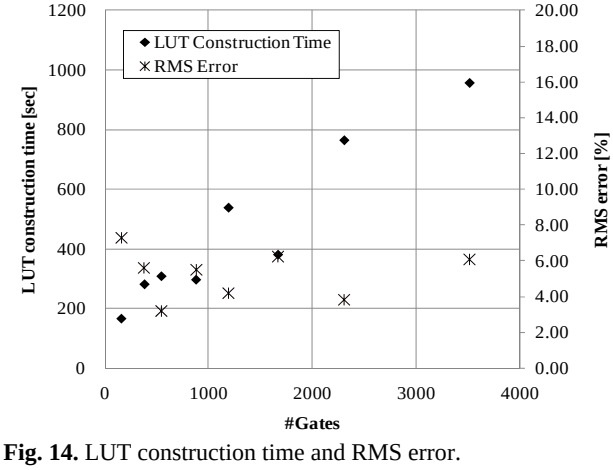


Fig. 14. LUT construction time and RMS error.

the gate level simulation and the RTL power macro-modeling using (P_{in}, D_{in}, SD). X-axis is the number of gate. The largest benchmark circuit is c7552, and the number of gates is 3,513.

We can see that the LUT construction time increases depending on the number of gates. However, it is expected that the LUT construction time for even 10 times larger RTL block than c7552 takes still acceptable time in terms of its computational complexity. Moreover, at least in our experiments, the estimation error does not depend on the number of the gates, and it is expected that an estimation error is still acceptable.

V. CONCLUSIONS

In this paper, we have proposed the new RTL power macro-modeling for an accurate power estimation. We have two contributions: the new parameter ***SD*** which characterizes the switching activities and the new table reference method based on the circuit characteristics. The parameter ***SD*** has a strong correlation with the power consumption, and the experimental results show that the RMS error is improved about 10% in average for ISCAS85 benchmark circuits. On the other hand, the new table reference method based on the circuit characteristics improves the RMS error for all benchmark circuits. The proposed table reference method is applicable for every table-based method. Combination of the proposed two methods maximally improves max error 30.36% and RMS error 1.70%. These experimental results are performed on the logic circuits having practical capacitances, and a back annotation of the real capacitance distribution after a place and routing realizes more accurate and more practical power estimation.

Proposed RTL power macro-modeling mainly targets simple combinational circuit, and another circuit models such as sequential circuit, analog circuit, custom circuit, and memory are out of scope. Sequential circuit is composed of combinational circuit and registers, and average transition density of registers is necessary to estimate power consumption of sequential circuit. Proposed RTL power macro-modeling is an important fundamental research for the power estimation of the sequential circuit. The other circuit models such as analog circuit, custom circuit, and memory are completely different with logic circuit, and different power models are necessary. Combining appropriate power models for each circuit model, more practical power estimation method is available.

At the same time, typical large RTL blocks are usually composed of some functional blocks, and the hierarchical power estimation method is another important future work. The LUT construction for large RTL blocks takes long time, and the hierarchical method is expected to perform fast and more accurate RTL power estimation.

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