Two Phase Clocked Adiabatic Static CMOS Logic and its Logic Family

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Abstract—**This paper proposes a two-phase clocked adiabatic static CMOS logic (2PASCL) circuit that utilizes the principles of adiabatic switching and energy recovery. The low-power 2PASCL circuit uses two complementary split-level sinusoidal power supply clocks whose height is equal to V_{dd}. It can be directly derived from static CMOS circuits. By removing the diode from the charging path, higher output amplitude is achieved and the power consumption of the diode is eliminated. 2PASCL has switching activity that is lower than dynamic logic. We also design and simulate NOT, NAND, NOR, and XOR logic gates on the basis of the 2PASCL topology. From the simulation results, we find that 2PASCL 4-inverter chain logic can save up to 79% of dissipated energy as compared to that with a static CMOS logic at transition frequencies of 1 to 100 MHz. The results indicate that 2PASCL technology can be advantageously applied to low power digital devices operated at low frequencies, such as radio-frequency identifications (RFIDs), smart cards, and sensors.**

Index Terms—**Adiabatic logic, low-power, two phase clocked, energy recovery, split-level, power clock generator**

I. INTRODUCTION

In recent times, researchers have focused on increasing clock and logic speeds in order to enhance the performance of mobile and wireless devices; hence, it has become important to design integrated circuits (ICs)

that help achieve high energy efficiency. The power consumption in digital circuits, which mostly use complementary metal-oxide semiconductor (CMOS) devices, is proportional to the square of the power supply voltage; therefore, voltage scaling is one of the important methods used to reduce power consumption. To achieve a high transistor drive current and thereby improve the circuit performance, the transistor threshold voltage must be scaled down in proportion to the supply voltage. However, scaling down of the transistor threshold voltage V_t results in significant increase in the subthreshold leakage current [1].

Recently, adiabatic computing has been applied to low-power systems, and several early adiabatic logic families have been proposed [2-5] emphasizing on the energy recovery principle. Then, several other papers on adiabatic logics have been published [6-15] for low-power logic applications. The energy dissipated in adiabatic circuits is considerably less than that in static CMOS circuits; hence, adiabatic circuits are promising candidates for low-power circuits that can be operated in the frequency range in which signals are digitally processed. However, diode-based logic families [3, 4, 6, 9, 11, 14, 15] have several disadvantages such as output amplitude degradation and power dissipation across the diodes in the charging path.

In this paper, we propose a two-phase clocked adiabatic static CMOS logic (2PASCL) [16] circuit to achieve low power consumption; we also compare its power consumption with that of a conventional CMOS circuit.

A novel method for reducing the power dissipation in a 2PASCL circuit involves the design of a charging path without diodes. In such a case, current flows only through the transistor during the charging. Thus, a 2PASCL circuit is different from other diode-based

adiabatic circuits in which current flows through both the diode and transistor. By using the aforementioned 2PASCL circuit, we can achieve high output amplitudes and reduce power dissipation. In addition, in order to minimize the dynamic power consumption in this circuit, we apply a split-level sinusoidal driving voltage.

The remainder of this paper is divided into five sections. Section II describes the differences between CMOS and adiabatic logic circuits. In Section III, the structure and operation of a 2PASCL circuit are explained. Section IV describes the simulation of a 2PASCL inverter and other logic gates and also provides a comparison between the power dissipations in 2PASCL and CMOS circuits. In Section V, the power clock generator circuit is introduced. Section VI discusses the advantages and disadvantages of 2PASCL, while Section VII includes concluding remarks.
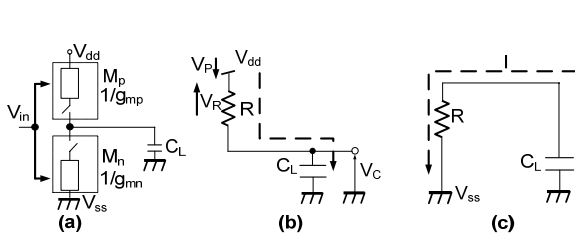
II. CMOS CIRCUITS VIS-A-VIS ADIABATIC LOGIC CIRCUITS

1. CMOS Circuits

Power dissipation in conventional CMOS circuits primarily occurs during device switching. As shown in Fig. 1, both pMOS and nMOS transistors can be modeled by including an ideal switch in series with a resistor in order to represent the effective channel resistance of the switch and the interconnect resistance.

The pull-up and pull-down networks are connected to the node capacitance C_L, which is referred to as the load capacitance in this paper.

When the logic level in the system is "1," there is a sudden flow of current through R. $Q=C_LV_{dd}$ is the charge supplied by the positive power supply rail for charging C_L to V_{dd}. Hence, the energy drawn from the power supply is $Q \cdot V_{dd}=C_LV^2_{dd}$ [10]. If it is assumed that the energy drawn from the power supply is equal to that supplied to C_L, the energy stored in C_L becomes one-half the supplied energy, i.e., $E_{stored}=0.5C_LV^2_{dd}$.

The remaining energy is dissipated in R. The same amount of energy is dissipated during discharging in the nMOS pull-down network when the logic level in the system is "0." Therefore, the total amount of energy dissipated as heat during charging and discharging is

$$E_{total} = E_{charge} + E_{discharge}$$
$$= 0.5C_LV^2_{dd} + 0.5C_LV^2_{dd} = C_LV^2_{dd} \tag{1}$$

From the above equation, it is apparent that the energy consumption in a conventional CMOS circuit can be reduced by reducing V_{dd}. By decreasing the switching activity in the circuit, the power consumption ($P= dE/dt$) can also be proportionally suppressed.

2. Adiabatic Logic Circuits

A. Adiabatic Logic Principle

Adiabatic switching is commonly used to minimize energy loss during charging/discharging. The word "adiabatic" (Greek *adiabatos*, which means impassable) indicates a state change that occurs without heat loss or gain. During adiabatic switching, all the nodes are charged or discharged at a constant current in order to minimize power dissipation. This is accomplished by using AC power supplies to initially charge the circuit during specific adiabatic phases and then discharge the circuit to recover the supplied charge. The principle of adiabatic switching can be best explained by contrasting it with the conventional dissipative switching technique.

Fig. 2 shows the manner in which energy is dissipated during a switching transition in adiabatic logic circuits. In contrast to conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the use of a time-varying voltage source

Fig. 1. (a) A CMOS model showing an ideal switch in series with resistor. (b) Charging. (c) Discharging.
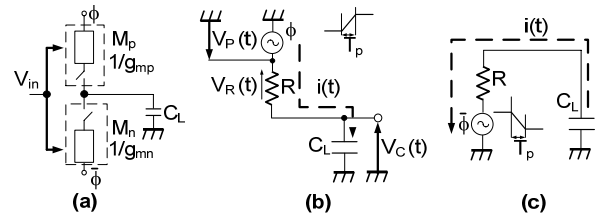
Fig. 2. (a) Model of adiabatic logic showing an ideal switch in series with resistance and two complementary voltage supply clocks. (b) Charging. (c) Discharging.

instead of a fixed voltage supply. Each voltage changes with time, as demonstrated in Fig. 3.

The peak current in adiabatic circuits can be significantly reduced by ensuring uniform charge transfers over the entire available time. Hence, if $\hat{I}$ is considered as the average of the current flowing to C_L, the overall energy dissipation during the transition phase can be reduced in proportion as follows [2]:

$$E_{\text{diss}} = \hat{I}^2 RT_p = \left(\frac{C_L V_{dd}}{T_p} \right)^2 RT_p = \left(\frac{RC_L}{T_p} \right) C_L V_{dd}^2. \qquad (2)$$

Theoretically, during adiabatic charging, when the time for the driving voltage ϕ to change from 0 V to V_{dd}, T_p is long, power dissipation is nearly zero.

When $\bar{\phi}$ changes from HIGH to LOW in the pull-down network, discharging via the nMOS transistor occurs. From Eq. (2), it is apparent that when power dissipation is minimized by decreasing the rate of switching transition, the system draws some of the energy that is stored in the capacitors during a given computation step and uses it in subsequent computations. The signal energy may be recycled instead of dissipated as heat [2]. It must be noted that systems based on the abovementioned theory of charge recovery are not necessarily reversible.
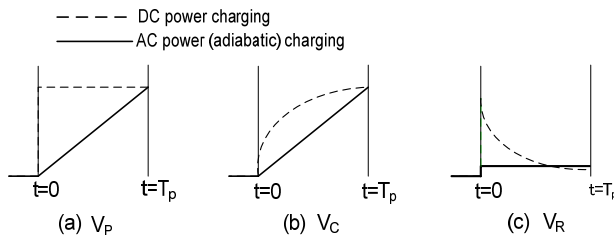

Fig. 3. Graph showing the changes of the voltage in adiabatic circuits to conventional dc power supply at the (a) power supply V_P, (b) node capacitance V_C, and (c) resistance V_R.

B. Conventional Adiabatic Logic Circuits

In this subsection, we will review the conventional adiabatic logics that are converted from CMOS static logic topology; 1n1pSLP, 1n1p quasi, ADCL, QSERL, and 2PADCL.

The first representative circuit is an asymptotically adiabatic circuit, 1n1p, with a split-level driving pulse [8]. As shown in Fig. 4, this circuit comprises a
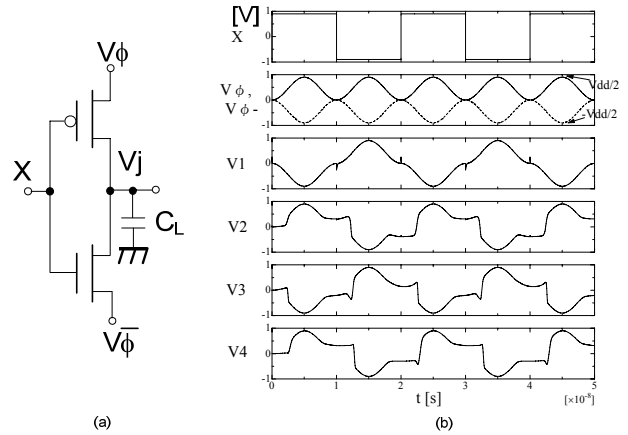

Fig. 4. (a) 1n1p split-level pulse adiabatic logic and (b) waveforms from the simulation of 4-inverter chain.

conventional CMOS gate with two complementary split-level pulse voltage drivers. The peak voltage of each clock supplies $V_{dd}/2$ to the gates.

The two major drawbacks of this asymptotically adiabatic logic are as follows: first, it cannot provide pipelining, and second, it is difficult to design the voltage driver of this circuit [12].

Although constructing logic with asymptotically zero energy loss [8] is feasible, schemes with partial (quasi) energy recovery [7, 9, 11, 14] are preferred because implementation becomes much simpler and area-efficient.

By implementing 1n1p quasi adiabatic [7] logic, it is possible to achieve quasi-adiabatic operations with conventional static CMOS gates under one-phase driving, as shown in the 1n1p quasi logic illustrated in Fig. 5. If the driver is varied sufficiently slowly, dissipation occurs only during the charging and discharging of the load capacitor. The power dissipation is minimum when the threshold voltages of nMOS and pMOS are equal in
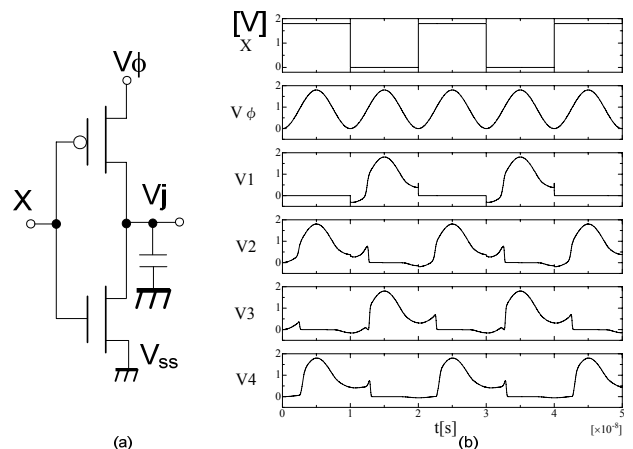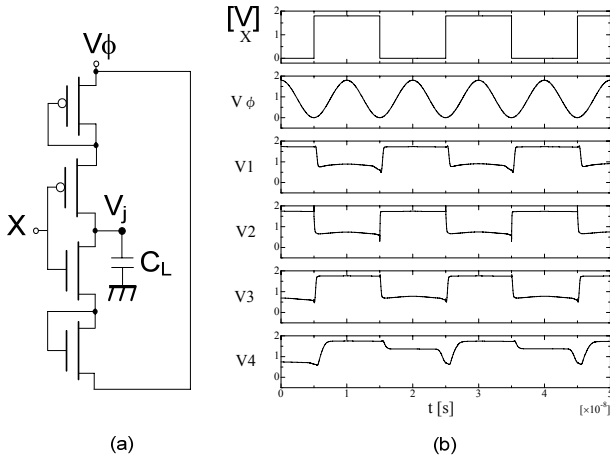

Fig. 5. (a) 1n1p quasi adiabatic logic and (b) waveforms from the simulation of 4-inverter chain.

magnitude ($V_{tn} = -V_{tp} = V_t$). However, the disadvantage of the 1n1p quasi logic is that it is also not suitable for pipelining.

Fig. 6 shows a diode-based adiabatic dynamic CMOS logic (ADCL) circuit [9]. It uses one clock supply in order to achieve a low-energy system. However, the delay time of each gate is one-half of the periodic power voltage in the ADCL circuit. This time delay decreases the operating speed of ADCL when a large number of gates are used.

The quasi-static energy recovery logic (QSERL) [11] and two-phase adiabatic dynamic CMOS logic (2PADCL) circuits [14] as shown in Fig. 7 and Fig. 8 respectively, lack robustness as a result of output floating associated with the alternate hold phases in operation [15]. Although the floating can be eliminated by adding a clocked feedback keeper to each logic circuit, unwanted power loss will still occur.

Fig. 6. (a) ADCL adiabatic logic and (b) waveforms from the simulation of 4-inverter chain.
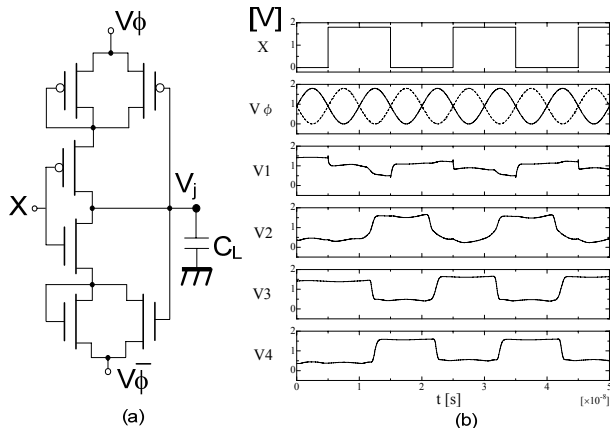
Fig. 7. a) QSERL adiabatic logic and (b) waveforms from the simulation of 4-inverter chain.
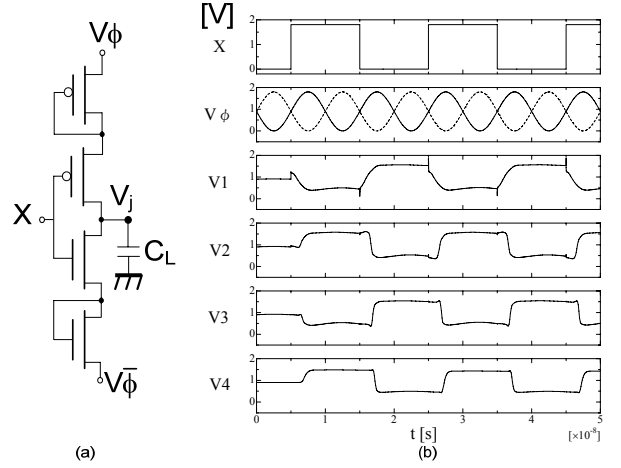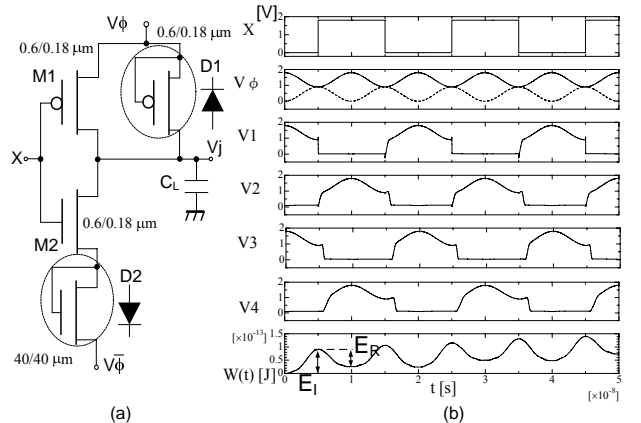

Fig. 8. (a) 2PADCL adiabatic logic and (b) waveforms from the simulation of 4-inverter chain.

III. TWO PHASE CLOCKED ADIABATIC STATIC CMOS LOGIC

1. Circuit Structure

Fig. 9 shows a circuit diagram and waveforms illustrating the operation of the 2PASCL 4-inverter chain logic. A two-diode circuit is used—one diode is placed between the output node and power clock, and the other diode is placed adjacent to the nMOS logic circuit and connected to another power source. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. Such a circuit design is particularly advantageous

Fig. 9. (a) 2PASCL adiabatic logic and, (b) the simulated waveforms of 4-inverter chain; transition frequency X=50 MHz, $V\phi=V\bar{\phi}$ =100 MHz. The last graph shows the energy injected from the clock generator E_I and energy that received back from the circuit capacitance E_R; therefore the energy dissipation at each transition is only $E_I - E_R$.

if the signal nodes are preceded by a long chain of switches.

The proposed system uses a two-phase clocking split-level sinusoidal power supply, wherein $V\phi$ and $V\bar{\phi}$ replace V_{dd} and V_{ss}, respectively. One clock is in phase while the other is inverted. The voltage level of $V\phi$ exceeds that of $V\bar{\phi}$ by a factor of $V_{dd}/2$. By using these two split-level sinusoidal waveforms, which have peak-to-peak voltages of 0.9 V, the voltage difference between the current-carrying electrodes can be minimized; and consequently, power consumption can be suppressed. The substrates of the pMOS and nMOS transistors are connected to $V\phi$ and $V\bar{\phi}$, respectively.

Since the criteria for maintaining thermal equilibrium —the voltage between the current-carrying electrodes is zero when the transistors are in the ON state [12] —are satisfied, the energy accumulated in C_L is not dissipated. The results of the simulation performed using a "simulation program with an integrated circuit emphasis (SPICE)" circuit simulator reveal that adiabatic circuits powered by the split-level sinusoidal waveforms consume less energy than a trapezoidal-waveform clock power supply, even when the rise and fall times of the trapezoidal waveforms are set to their maximum values. Moreover, sinusoidal waveforms can be generated with higher energy efficiency than trapezoidal waveforms [11].

2. Circuit Operation

The circuit operation is divided into two phases: *evaluation* and *hold,* as illustrated in Fig. 10. In the *evaluation* phase, $V\phi$ swings up and $V\bar{\phi}$ swings down. On the other hand, in the *hold* phase, $V\bar{\phi}$ swings up and $V\phi$ swings down. Let us consider the inverter logic circuit demonstrated in Fig. 9. The operation of the 2PASCL inverter is explained as follows:

1) *Evaluation* phase:
   a) When the output node Y is LOW and the pMOS tree is turned ON, C_L is charged through the pMOS transistor; hence, the output is in the HIGH state.
   b) When node Y is LOW and nMOS is ON, no transition occurs.
   c) When the output node is HIGH and the pMOS is ON, no transition occurs.
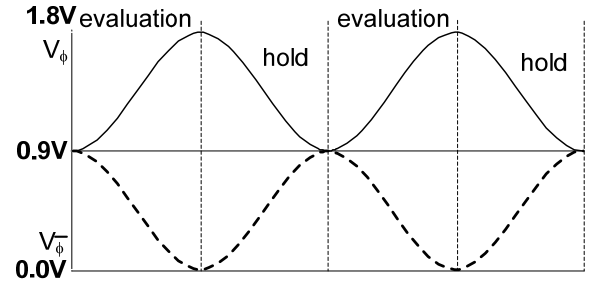
Fig. 10. The clocked voltage driver showing the evaluation and hold phases.

   d) When node Y is HIGH and the nMOS is ON, discharging via nMOS and D2 causes the logic state of the output to be "0" [14].

2) *Hold* phase:
   a) When node Y is LOW and the nMOS is ON, no transition occurs.
   b) At the point when the preliminary state of the output node is HIGH and the pMOS is ON, discharging via D1 occurs.

The number of dynamic switching transitions occurring during the operation of the 2PASCL circuit decreases since the charging/discharging of the circuit nodes does not necessarily occur during every clock cycle. Hence, node switching activities are suppressed to a significant extent, and consequently, power dissipation is also reduced. One of the advantages of the 2PASCL circuit is that it can be made to behave like a static logic circuit.

3. Theoretical Analysis

In adiabatic circuits, power dissipation occurs through the threshold voltage and transistor channel resistance. To estimate the energy consumption in adiabatic circuits, we utilize an RC model with a threshold voltage V_t. The energy dissipation in a 2PASCL inverter is as follows:

$$
\begin{aligned}
E_{2PASCL} &= E_{chrg(M1)} + E_{dischrg(D1)} + E_{dischrg(M2,D1)} \\
&= 0.5C_L V_{tp}^2 + 0.5C_L V_{\phi p-p} |V_{tp}| + 0.5C_L \left(V_{\bar{\phi} p-p} - V_{tn}\right) V_{tn} \\
&= 0.5C_L \left(V_{tp}^2 + V_{\phi p-p}|V_{tp}| + \left(V_{\bar{\phi} p-p} - V_{tn}\right) V_{tn}\right),
\end{aligned}
\tag{3}
$$

where C_L is the load capacitance; V_{tp}, the threshold voltage of pMOS; V_{tn}, is the threshold voltage of nMOS; and $V\phi_{p-p}$ and $V\bar{\phi}_{p-p}$, the voltage supplies.

By assuming $C_L = 0.01$ pF, $V_{tp} = -0.24$ V, $V_{tn} = 0.58$ V and $V_{\phi p-p} = V_{\bar{\phi} p-p} = 0.9$ V, the theoretical calculations are plotted.

As shown in Fig. 11, the power dissipation at each transition frequency is compared. The unmatched values of the simulation and analytical results are primarily because of the shape factor [17] of voltage drivers, which were not considered in the theoretical calculations. We are using the split-level sinusoidal waveforms while for theoretical calculations, linear ramp waveforms are utilized. However, the trend is similar and we have understood the fundamental factors that contributed to the power dissipation in the 2PASCL inverter from this analytical analysis. From Eq. (3), by applying $V_{\phi p-p}$ and $V_{\bar{\phi} p-p}$ as split-level sinusoidal waveforms with each peak-to-peak voltage being 0.9 V, we have saved approximately 50% of the energy, as compared to non split-level waveforms.
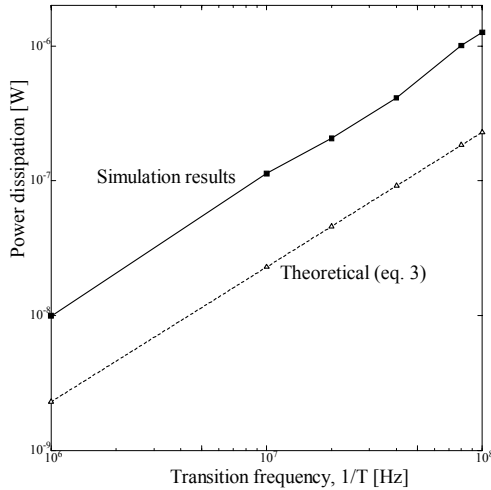
Fig. 11. Power dissipation per cycle: comparison of the simulation results and theoretical values of a single 2PASCL inverter gate.

IV. SIMULATION RESULTS AND DISCUSSION

1. Inverter Circuits

A. Simulation Condition

In this section, we examine the topology and functionality of 4-chain inverter 2PASCL gates and compare the results with CMOS, 1n1p split-level pulse, 1n1p quasi, ADCL, QSERL, and 2PADCL.

The simulations in this study were performed using a SPICE circuit simulator with a 0.18-µm, 1.8-V standard

CMOS process. The width W and length L of the nMOS and pMOS logic gates were 0.6 µm and 0.18 µm, respectively. A load capacitance C_L of 0.01 pF was connected to the output node i.e. at $V4$ for this 4-inverter chain simulation. The frequency of the power supply clock was set to a value exactly two times the transition frequency.

Simulations were performed for the following purposes: *a) Logic functions:* Evaluation of the 2PASCL 4-inverter chain at a transition frequency of 50 MHz. *b) Power dissipation:* Comparison of the power dissipation per cycle between the 4-inverter chain of 2PASCL, CMOS, and other adiabatic logic circuits at transition frequencies of 1, 10, 20, 40, 50, 80, and 100 MHz. *c) Load capacitance:* Power dissipation comparison between the 2PASCL and CMOS circuits for C_L values of 0.01, 0.02, 0.05, 0.1, 0.2, 0.3, 0.4, and 0.5 pF.

B. Simulation Results

a) Output waveforms: The SPICE simulation results obtained for the 4-inverter chain of 2PASCL are shown in Fig. 9 (b). The top graph shows the input signals, which are CMOS-compatible rectangular pulses. The middle graph shows the driving voltage of the split-level sinusoidal supply clock, and the other four graphs show the output waveform at $V1$, $V2$, $V3$ and $V4$. The 4-inverter chain simulation is performed to examine whether the output signals of cascaded logics affecting the power dissipation especially in 2PASCL. The energy dissipation is calculated by integrating the product of voltage and current as follows:

$$E = \int_0^T \left(\sum_{i=1}^n \left(V_{pi} \cdot I_{pi} \right) \right) dt , \qquad (4)$$

where T is the period of the primary input signal; V_p, the power supply voltage; I_p, the power supply current; and n, the number of power supplies [14]. The energy obtained in joules is then converted to power consumption in watt (W) by multiplying it with the input frequency.

b) Frequency characteristics of power consumption: The comparison graph shown in Fig. 12 reveals that with the 2PASCL inverter, up to 79% of the power dissipated from the CMOS inverter can be saved. The results also

show that the 2PASCL inverter offers the third lowest power dissipation among all the other adiabatic 4-inverter chain logic circuits. 1n1p quasi has the lowest since it only uses single clock. However, as described earlier, 1n1p quasi based circuit is difficult for pipelining. Furthermore, as clearly demonstrated in Fig. 4 and 5, 1n1p split-level pulse adiabatic and 1n1p quasi are not producing good output waveforms. The advantage of 2PASCL is that it is capable of pipelining and has been proved to work in more complicated and cascaded logic circuits. ADCL is taken out from the comparison graphs as it only operated at only very low transition frequency for this simulation. To further show the consequences of the output signal in power dissipation, we calculate the average power dissipation of a single inverter, 2-inverter, 3-inverter and 4-inverter chains. The simulation results are shown in Fig. 13. From the graph we understand that
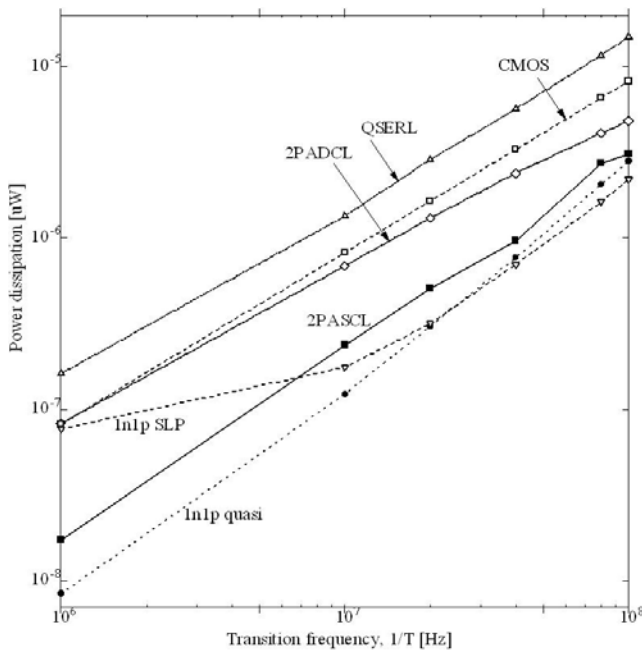

Fig. 12. Energy dissipation comparison of 2PASCL 4-inverter chain to CMOS and other simple adiabatic logics at transition frequencies of 1 to 100 MHz.
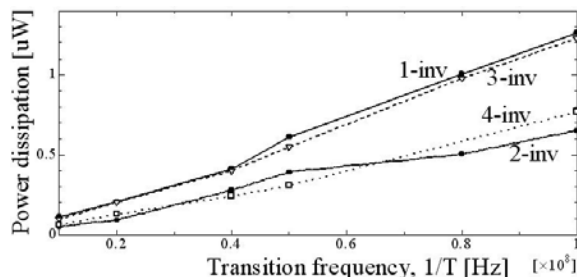
Fig. 13. Average power dissipation of an inverter in a 1-,2-,3- and 4-inverter chain.

the output waveforms which will be the next input signals do not affect the power dissipation of the cascaded inverters using 2PASCL topology.

c) Power dissipation at different values of C_L: The simulation results show that the power dissipation in the 2PASCL inverter is in average 65% lower than that of static CMOS when C_L values are changed from 0.01 to 0.5 pF, as shown in Fig. 14.
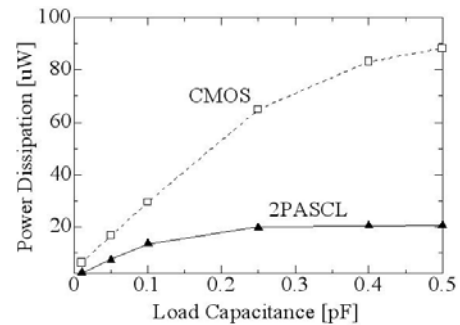

Fig. 14. Energy comparison of 2PASCL inverter to CMOS for load capacitance from 0.01 to 0.5 pF using 4-inverter chain logics.

## 2. Combination Logic Circuits

By considering the output waveforms shape of the combination circuits below which are similar to inverter circuit waveforms, we design NAND, XOR and NOR based on 2PASCL and compare a non-cascaded gate to those design using conventional CMOS. The first combination circuit examined in this study is NAND logic. Our proposed schematic is shown in Fig. 15. The logic function of the circuit is confirmed. From the comparison study with CMOS as shown in Fig. 18, we find that a 2PASCL-based NAND circuit can save up to 69% at transition frequencies of 1 to 100 MHz.

We then simulated two combination logic circuits— 2PASCL-based XOR and NOR circuits. Both the schematics are demonstrated in Figs. 16 and 17, respectively. By using the split-level sinusoidal driving clocks, the proposed XOR and NOR have 36% and 72% lower energy than conventional static CMOS, respectively.

As shown in Fig. 16, the scheme for a 2PASCL XOR has no diode at the output Y. The discharging diodes of pMOS are placed only at the inverter site of the circuit. However, in the case of an nMOS diode, it remains adjacent to the nMOS logic circuit and $V\bar{\phi}$.
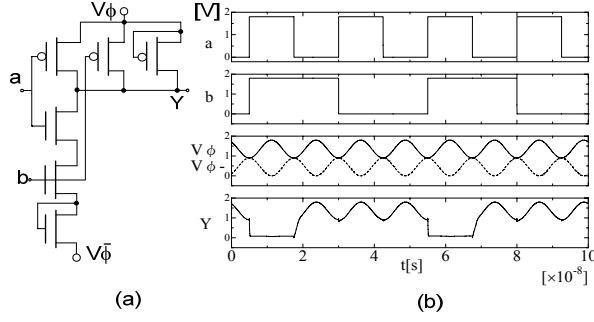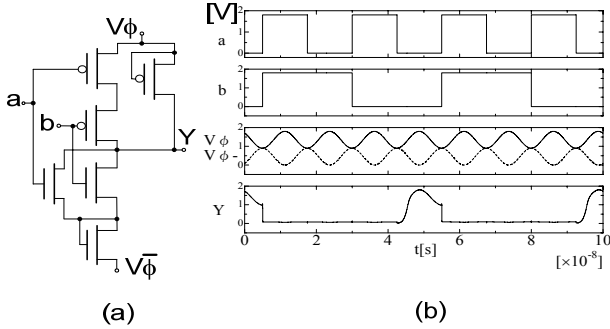
Fig. 15. (a) Scheme for 2PASCL-based NAND logic, and (b) waveforms from the simulation.
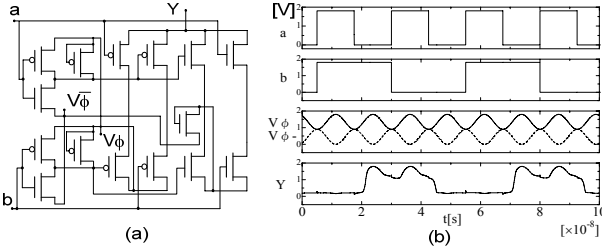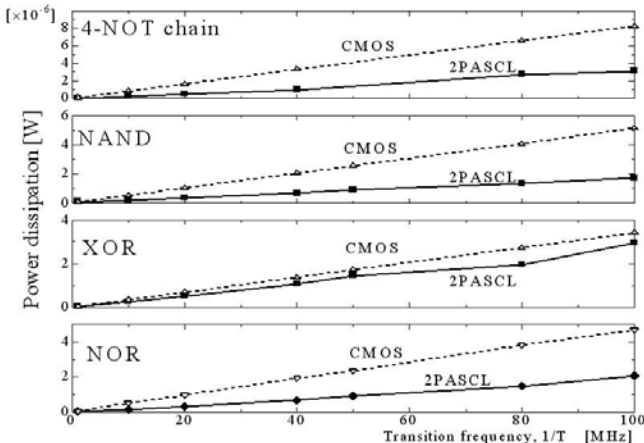

Fig. 16. (a) Scheme for 2PASCL-based XOR logic, and (b) waveforms from the simulation.

Fig. 18 shows the simulation results of power dissipation for 2PASCL 4-inverter chain, NAND, XOR,

Fig. 17. (a) Scheme for 2PASCL-based NOR logic, and (b) waveforms from the simulation.

Fig. 18. Power dissipation of 2PASCL 4-inverter chain, NAND, XOR and NOR logics compared to CMOS.

and NOR logics as compared to CMOS topology. At the transition frequencies of 1 to 100 MHz, the power dissipation of logics using 2PASCL topologies show lower power dissipation compared to CMOS.

V. POWER CLOCK GENERATOR

In Fig. 19, we present a simple LC resonant oscillator for driving two complementary clock-supply nodes of a 2PASCL system. It is an extended circuit first introduced by Himman and Schlecht [18].

The waveform presented at V_ϕ and $V_{\bar\phi}$ will be a sine wave with amplitude that decreases with time due to the resistive losses in the inductor. To maintain the amplitude of the supply waveform, switches to the dc supply. M1 and M2 are provided. The gates are activated by pulse generator V_{G1} and V_{G2}. Voltage regulator with $3V_{dd}/4$ and $V_{dd}/4$ are used to increase the voltage level for generating split-level sinusoidal waveforms as demonstrated in the next equations.

$$V_\phi \cong \frac{V_{dd}}{2}\sin(\omega_0 t) + \frac{3}{4}V_{dd} ,$$
$$V_{\bar\phi} \cong \frac{V_{dd}}{2}\sin(\omega_0 t) + \frac{1}{4}V_{dd} . \tag{5}$$
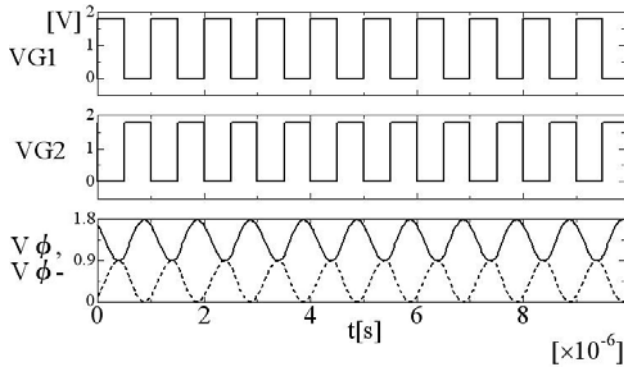
The resonant frequency is

$$\omega_0 = \frac{1}{\sqrt{(L_1 + L_2)C}} . \tag{6}$$

The input waveforms of V_{G1}, V_{G2} and the output waveforms V_ϕ and $V_{\bar\phi}$ at 1 MHz are as shown in Fig. 20. From the simulation results, to generate 1 MHz of
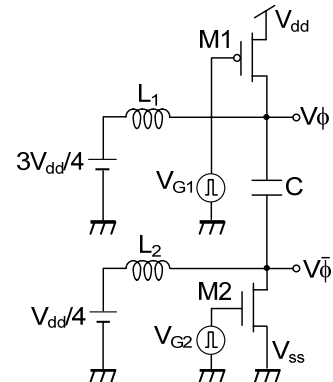
Fig. 19. Two-phase split-level sinusoidal power clock generator circuit for 2PASCL.

Fig. 20. 1 MHz split-level sinusoidal waveforms produced from power generator described in Fig. 19.

two complementary split-level sinusoidal clocks, the circuit consumes 16 µW of power from the supply.

The parameters used in Fig. 19 are summarized in Table 1.

Table 1. Parameters for elements in power clock generator circuit.

L1, L2	110 µm
C	61.7 pF
M1 W/L	0.24 µm/ 0.18 µm
M2 W/L	0.18 µm/ 0.18 µm
V_{dd}	1.8 V

VI. DISCUSSION

While the 2PASCL circuit has advantages such as low power dissipation and high fan out, its main disadvantage is floating outputs, which are attributed to the alternate hold phases that exist during the circuit operation. These problems will be addressed in our future research.

VII. CONCLUSIONS

In this paper we have proposed a two-phase clocked adiabatic CMOS logic (2PASCL) circuit and its power clock generator. The simulation results show that power consumption in the 2PASCL NOT, NAND, XOR and NOR circuits are considerably **less** than that in a CMOS. For instance, when the input frequency is simulated from 1 to 100 MHz, the 2PASCL inverter logic dissipates minimally as only 21% of the power dissipated by a static CMOS in 4-inverter chain logic circuit. Furthermore, the energy dissipated by a 2PASCL inverter remains low even when the load capacitance is increased. We believe that the proposed adiabatic logic circuit is advantageous for ultra low-energy computing applications.

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